INTRODUCTION TO CCD AND CMOS IMAGING SENSORS AND APPLICATIONS (SC504)

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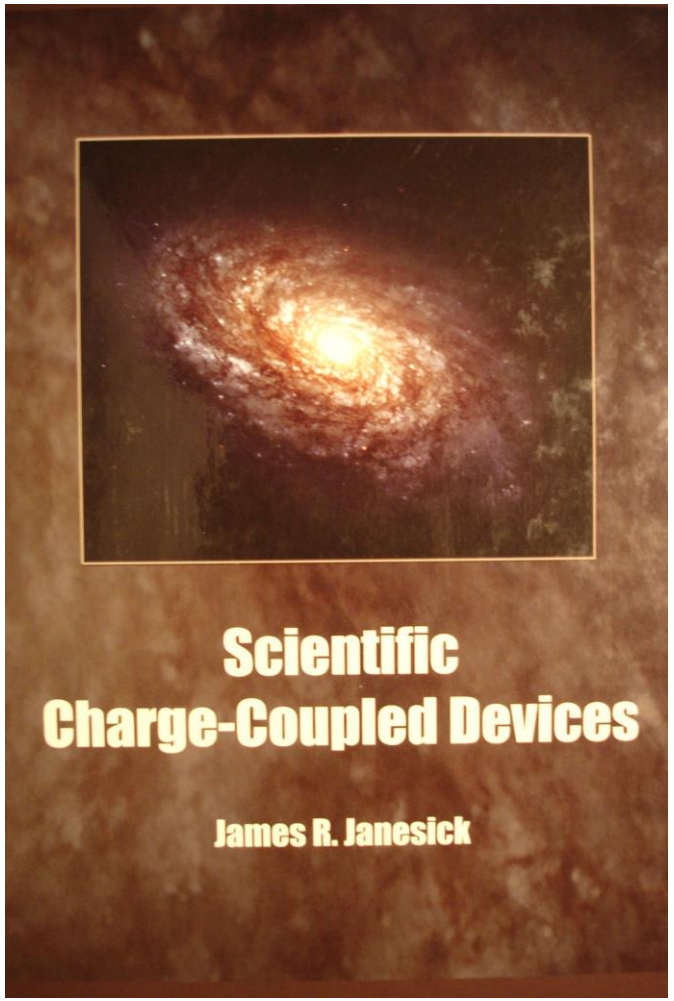
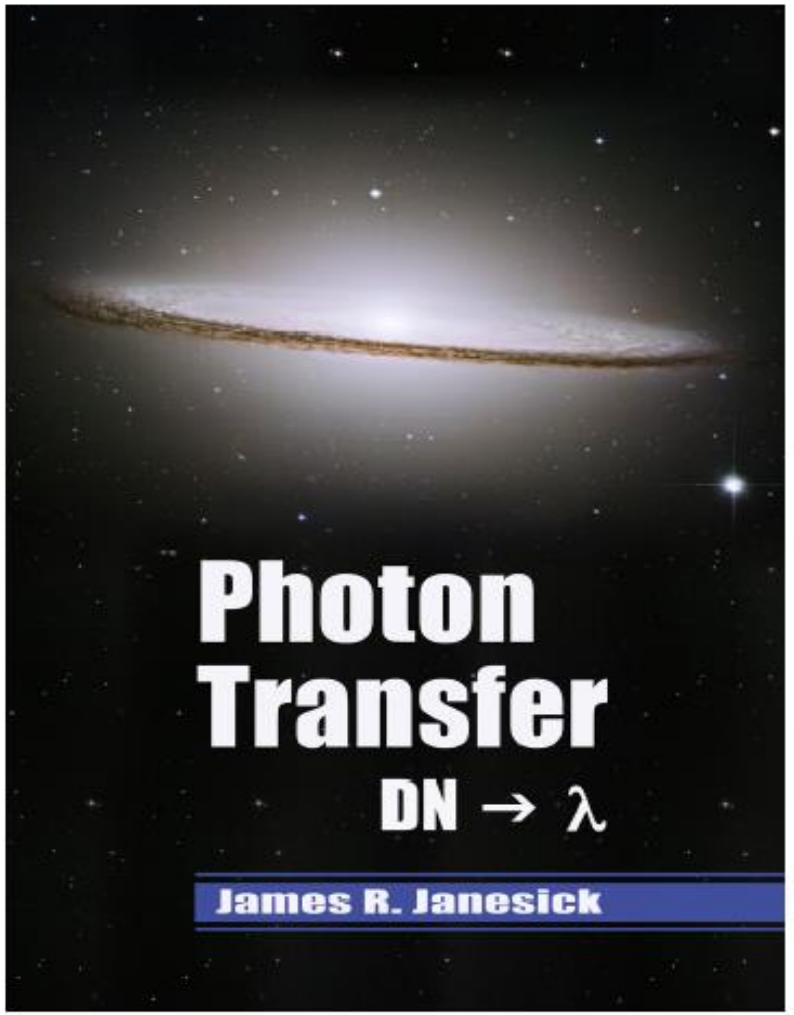
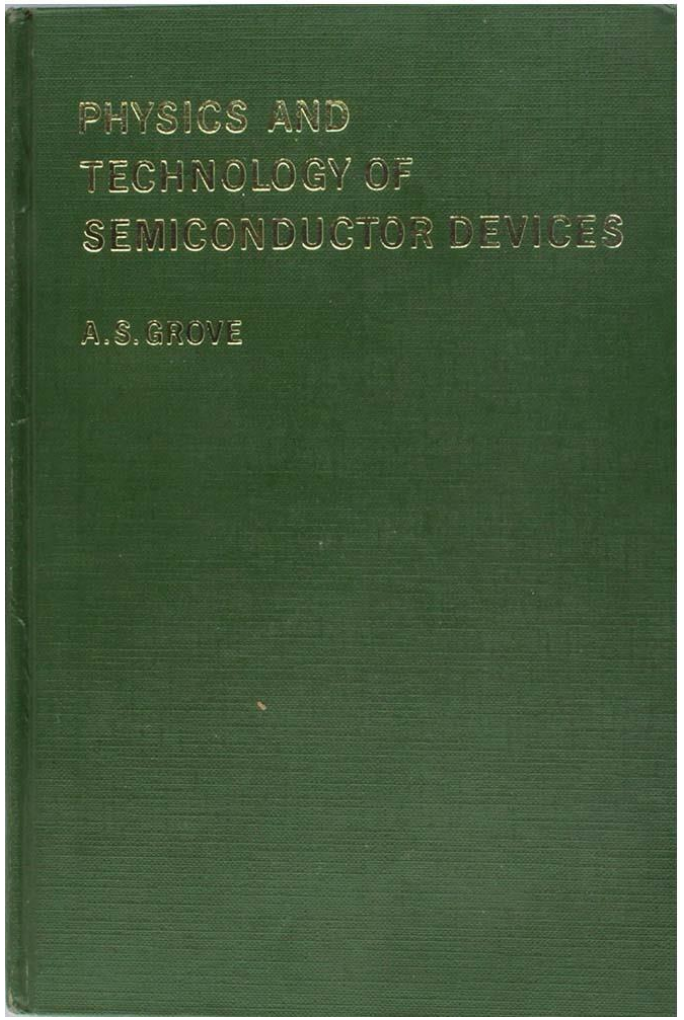
Main Reference Sources for this Talk







INTRODUCTION TO CCD AND CMOS IMAGING SENSORS AND APPLICATIONs

Part 1: Basic Principles & Concepts

Part 2: Charge Generation

Part 3: Charge Collection

Part 4: Charge Transfer

Part 5: Charge Measurement

Part 6: Noise Sources

Part 7: Performance Measurement

Part 8: Important CMOS Performance Differences vs CCD

Part 9: Manufacturing

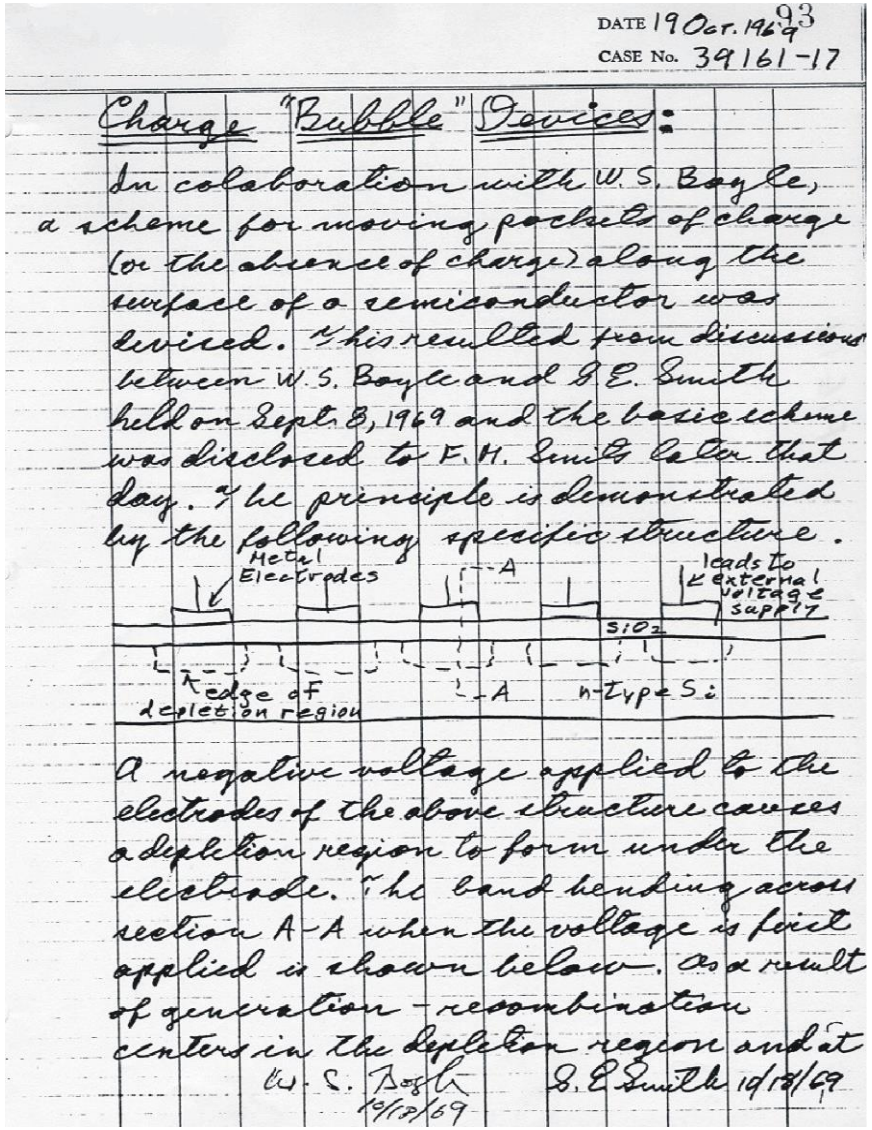
Part 10: CMOS Pixel Scaling

Part 11: Design Problem: Selecting the right Image Sensor for the job

Part 1

Basic Principles & Concepts

CCD INVENTION



DATE 19 Oct. 1969 93
CASE No. 39161-17

Charge "Bubble" Devices:

In colaboration with W. S. Boyle, a scheme for moving pockets of charge (or the absence of charge) along the surface of a semiconductor was devised. This resulted from discussions between W. S. Boyle and G. E. Smith held on Sept. 8, 1969 and the basic scheme was disclosed to F. H. Smits later that day. The principle is demonstrated by the following specific structure.

A negative voltage applied to the electrodes of the above structure causes a depletion region to form under the electrode. The band bending across section A-A when the voltage is first applied is shown below. As a result of generation-recombination centers in the depletion region and at

W. S. Boyle 10/13/69 G. E. Smith 10/13/69

Boyle & Smith ATT Bell Labs, 1969

Nobel Goes to Boyle and Smith for CCD Camera Chip

IEEE Fellows Willard Boyle and George Smith recognized for starting the digital-imaging revolution

By **Neil Savage**

Corrected 8 October 2009.

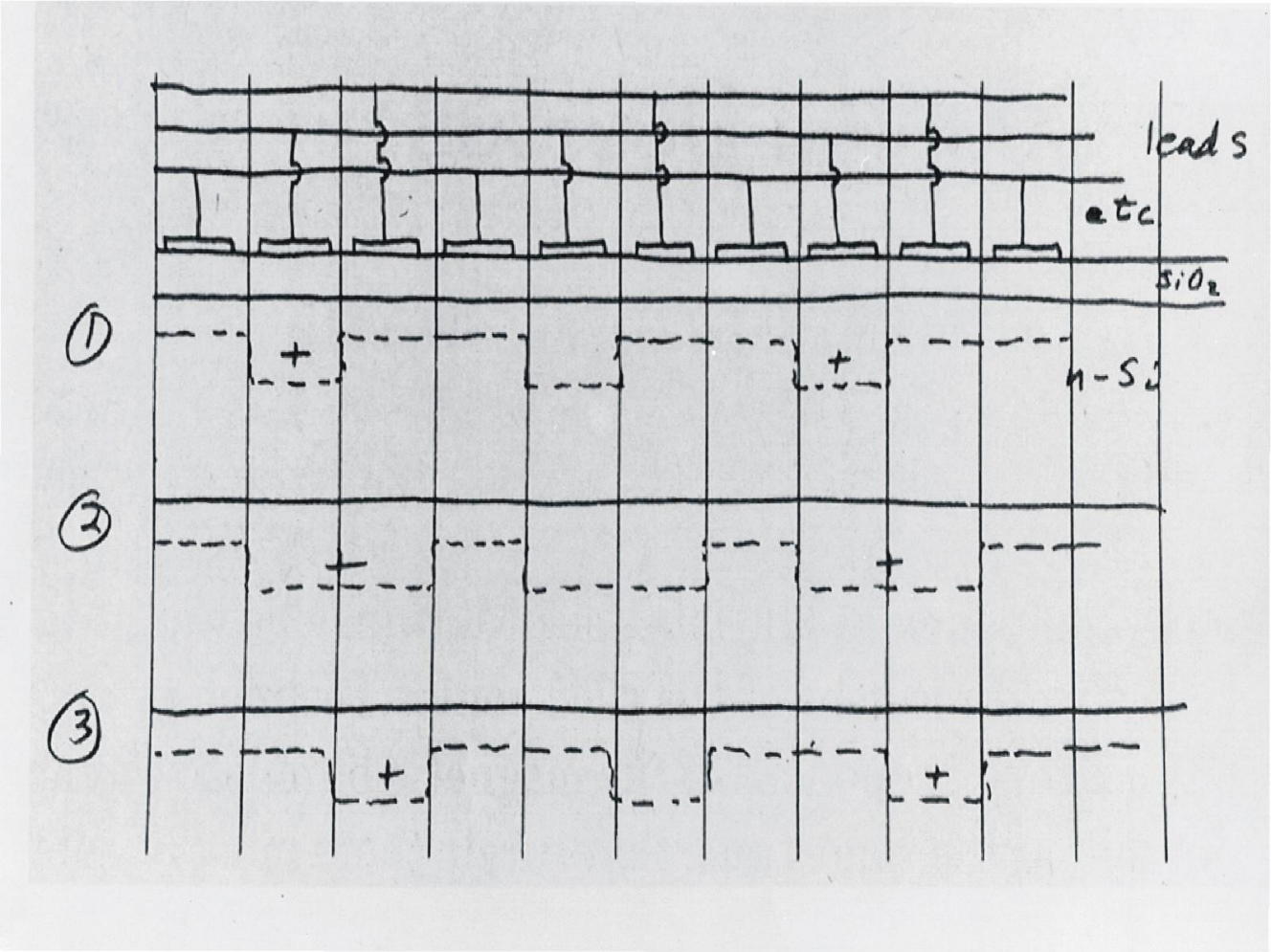
7 October 2009—Willard Boyle and George Smith, formerly of Bell Telephone Laboratories, in Murray Hill, N.J., will share half of this year's Nobel Prize in Physics "for the invention of an imaging semiconductor circuit-the CCD," the basis for digital imagery in everything from pocket cameras to the Hubble Space Telescope. (The "imaging" part of the citation is in dispute, as the first imaging CCD was developed by IEEE Fellow Michael F. Tompsett, a colleague of Boyle and Smith.) In announcing the awards, the Royal Swedish Academy of Sciences called Boyle and Smith "masters of light" and said that, with fellow winner and optical-fiber pioneer Charles Kuen Kao, they "helped to shape the foundations of today's networked societies."

Boyle and Smith came up with the idea for the CCD during a brief meeting in 1969. The two were working on semiconductor integrated circuits, and Smith had been involved with trying to create an imaging chip for the Picturephone, which consisted of an array of silicon diodes. At the time, Bell Labs was also working on a new type of computer memory that relied on tiny bubbles of magnetism. As the two recalled in a 1976 article in *IEEE Transactions on Electronic Devices* , their boss, Jack Morton, urged them to look at whether it was possible to make a form of bubble memory using semiconductors.

The idea is fairly simple. You start with a layer of silicon, doped so that it's deficient in electrons and oxidized at the surface. Atop the oxide, add an array of metal electrodes as gates, creating capacitors that can store charge. Then apply a voltage to the gate, which repels the silicon's positive carriers—the holes—and creates a potential well at the surface of the silicon. When a photon strikes the silicon, it creates an electron-hole pair, and the electron moves toward an electrode into the well. Electrons accumulate in the interface between the silicon and the oxide. When you apply a sequence of high and low voltages to adjacent gates, the electrons move from one gate to the next, like water being poured from one bucket to another, until they reach the edge of the chip, where the level of charge can be read as a measure of light intensity.

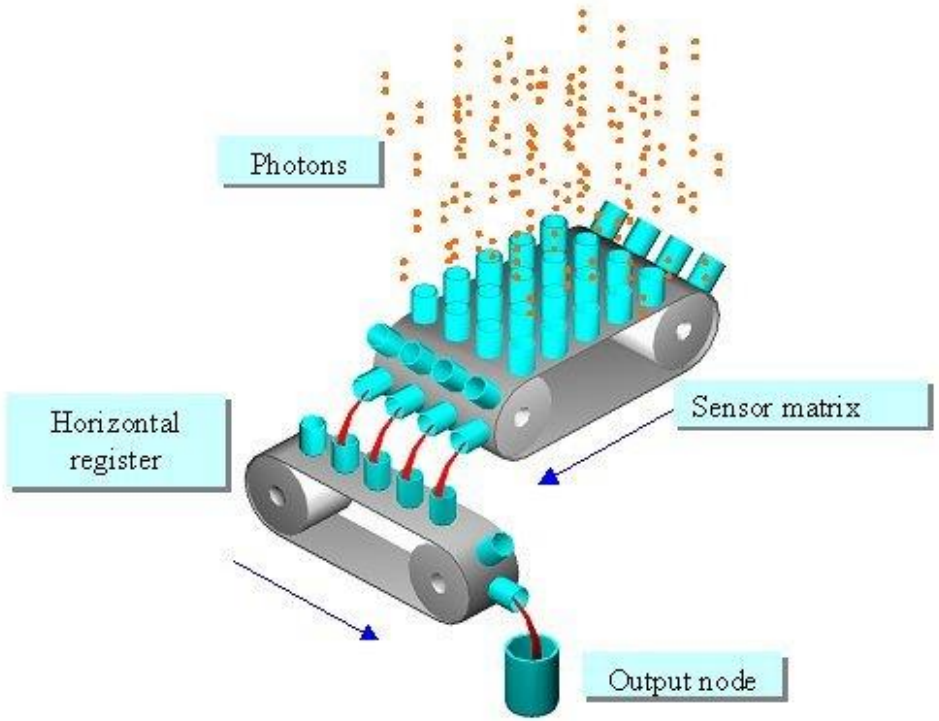
Nobel Prize in Physics 2009

CCD INVENTION - 1969

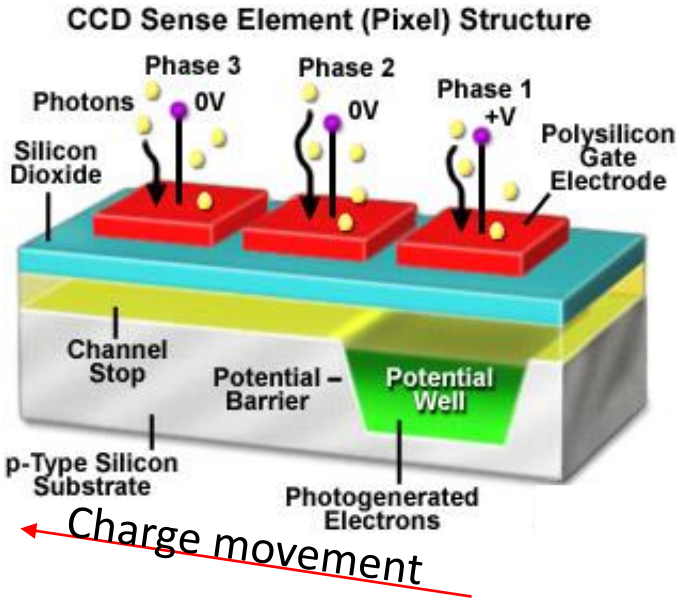


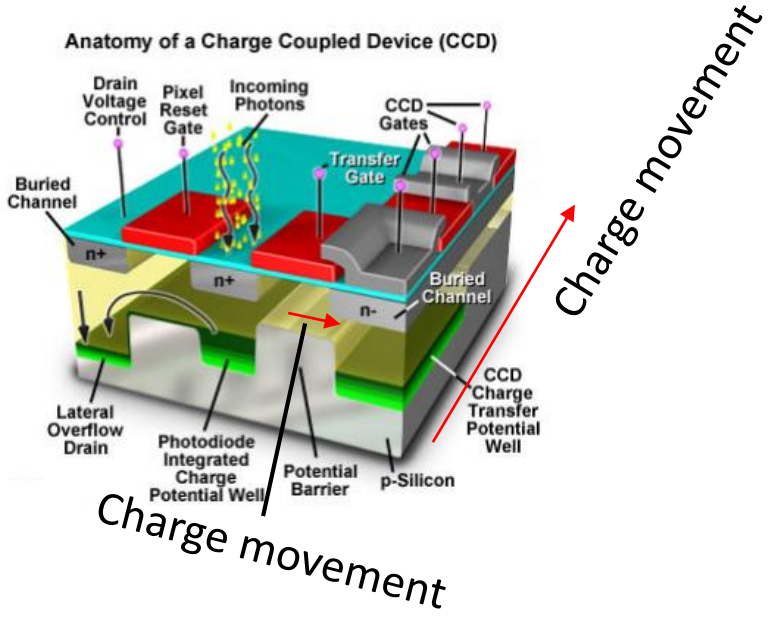
From Lab Notebook

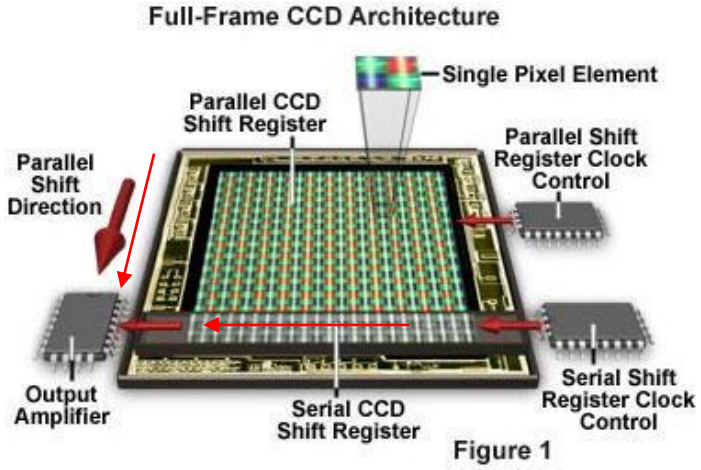
CCD Operation



CCD Operation



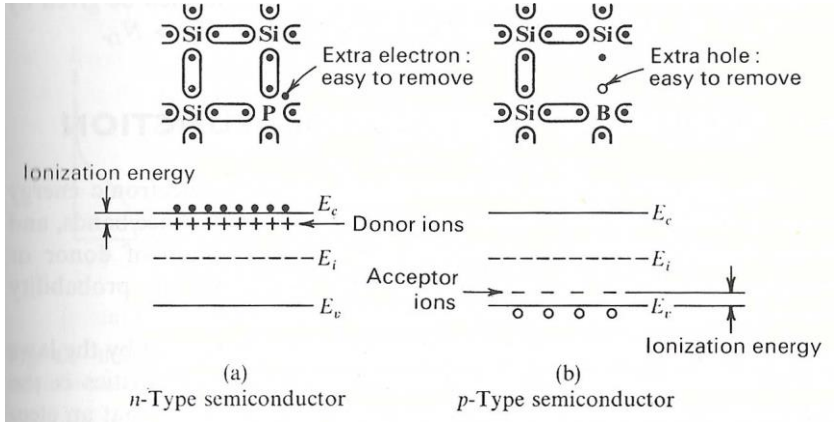




Key CCD Functions

- **CHARGE GENERATION:**
  - **-PHOTO- ELECTRIC EFFECT**
  - **-Light to charge conversion**
- **CHARGE COLLECTION:**
  - **-POTENTIAL WELL**
  - **-Create discrete regions to capture charge (pixels) in XY array**
- **CHARGE TRANSFER:**
  - **-POTENTIAL WELL**
  - **-Move charge from pixels to where it can be measured**
- **CHARGE MEASUREMENT:**
  - **-SENSE CAPACITOR**
  - **-Charge on capacitor creates voltage that is sensed**

Doping: N and P type Silicon



At equilibrium:
$n * p = n_i^2$

n= mobile electrons/cm^3
p= mobile holes/cm^3

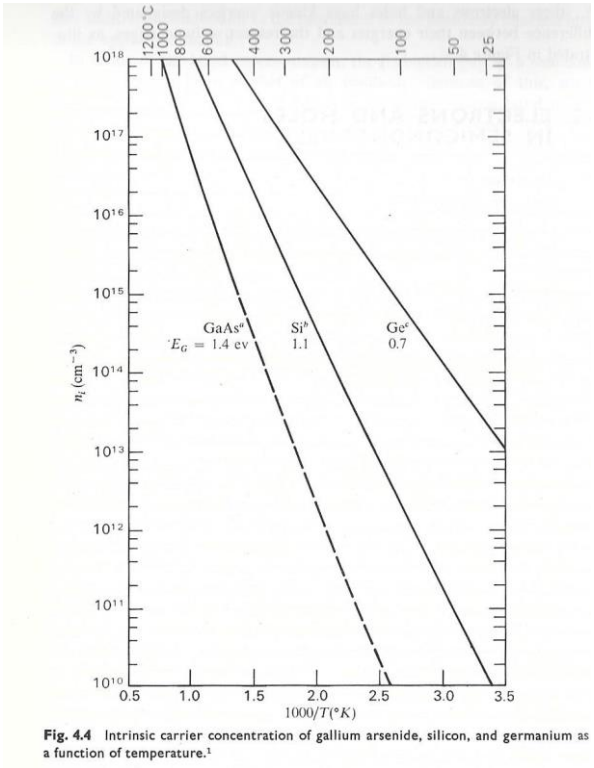
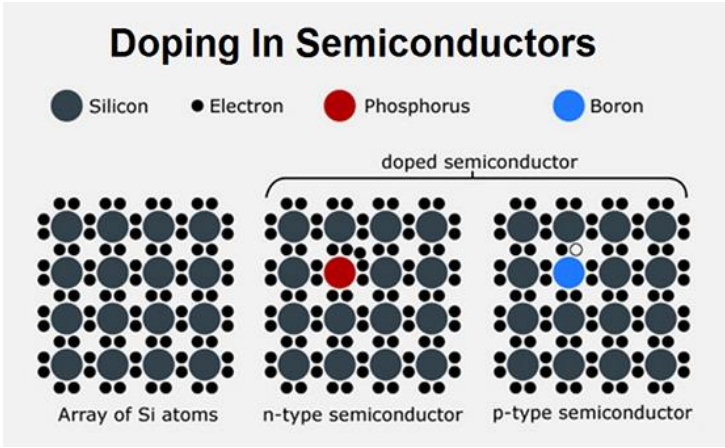


Fig. 4.4 Intrinsic carrier concentration of gallium arsenide, silicon, and germanium as a function of temperature.[1]



N_A = # Acceptor Atoms/ cm^3 (boron)
N_D = # Donor Atoms/ cm^3(phosphorus)

At room temperature:
In Ptype silicon, p_{p0} = ~ N_A
In Ntype silicon, n_{n0} = ~ N_D

Photo-electric Effect

Einstein's Nobel Prize (1921)

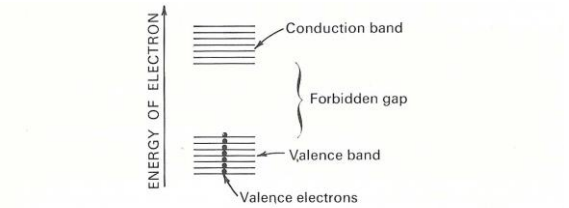
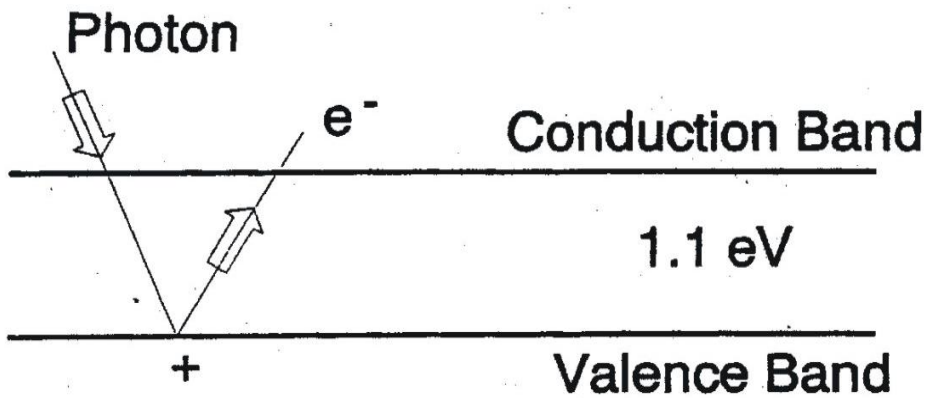


Fig. 4.1 Schematic energy band representation for electrons in a solid illustrating the energy bands and a forbidden gap.



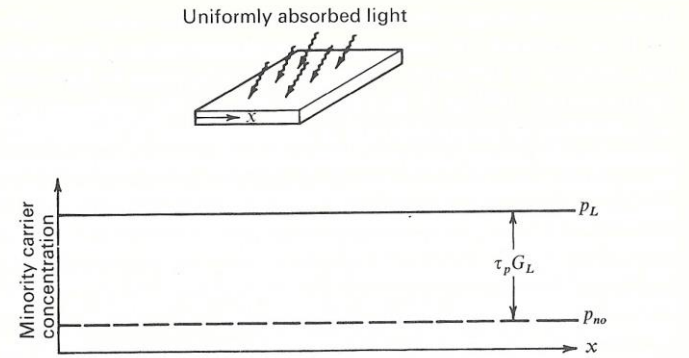
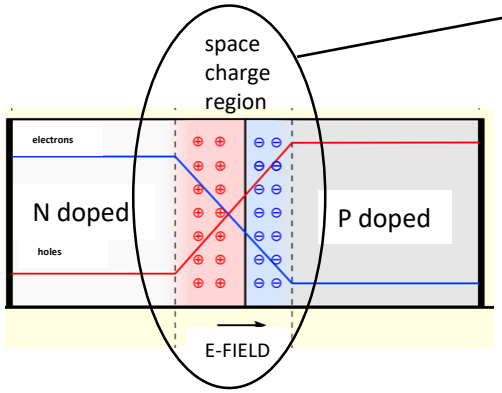


Fig. 5.2 Illustration of the steady-state minority carrier distribution in a uniformly illuminated semiconductor sample, in the absence of surface recombination.

- **4000 A < λ < 10,000 A , $e^- = 1$**
- **1 A < λ < 1000 A , $e^- =$ eV/ 3.65 eV/e-**

PN Junction & Depletion Region



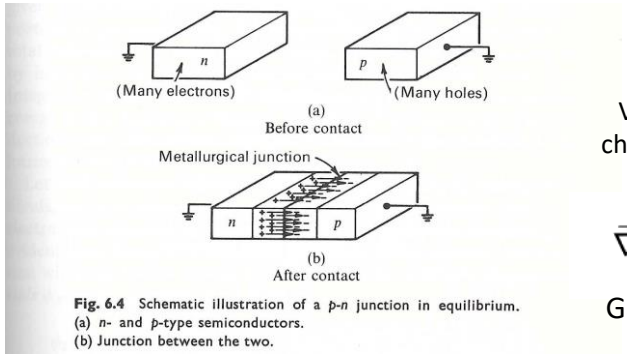
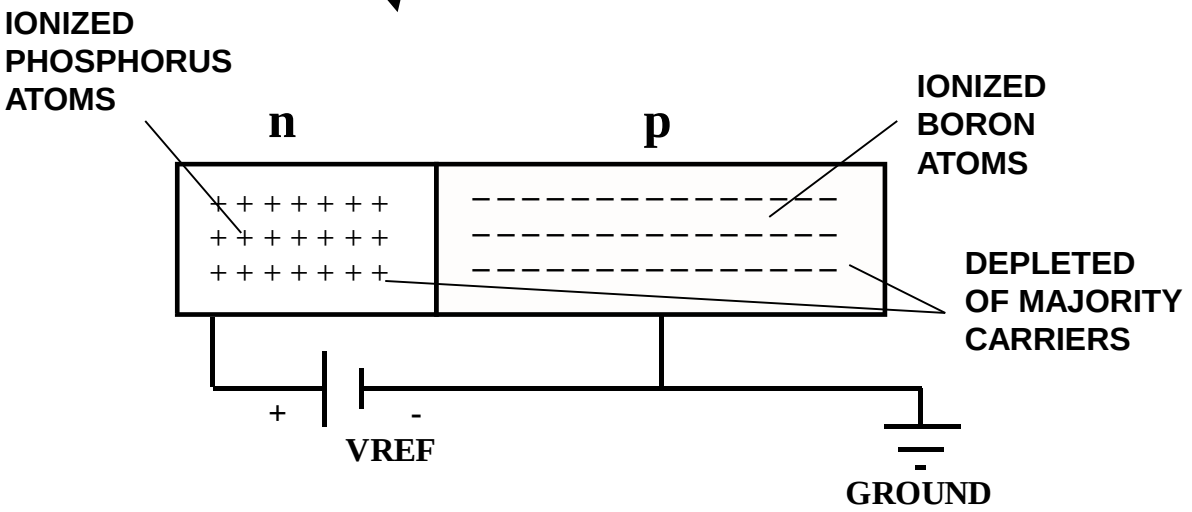


Fig. 6.4 Schematic illustration of a *p-n* junction in equilibrium. (a) *n*- and *p*-type semiconductors. (b) Junction between the two.

DIODE



CHARGE

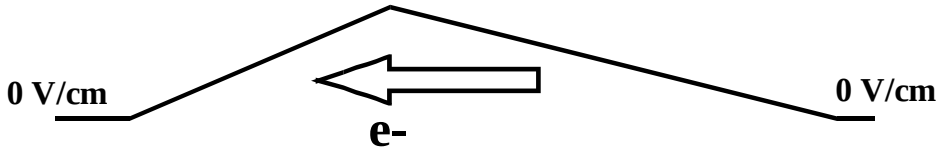
ρ

Volumetric charge density

ELECTRIC FIELD

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon_0}.$$

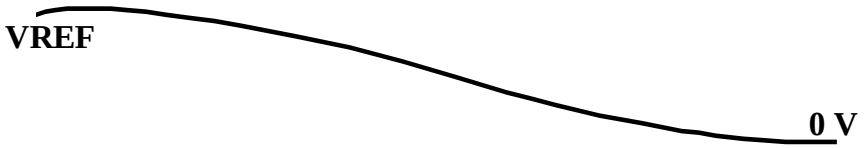
Gauss's Law



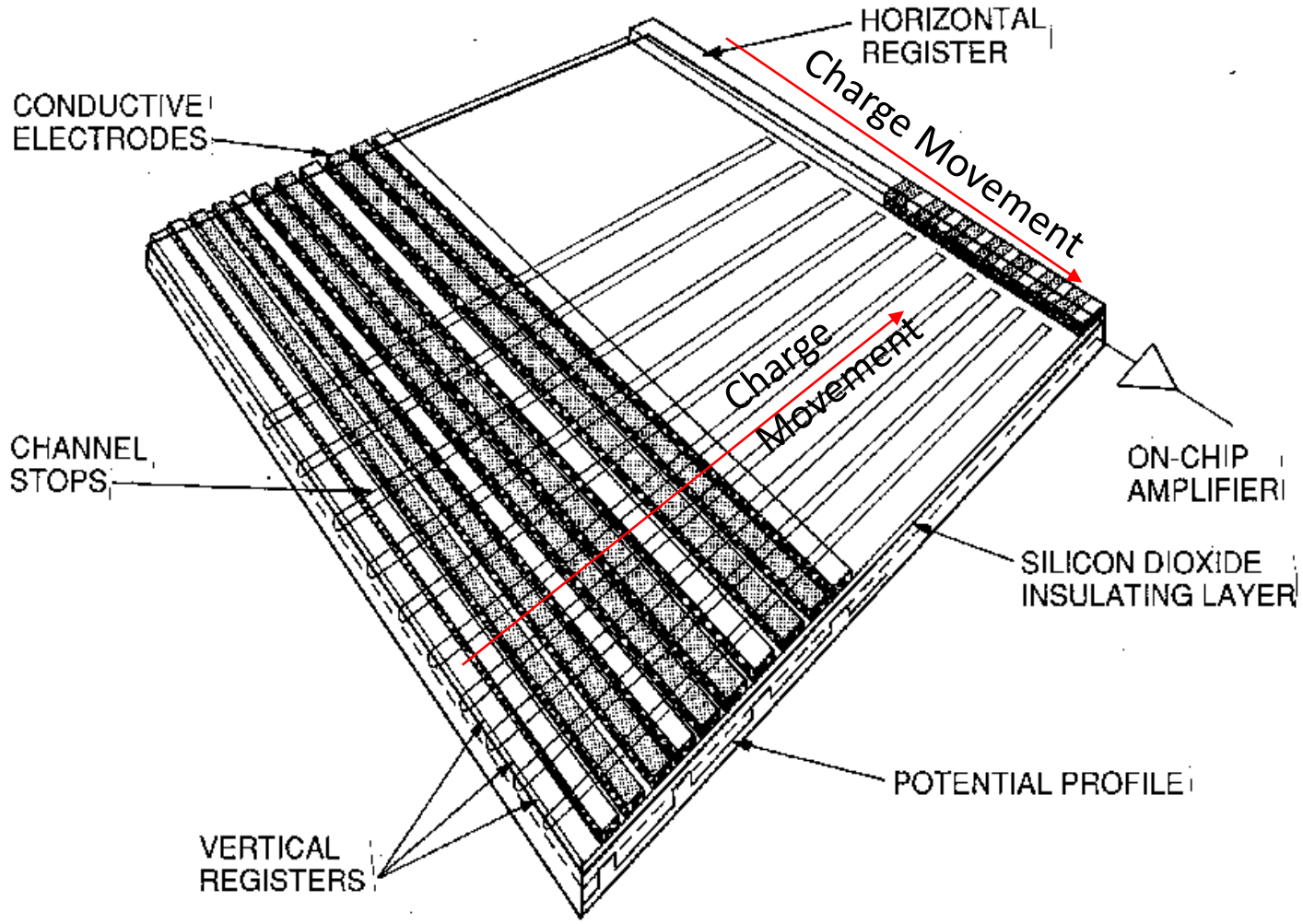
POTENTIAL

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon}.$$

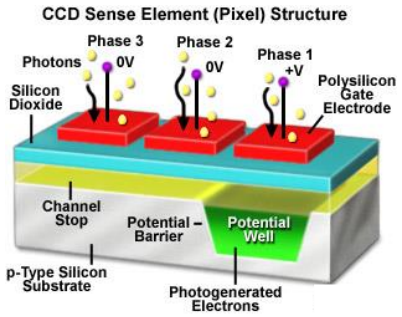
Poisson's Equation



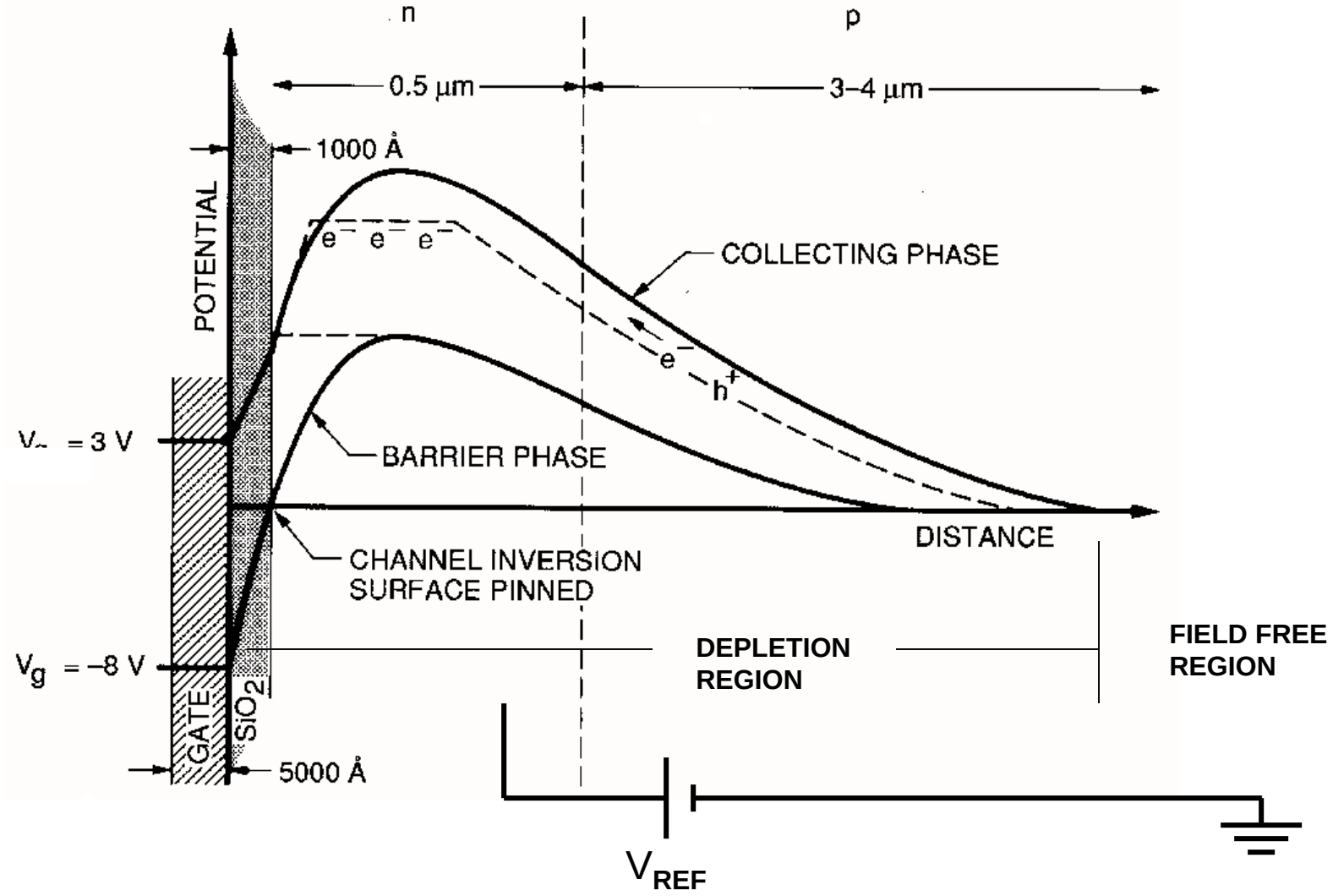
CCD STRUCTURE



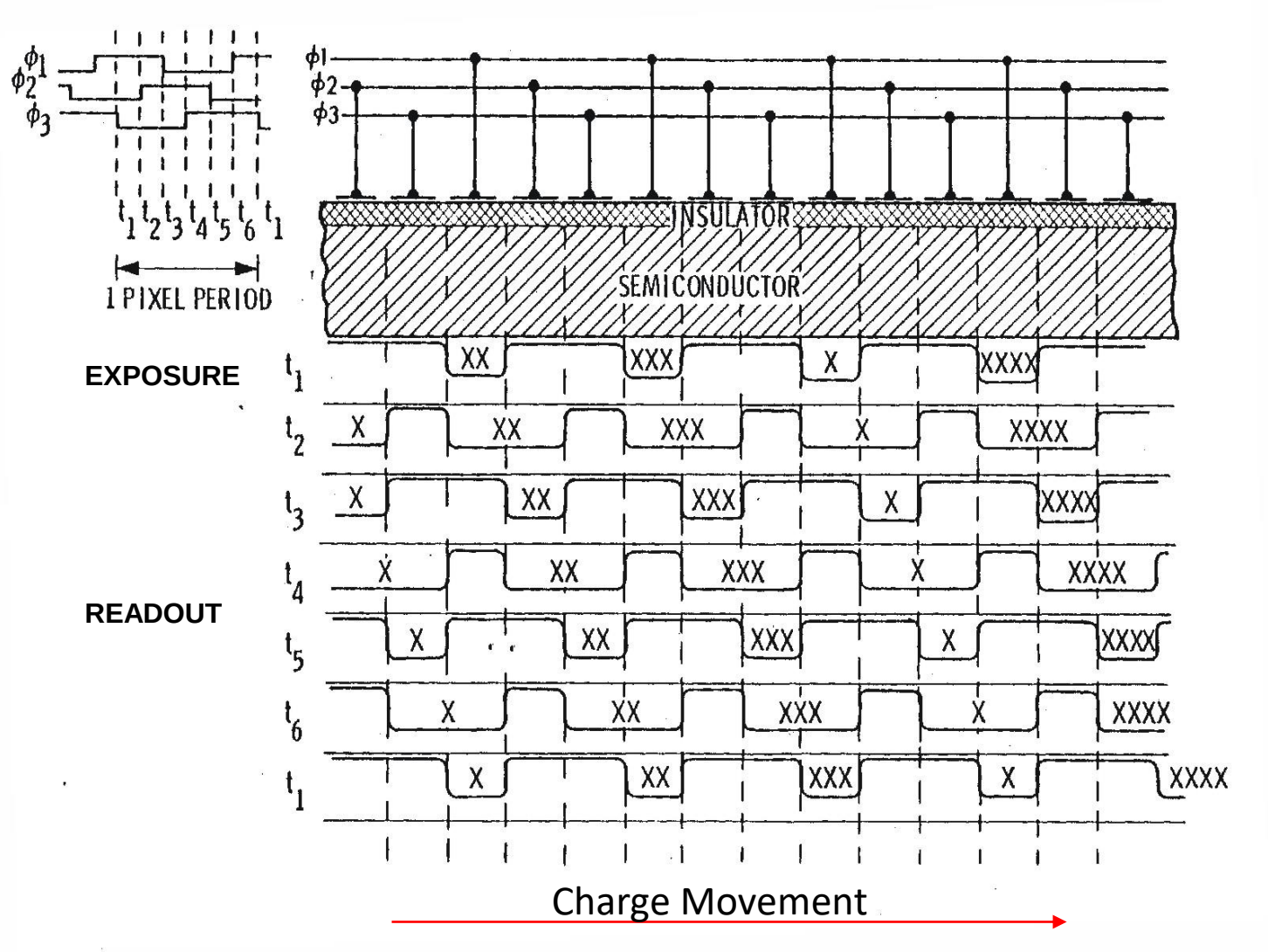
POTENTIAL WELL

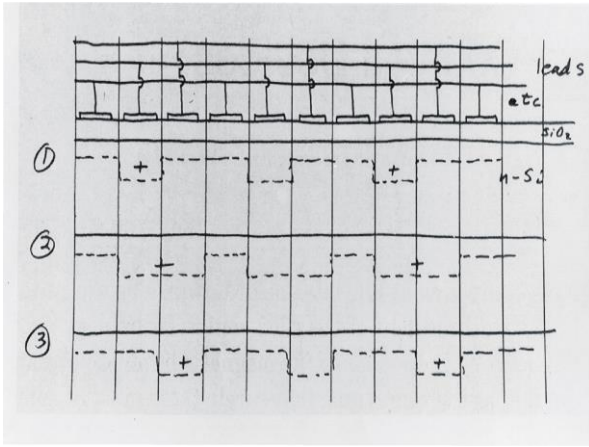


Charge movement



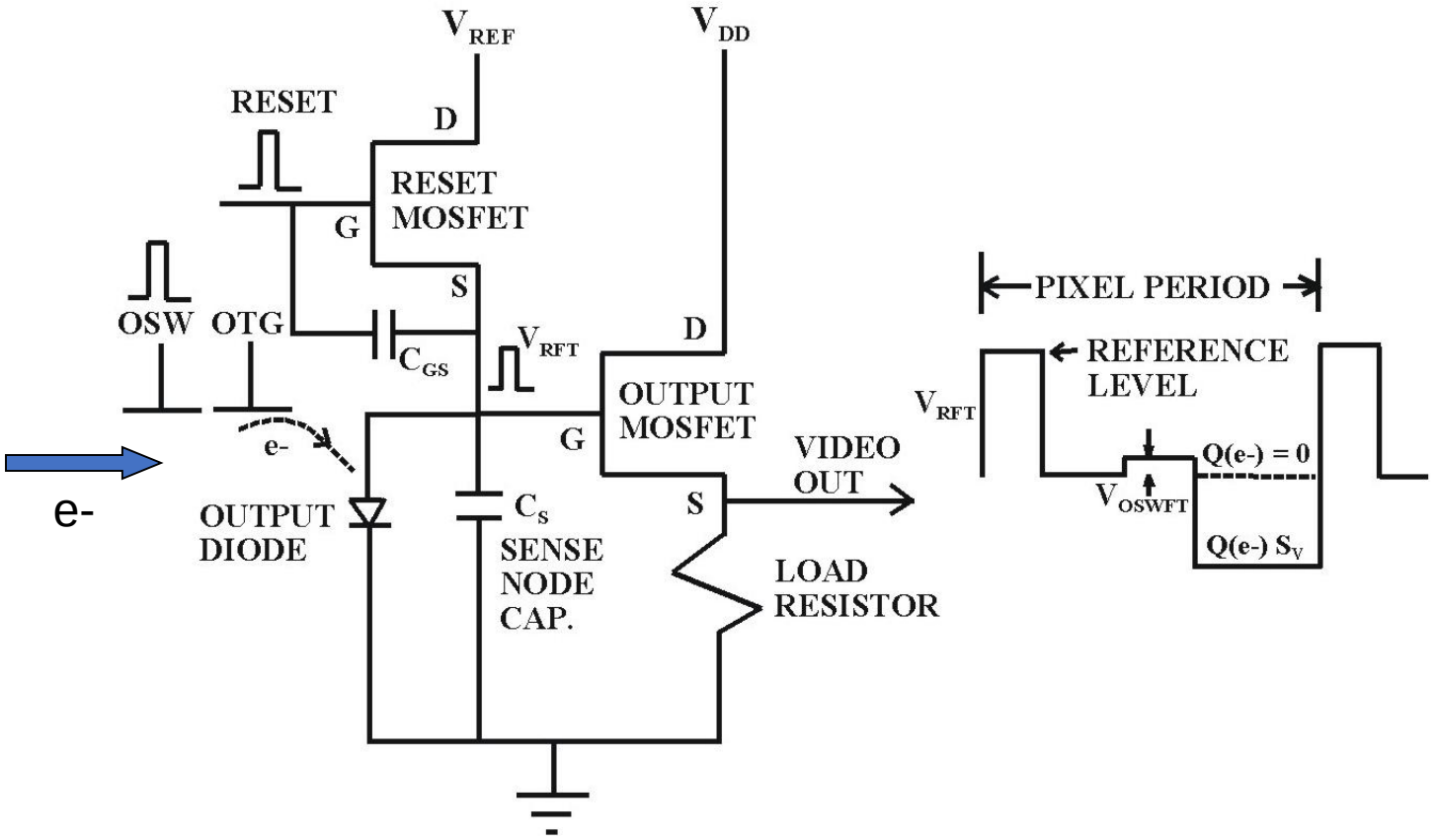
CHARGE TRANSFER





Boyle & Smith's 1969 notebook entry

CCD READOUT CIRCUIT



CHARGE DETECTION

V = charge/ capacitance = q/C (from electrostatics)
(Coulomb/Farad = Volt)

Video-out =

q (electron charge) * #e- / NodeCapacitance

1.6 x 10^{-19} S(e^-) / node capacitance(F) (Volts)

e.g.,

Signal = 1 e^-

Capacitance = 10^{-14} F

Video-out = 16 micro-volts

CCD Architectural Types

FULL FRAME (PROGRESSIVE SCAN)

- **HIGH PERFORMANCE SCIENTIFIC CCD PIXELS**
- **MAXIMUM PIXEL AREA FOR GIVEN PIXEL PITCH**
- **REQUIRES SHUTTER OR PULSED LIGHT SOURCE**
- **DIFFICULT FOR VIDEO**

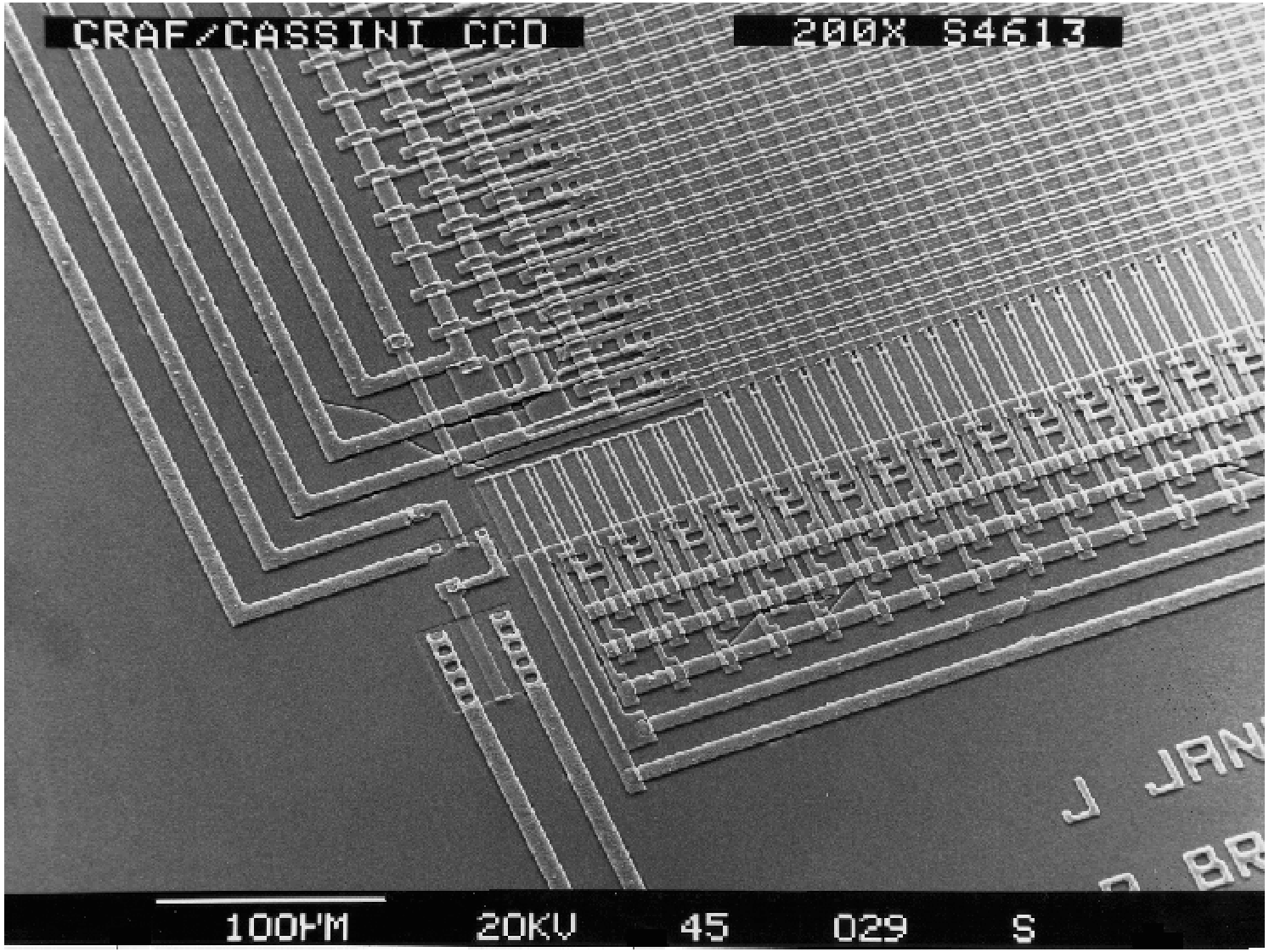
FRAME TRANSFER

- **COMMERCIAL CCD PIXELS**
- **ELECTRONIC SHUTTERING**
- **NO PIXEL FILL FACTOR LOSS**
- **IMAGE SMEAR**
- **RARELY EMPLOYED TODAY**
- **~2X DIE SIZE VS FULL FRAME**

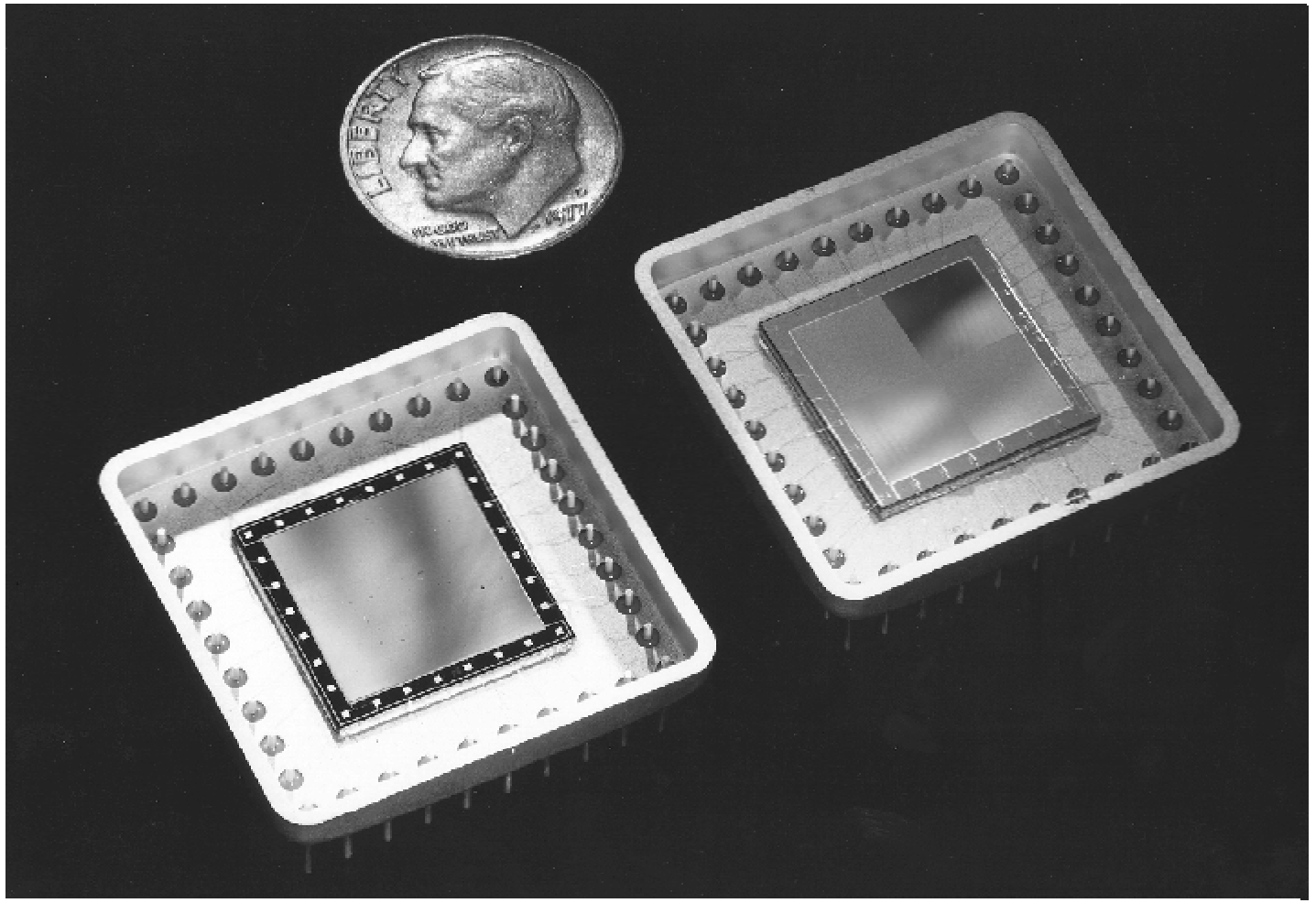
INTERLINE TRANSFER

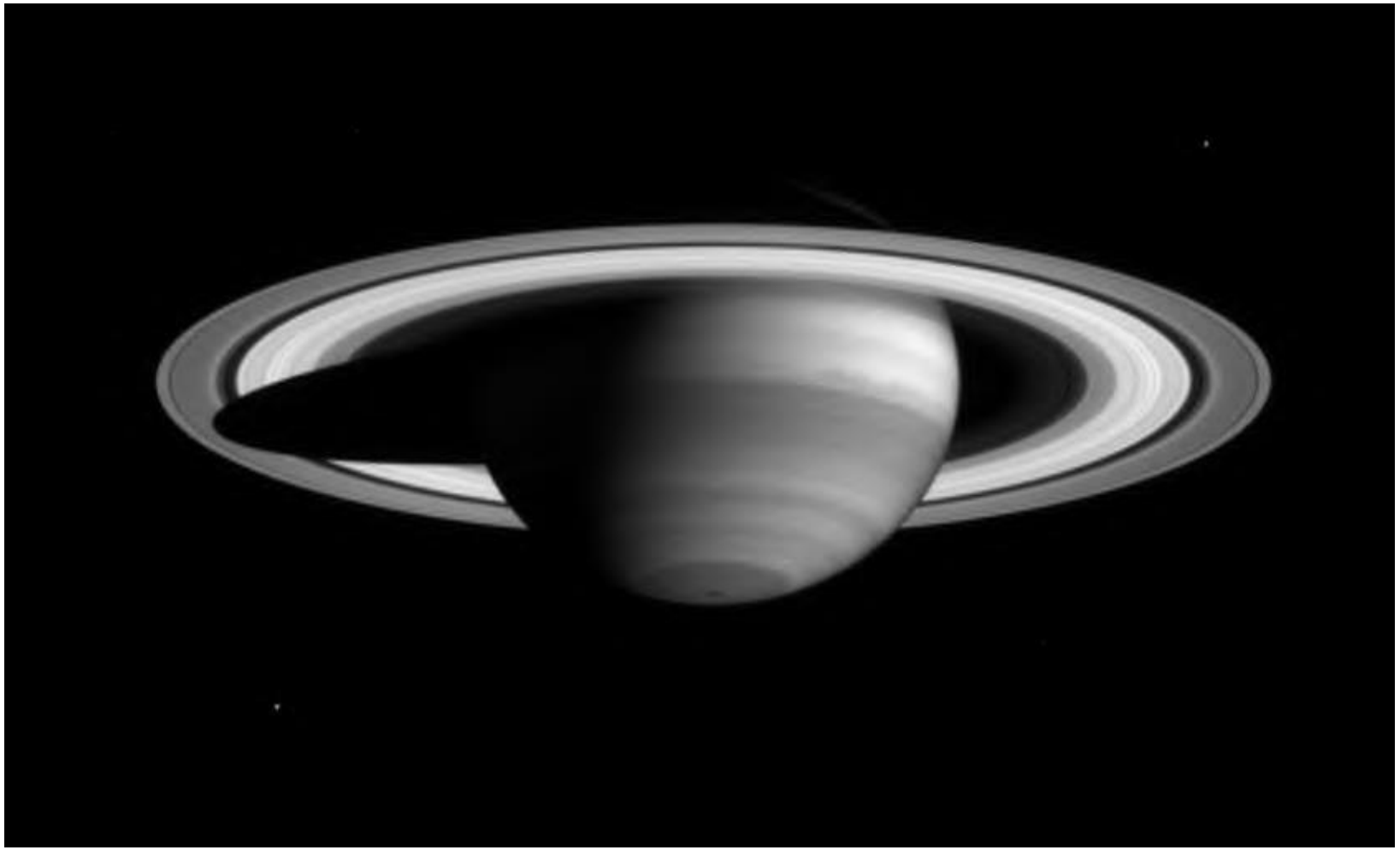
- **COMMERCIAL CCD PIXELS**
- **ELECTRONIC GLOBAL SNAP SHUTTER: USEFUL FOR VIDEO/NO IMAGE SMEAR**
- **ABOUT HALF OF PIXEL IS OPTICALLY DEAD (FILL FACTOR ~50%)**
- **PIXEL FILL FACTOR LOSS ALLEVIATED BY MICRO LENS**
- **KEY TECHNOLOGY FOR MACHINE VISION/AUTOMATION**

CASSINI 1024 X 1024 IMAGER



CASSINI IMAGERS



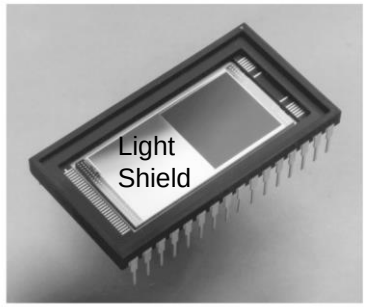


PLANET SATURN

FRAME TRANSFER
(ELECTRONIC SHUTTER)

Pros:
Shutterless video CCD
High fill factor
Cons:
Image Smear
Die size = Cost

CCD47-20 Back Illuminated
AIMO Frame-Transfer
High Performance CCD Sensor



TYPICAL PERFORMANCE

Maximum readout frequency	5 MHz
Output amplifier responsivity	4.5 µV/e⁻
Peak signal	100 ke⁻/pixel
Dynamic range (at 20 kHz)	~50,000:1
Spectral range	200 – 1100 nm
Readout noise (at 20 kHz)	2 e⁻ rms

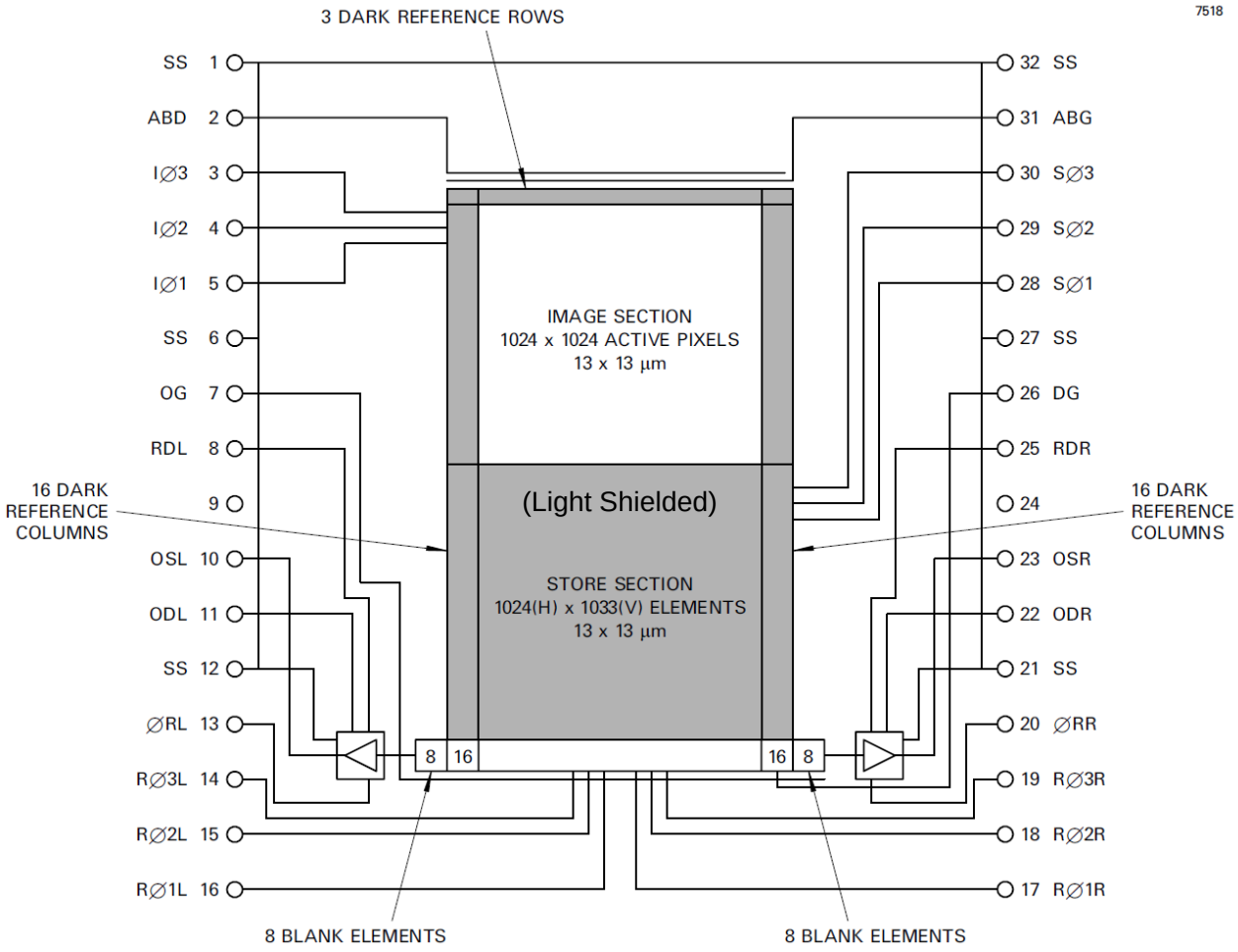
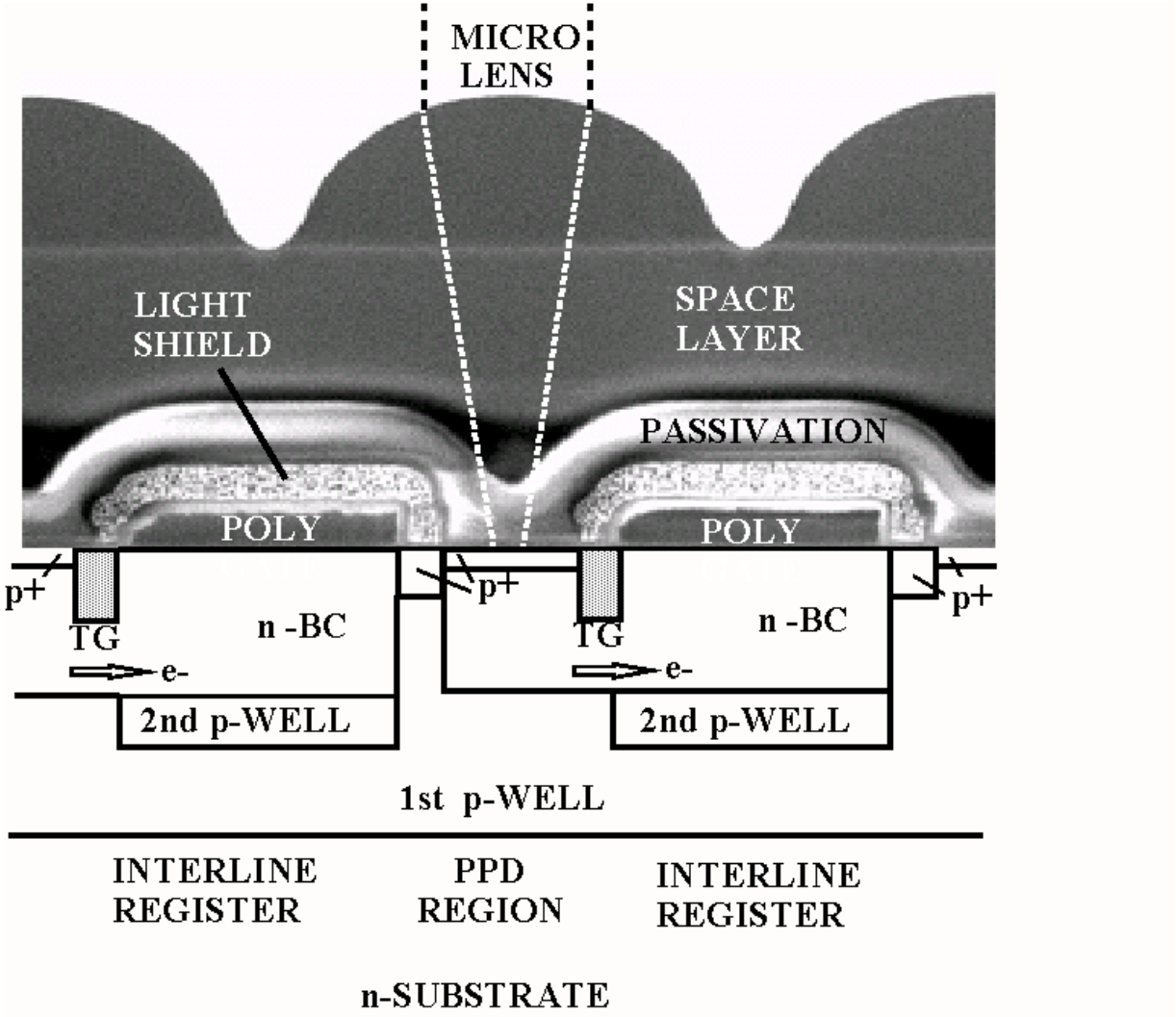
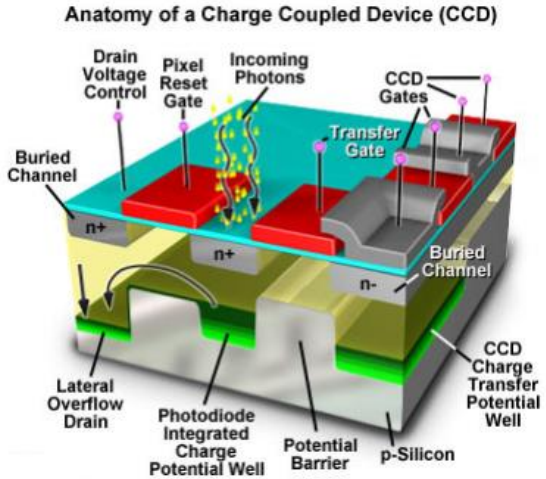


IMAGE SMEAR
(Frame Transfer CCD)

INTERLINE TRANSFER
(ELECTRONIC SHUTTER)





CCD IMAGERS

Qualities

- **Text book performance for all parameters (QE, read noise, MTF, dark current, linearity, etc.).**

Deficiencies

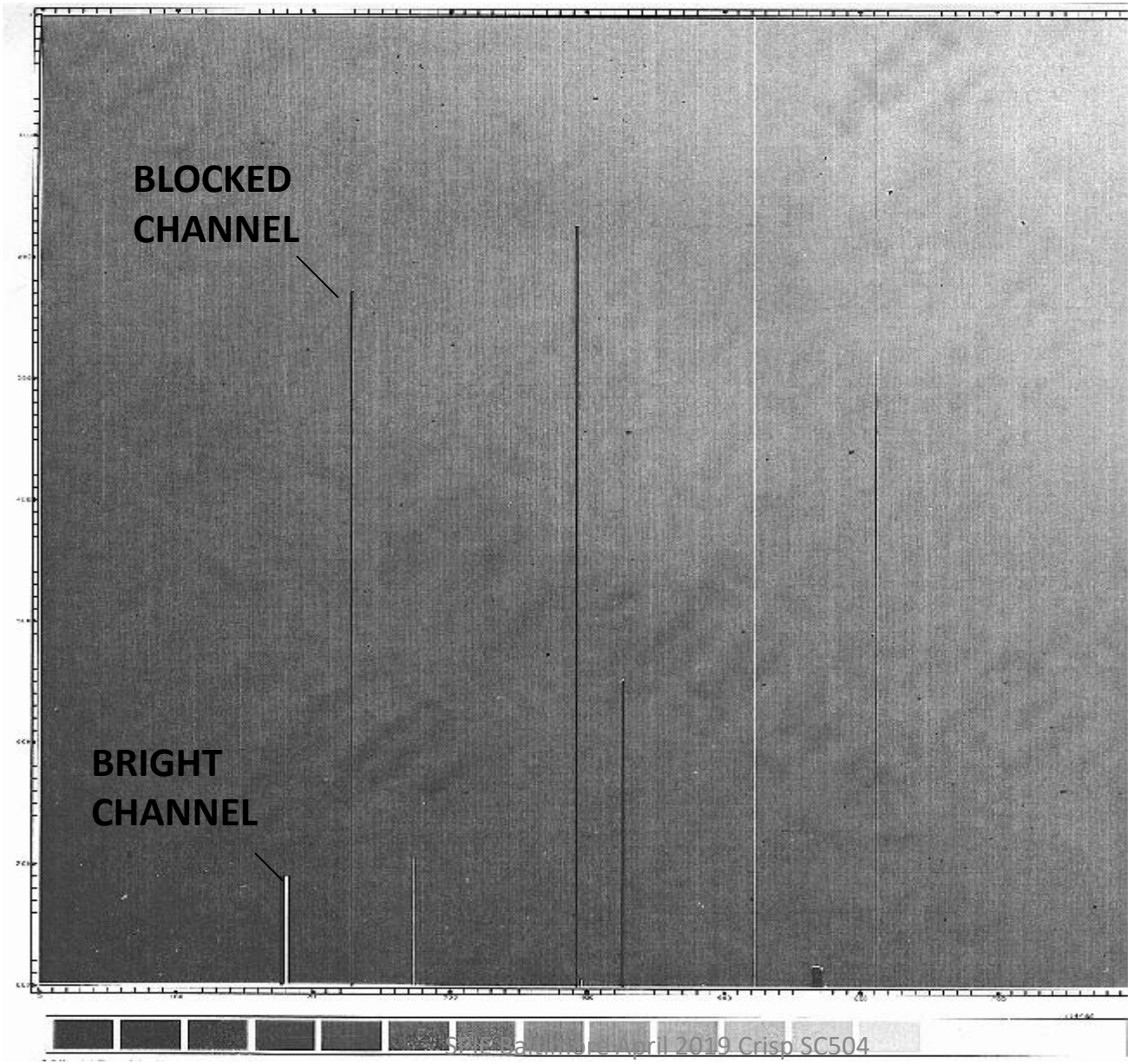
- **Low tolerance for high-energy radiation damage.**

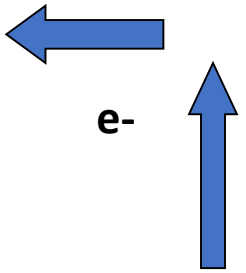
  e.g. proton bulk damage and resultant CTE degradation.

- **Significant off-chip electronic support required.**

- **Difficulty with high-speed readout (inherently a serial read out device).**

COSMETICS





CMOS BASICS
(building on CCD fundamentals)

CMOS IMAGERS

Merits

- **Very tolerant to high-energy radiation sources (long life time)**

  Any charge transfer degradation applies only to one transfer in array vs thousands for serial readout CCD

- **On- chip system integration (low power, low weight and compact designs).**

  Easy to build CDS, A/D & other support circuitry on-chip with both N&P type MOSFETS available

- **High speed / low noise operation (inherently a parallel- random access readout device).**

  Each column can have its own signal processing & A/D conversion circuitry with digital outputs. Limited only by power and pincount (and ability to store data)

Deficiencies

- **Historically lacked performance in most areas compared to the CCD (charge generation, charge collection, charge transfer and charge measurement).**

  Much improvement has been realized in recent years. Some remaining challenges arising from V/e- nonlinearity in flat fielding area

- **Wafer processing typically is more expensive and uses many more lithography steps. On the other hand typically is fabricated on modern 300mm wafers with many more die per wafer vs large CCDs fabricated on small wafers (due to lithography limitations)**

CMOS IMAGER TYPES

PROGRESSIVE SCAN

- **CHARGE TRANSFER CMOS PIXELS**
- **IMAGE MOTION SMEAR**
- **REQUIRES SHUTTER OR PULSED LIGHT SOURCE**
- **READ NOISE LIMITED BY PIXEL SOURCE FOLLOWER AMPLIFIER**
- **NO SENSE NODE BLOOMING AND SMEAR**

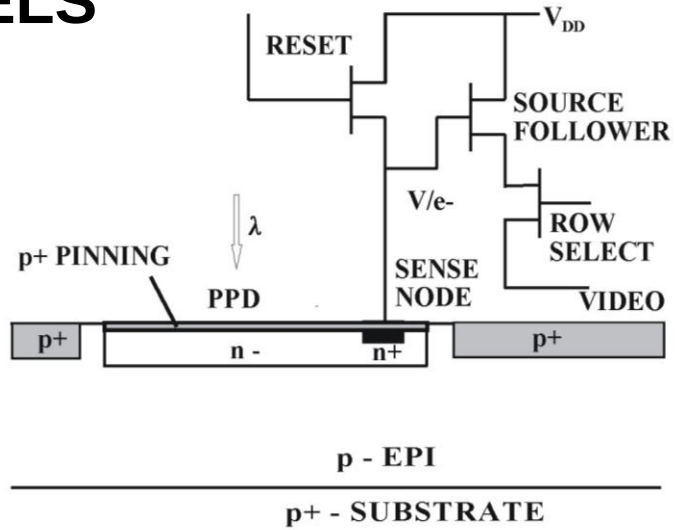
ROLLING SHUTTER

- **3T PHOTO DIODE PIXELS**
- **ELECTRONIC SHUTTERING**
- **IMAGE MOTION SMEAR**
- **RESET NOISE LIMITED (UNLESS ACTIVE RESET IS EMPLOYED)**

SNAP

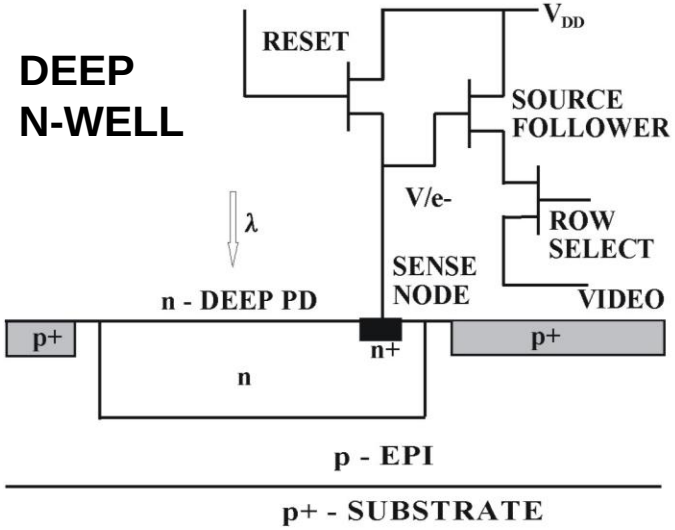
- **CHARGE TRANSFER CMOS PIXELS**
- **ELECTRONIC SHUTTERING**
- **NO IMAGE MOTION SMEAR**
- **RESET NOISE LIMITED (TRUE CDS CANNOT BE PERFORMED)**
- **SENSE NODE BLOOMING AND SMEAR**

Example CMOS PIXELS

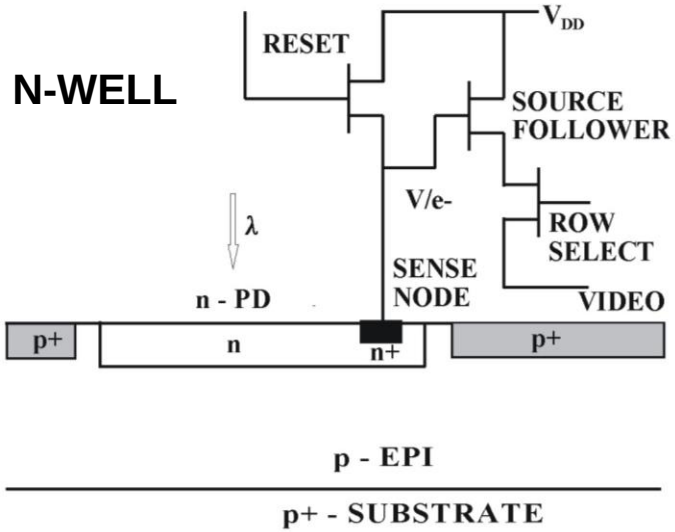


PINNED PHOTO DIODE

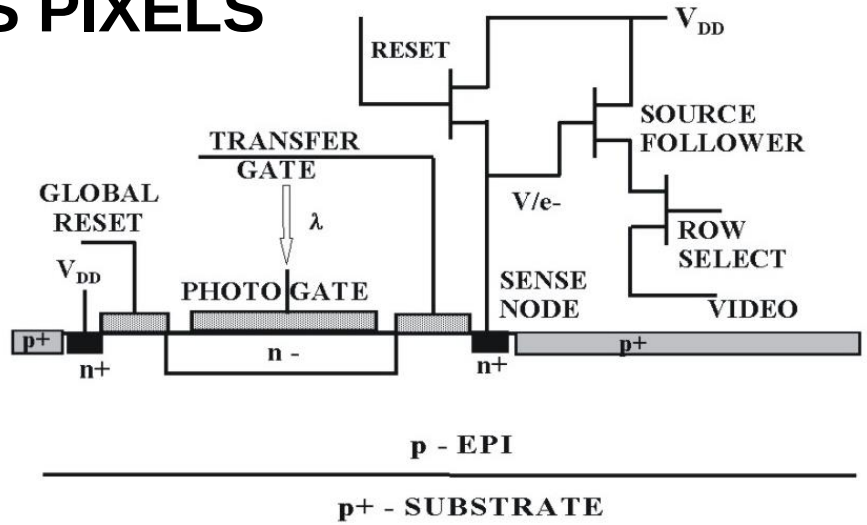
DEEP N-WELL



N-WELL



Example CMOS PIXELS



6T
PHOTO GATE

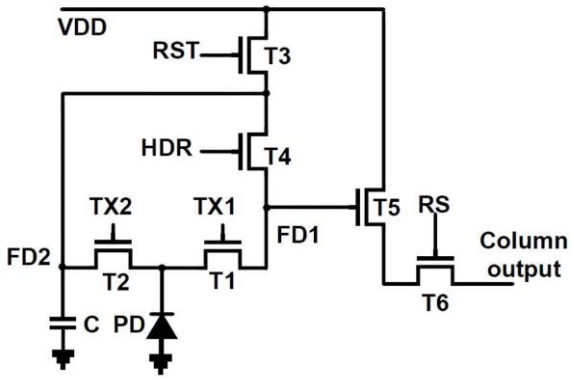
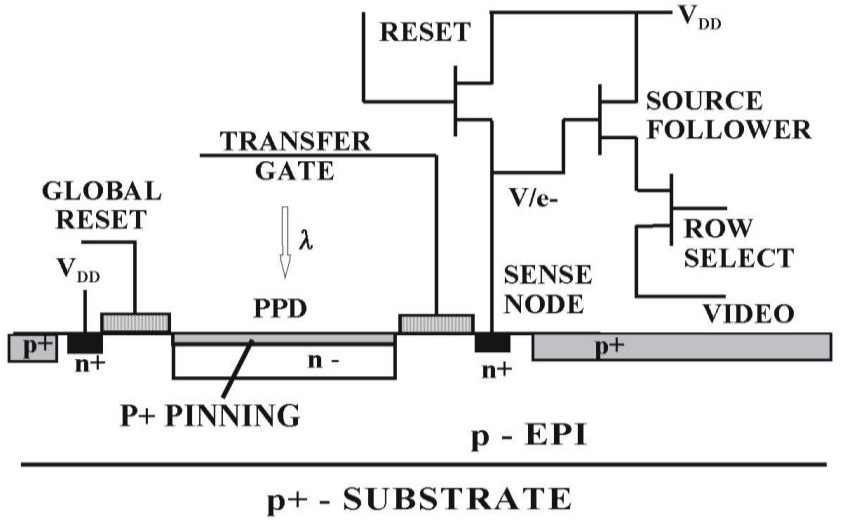


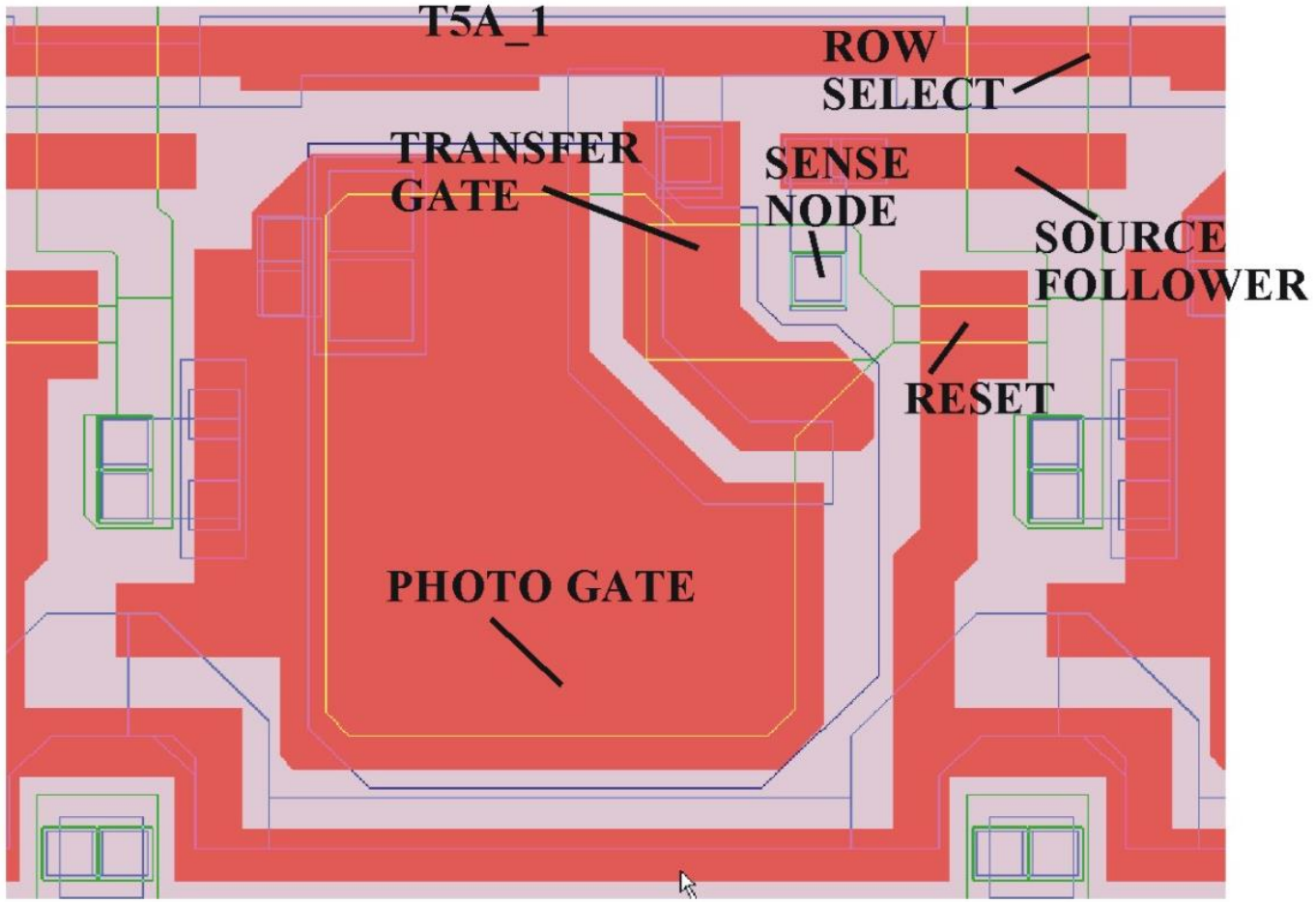
Fig. 3.6 dual-transfer-gates HDR image sensor structure [3.5]

6T High Dynamic Range

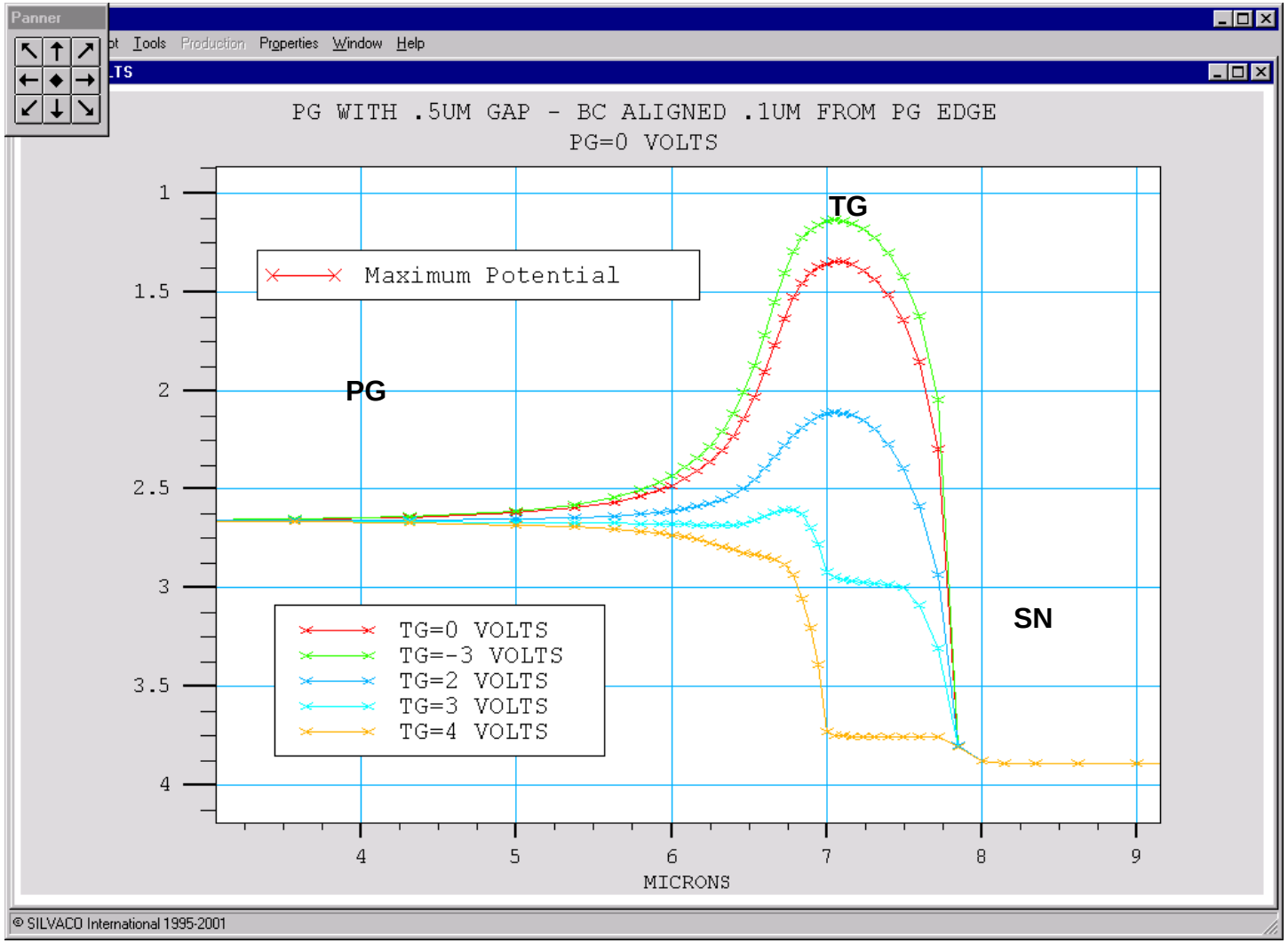


5T
PINNED
PHOTO
DIODE

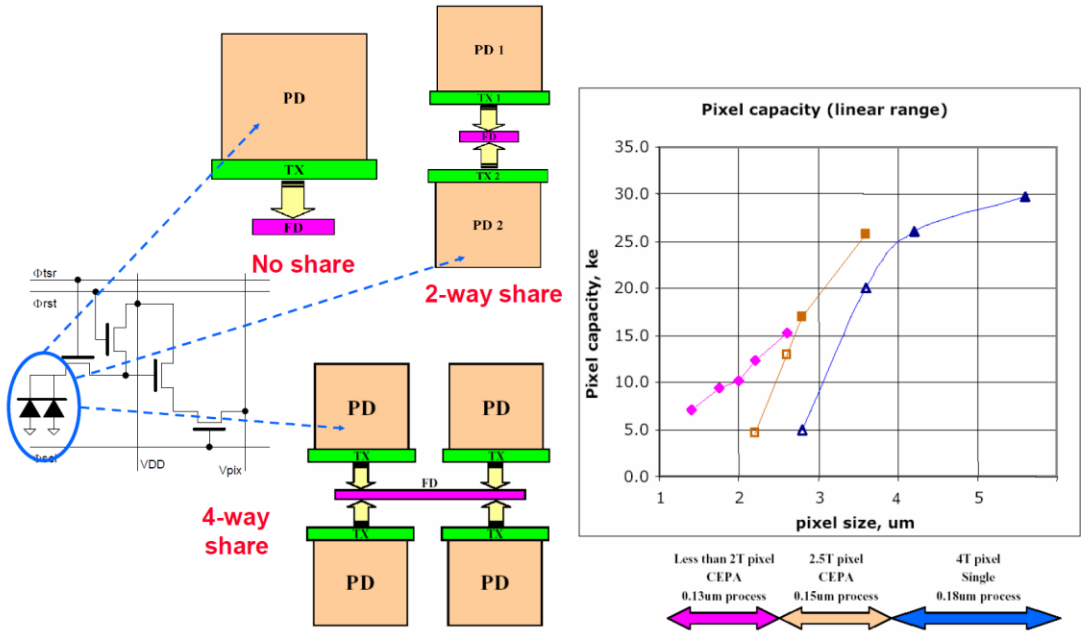
CMOS Photogate Pixel



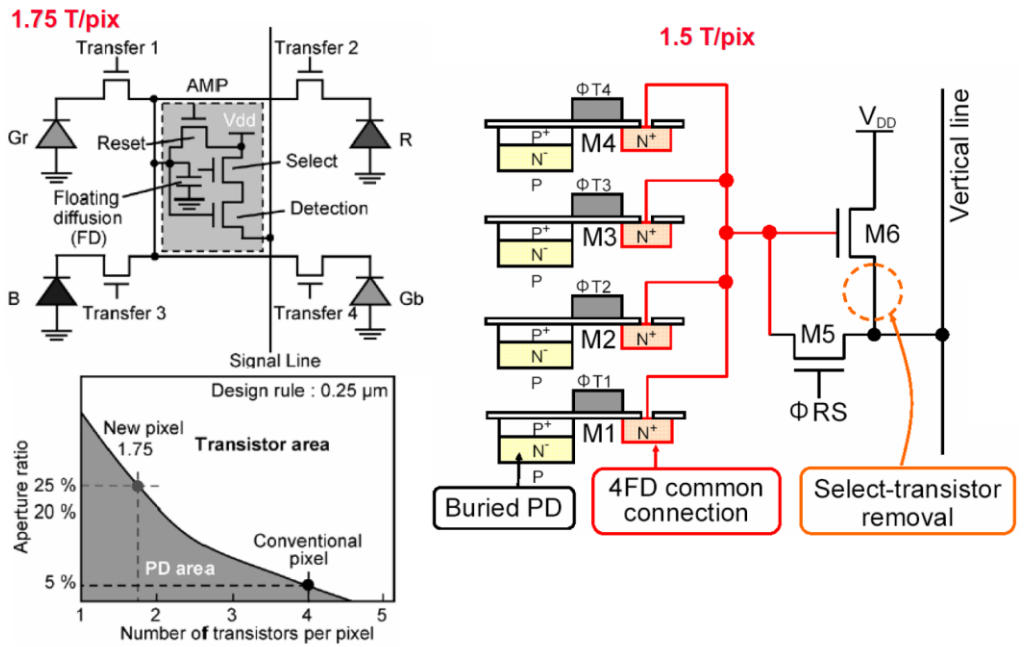
CMOS PHOTO GATE PIXEL



SHARED PIXELS



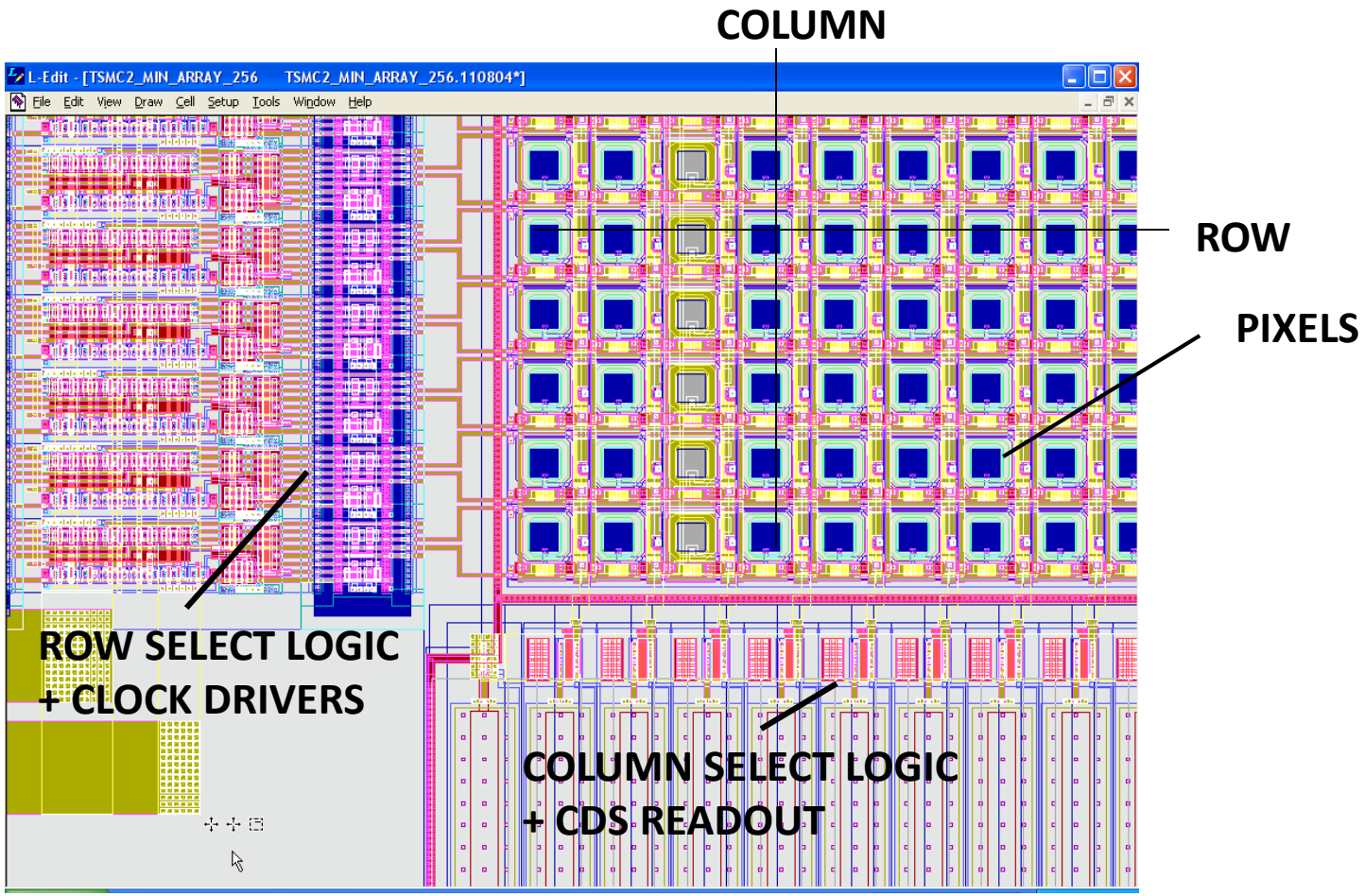
FURTHER REDUCTION IN FET COUNT



Amortize the readout circuitry over more than one pixel to improve Fill Factor, QE and to support on-chip summation of multiple pixels

CMOS PIXEL READOUT
(PARALLEL RANDOM ACCESS READOUT)

The pixel array is accessed using a row and column address as if it were a memory IC



ULTRA LOW NOISE (2 e-) READ MODES

3T PPD DCDS PROGRESSIVE SCAN READ OUT

- Sample the first row of pixels, encode and save (all other rows integrate signal charge).
- Reset that same row and immediately sample the reset levels, encode and save.
- Progressively read and sample the next row of pixels in the same fashion.
- Repeat until all rows of the imager are read out.
- Subtract video and reset levels with computer to eliminate reset noise.
- Repeat frame readout.

- VARIATIONS
  - -Integrate before readout
  - -Rolling shutter readout

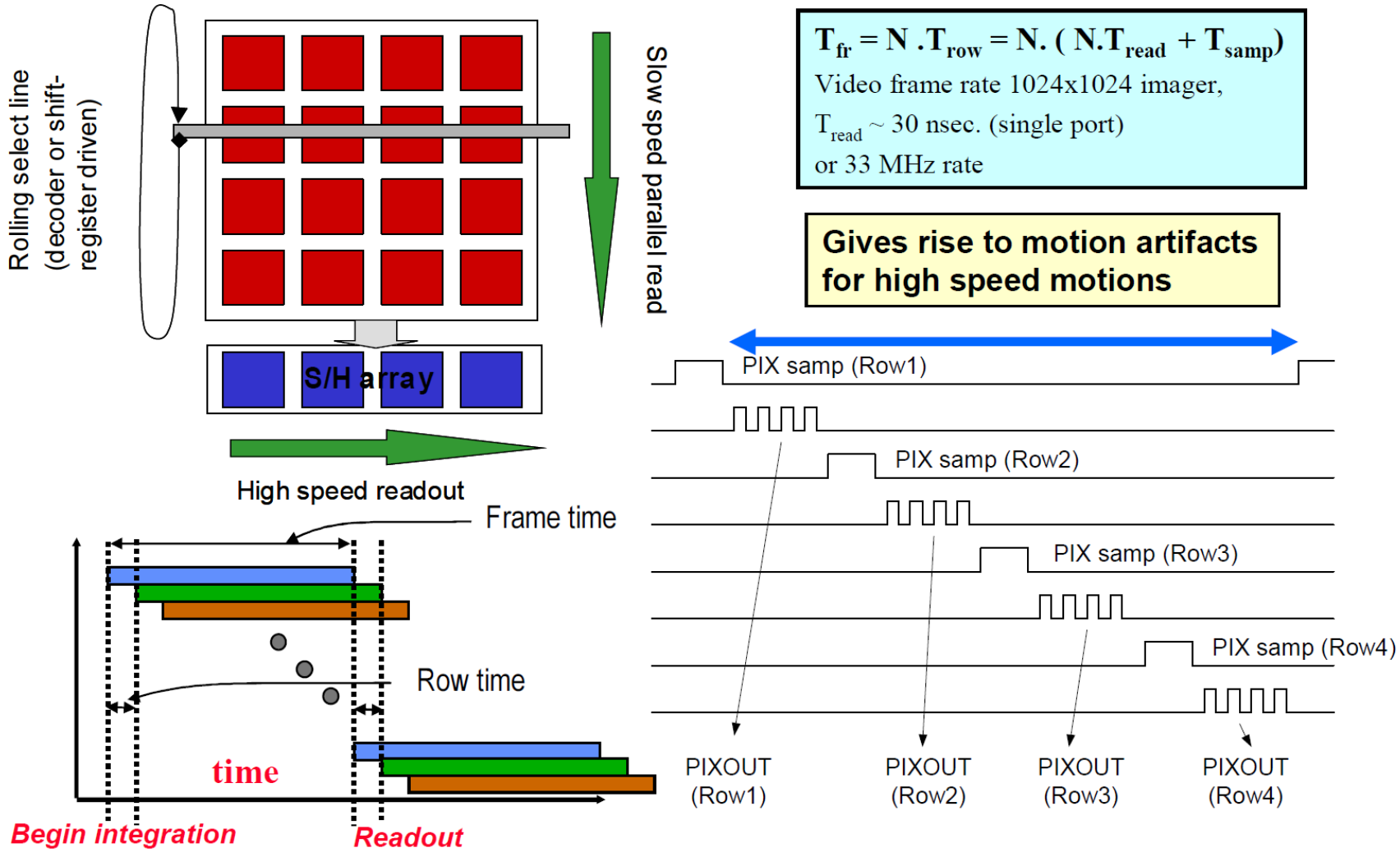
4T PPD DCDS SNAP READ OUT

- SNAP video to sense node for all pixels (all rows integrate charge during readout).
- Sample the first row of pixels, encode and save.
- Reset that same row and immediately sample the reset levels, encode and save.
- Progressively read and sample the next row of pixels in the same fashion.
- Repeat until all rows of the imager are read out.
- Subtract video and reset levels with computer to eliminate reset noise.
- Repeat frame readout.

VARIATIONS

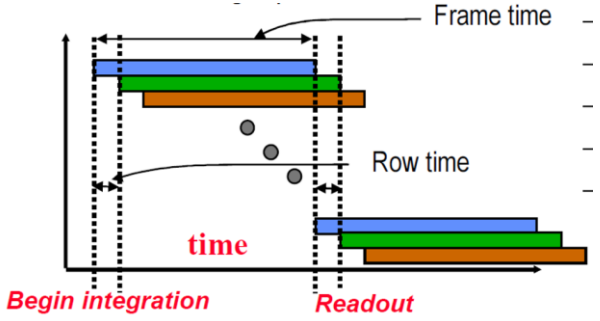
- -Integrate before readout

Rolling Shutter Operation



MOTION SMEAR
(ROLLING SHUTTER)

Each scanline (row) of image is sampled at a different time leading to motion smear

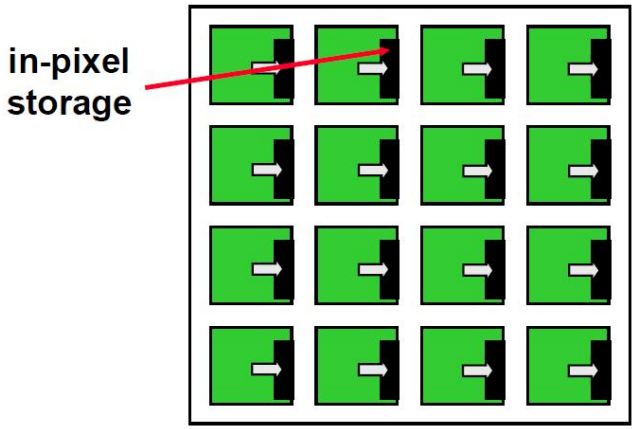


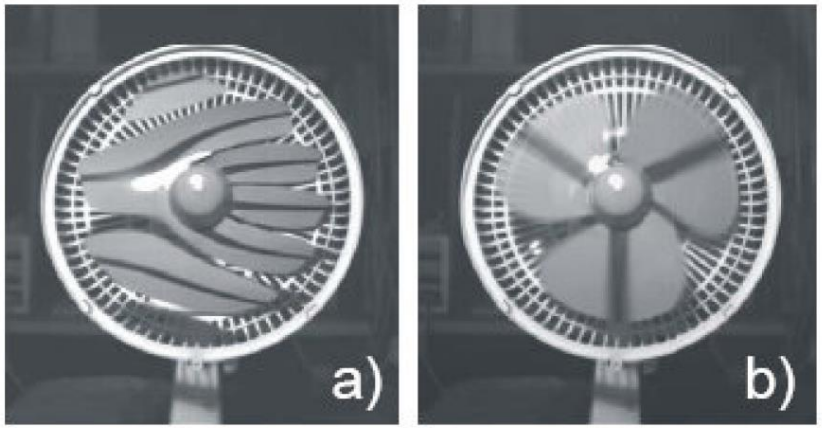
Global Snap Shutter

SNAP-SHOT MODE
- Single simultaneous in-pixel Xfer
- Pixel-at-a-time readout
- Min. intg. time ~ 1 msec.
- Motion artifact minimized
- No reduction in anti-blooming

PIXEL TYPES:
- Photogate w/sense node as in-pixel buffer
- Photodiode w/charge sharing
- Pinned-photodiode

All of them require **an extra gate** for anti-blooming and short exposure time definition *(FIT-CCD with no smear)*





Rolling Shutter Snap Shutter

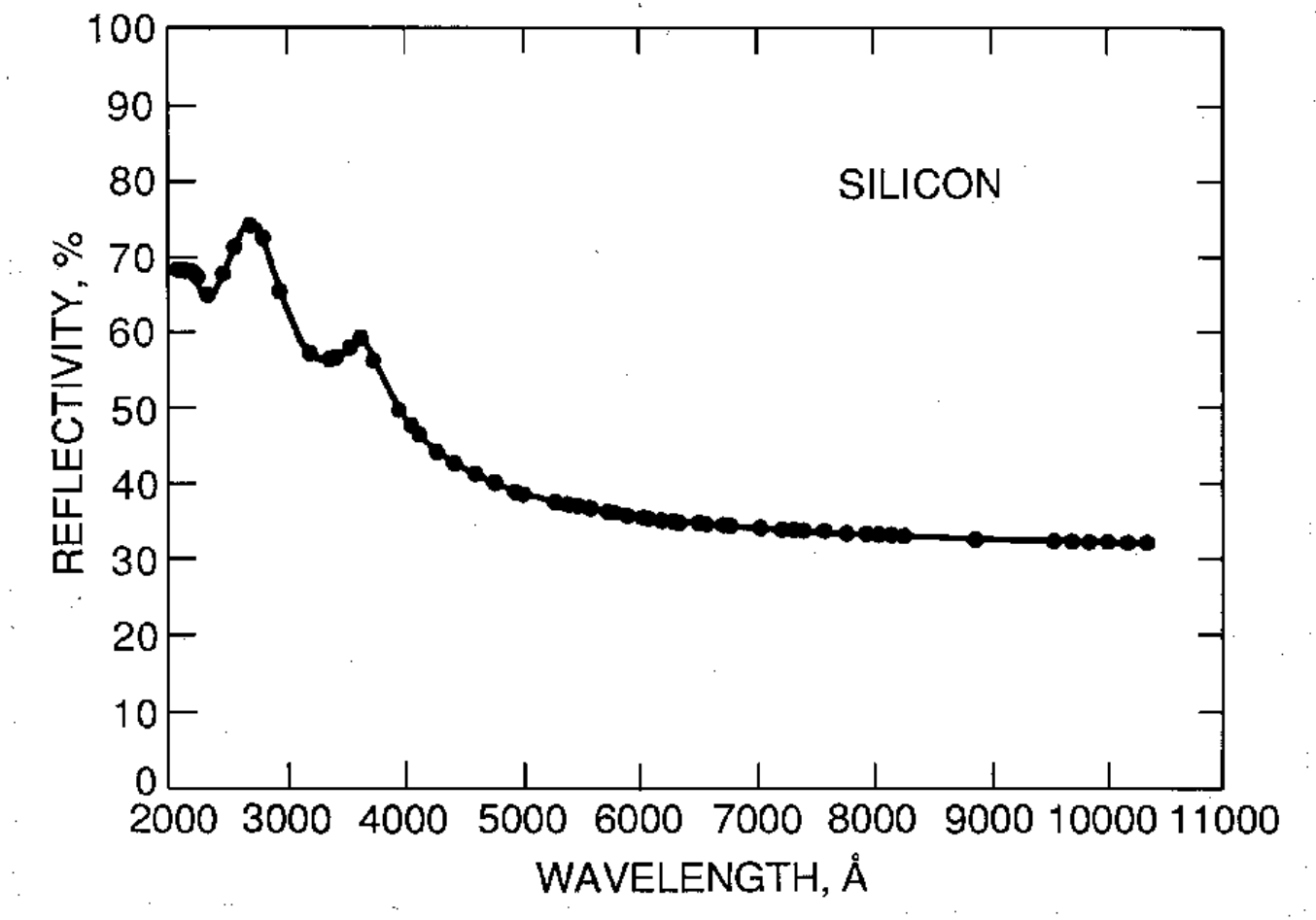
Part 3

CHARGE GENERATION

CHARGE GENERATION

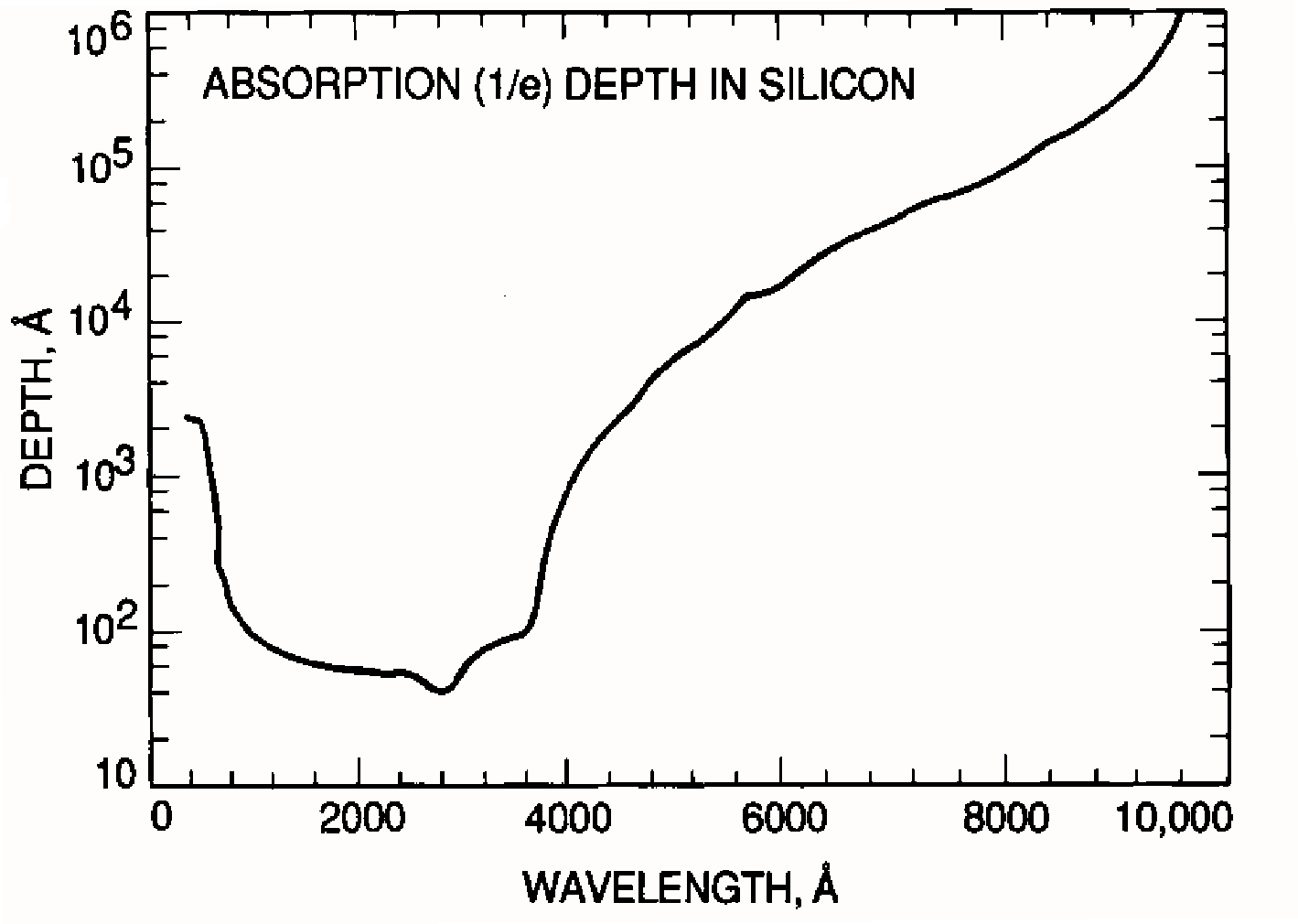
- **Silicon Interaction**
  - **Near IR (7000 - 10,000 A)**
  - **Visible (4000 - 7000 A)**
  - **UV (1000 - 4000 A)**
  - **EUV (100-1000 A)**
  - **Soft X-ray (1-100 A)**
- **Interacting QE is limited by the absorbing layers that bound the epitaxial layer.**
- **Critical wavelength = 2500 A**
  - **Absorbtion depth = 30 A**
  - **Reflectivity = 70 %**
- **Absorption depth @ 4000 A = 2000 A**

Reflectivity vs wavelength



How many photons make it into the silicon to interact?

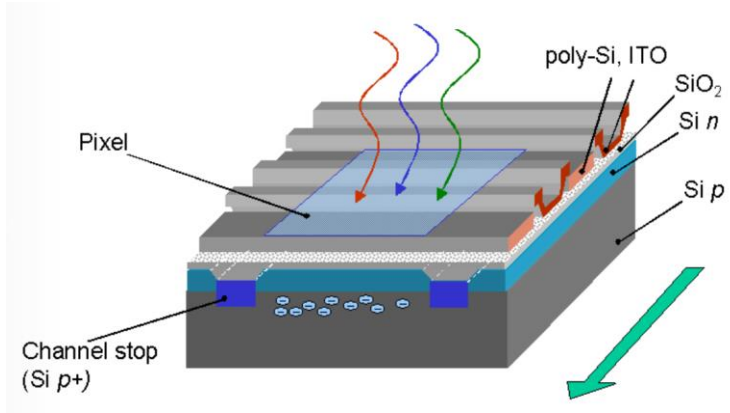
PHOTON ABSORPTION DEPTH

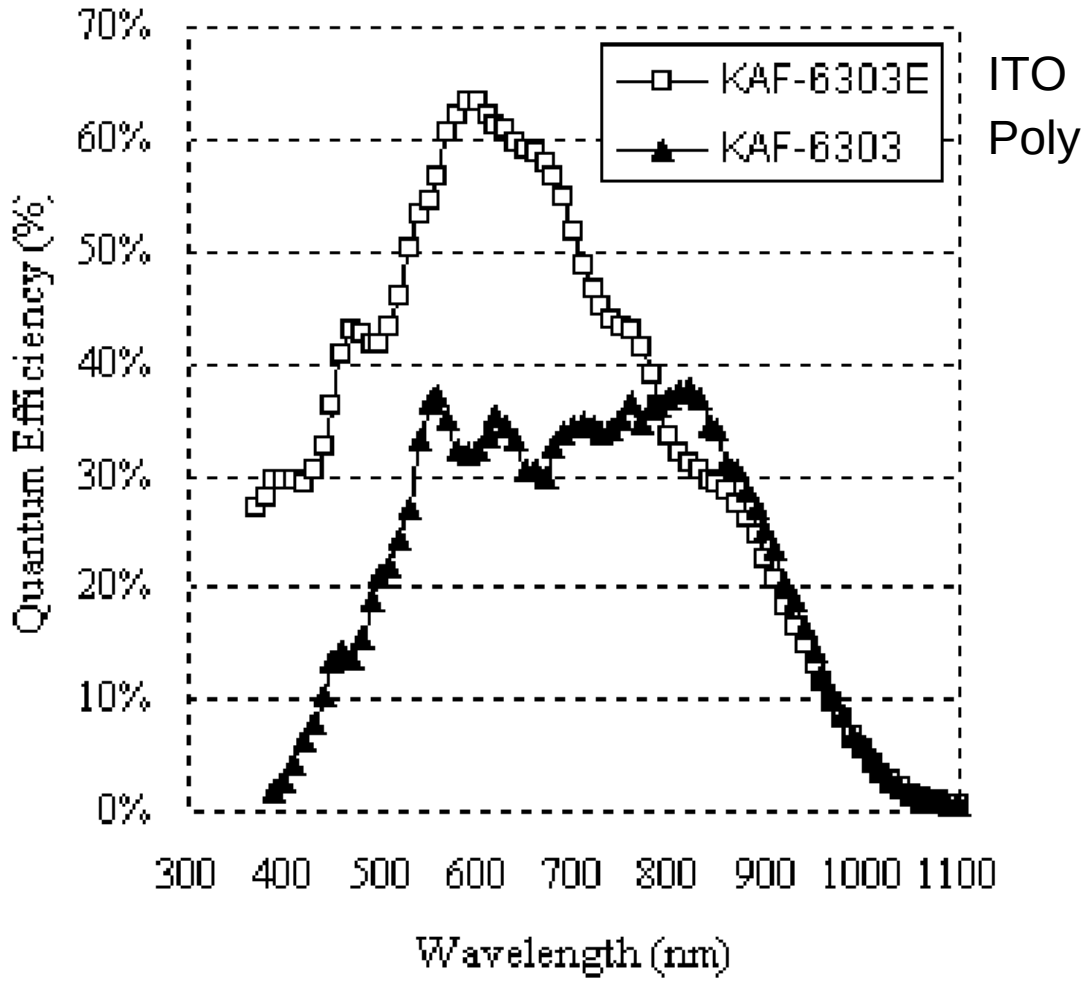


How deep do you make the depletion region for optimum spectral response?

QE Boosting: Indium Tin Oxide Transparent Gate

KODAK (now On-Semi)





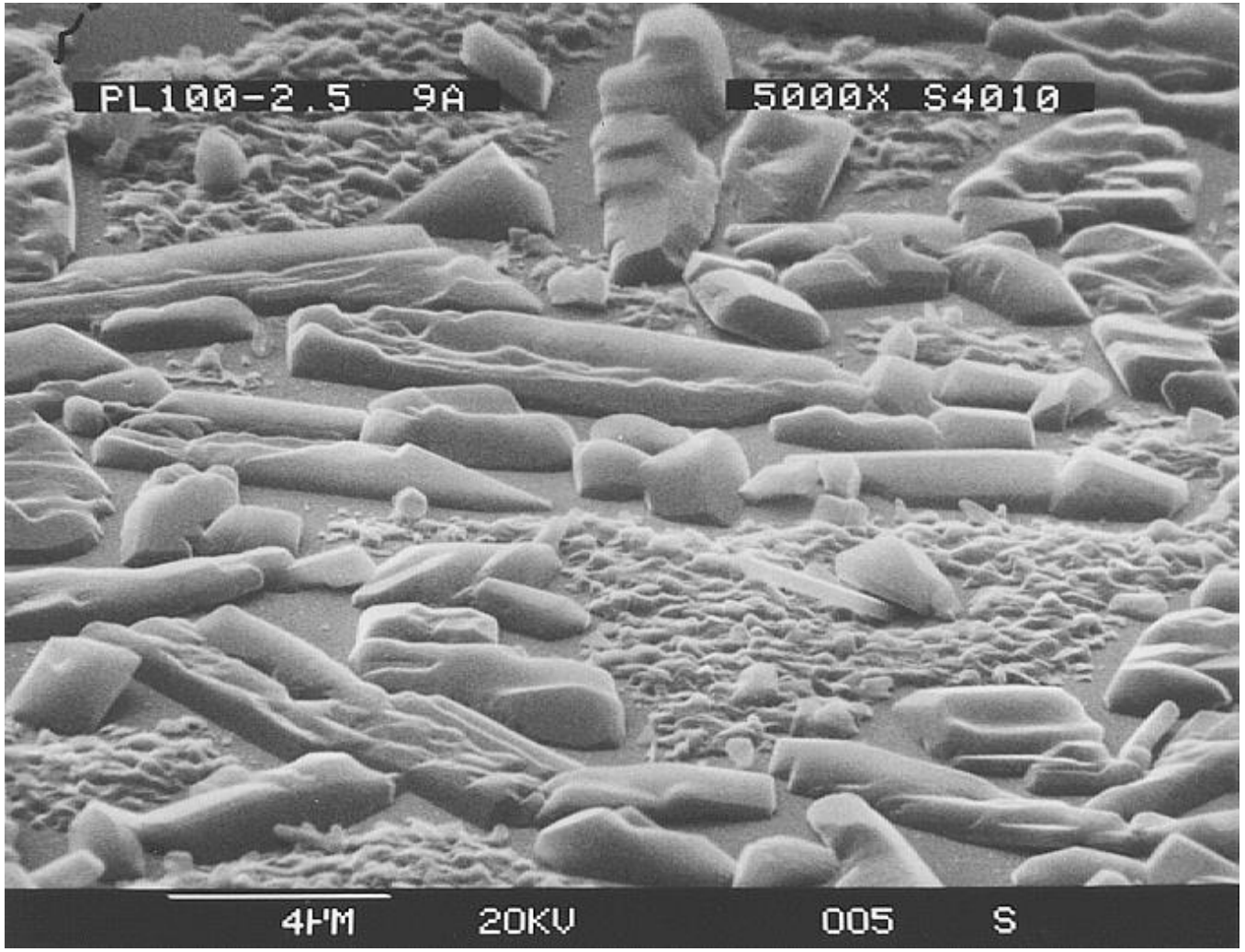
ITO

Poly

QE Boosting for UV/Near UV: Lumigen Coating

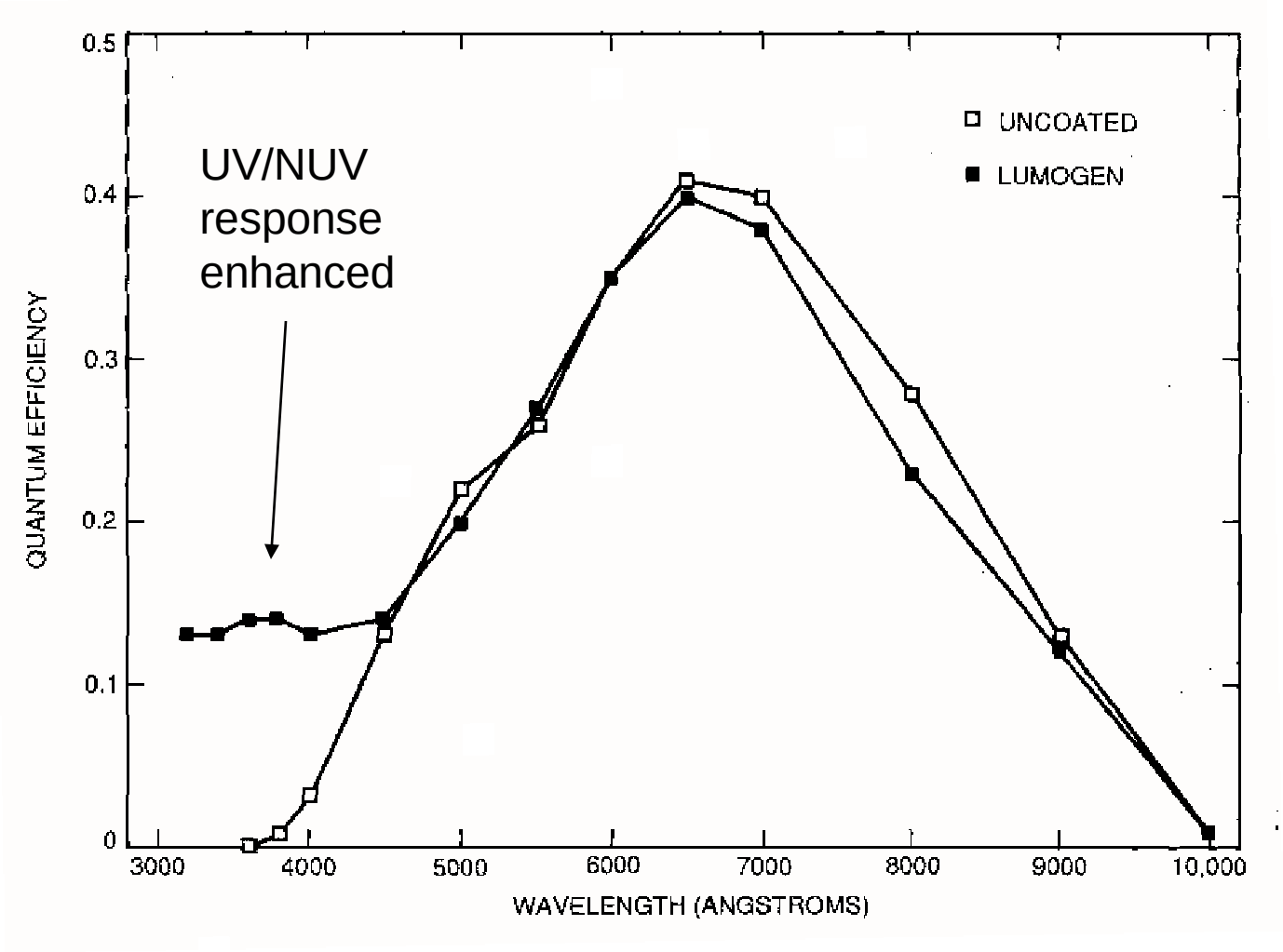
- **Organic Phosphors (e.g., Lumigen - Yellow -High Lighting Pen)**
- **Down Converts Photons Shortward of 4600 A to 5200 A**
- **100 % Quantum Yield**
- **Thermally Vacuum Deposited (6000 A) @ 70 C at 10^{-6} Torr**

Vacuum Deposited Lumigen Coating

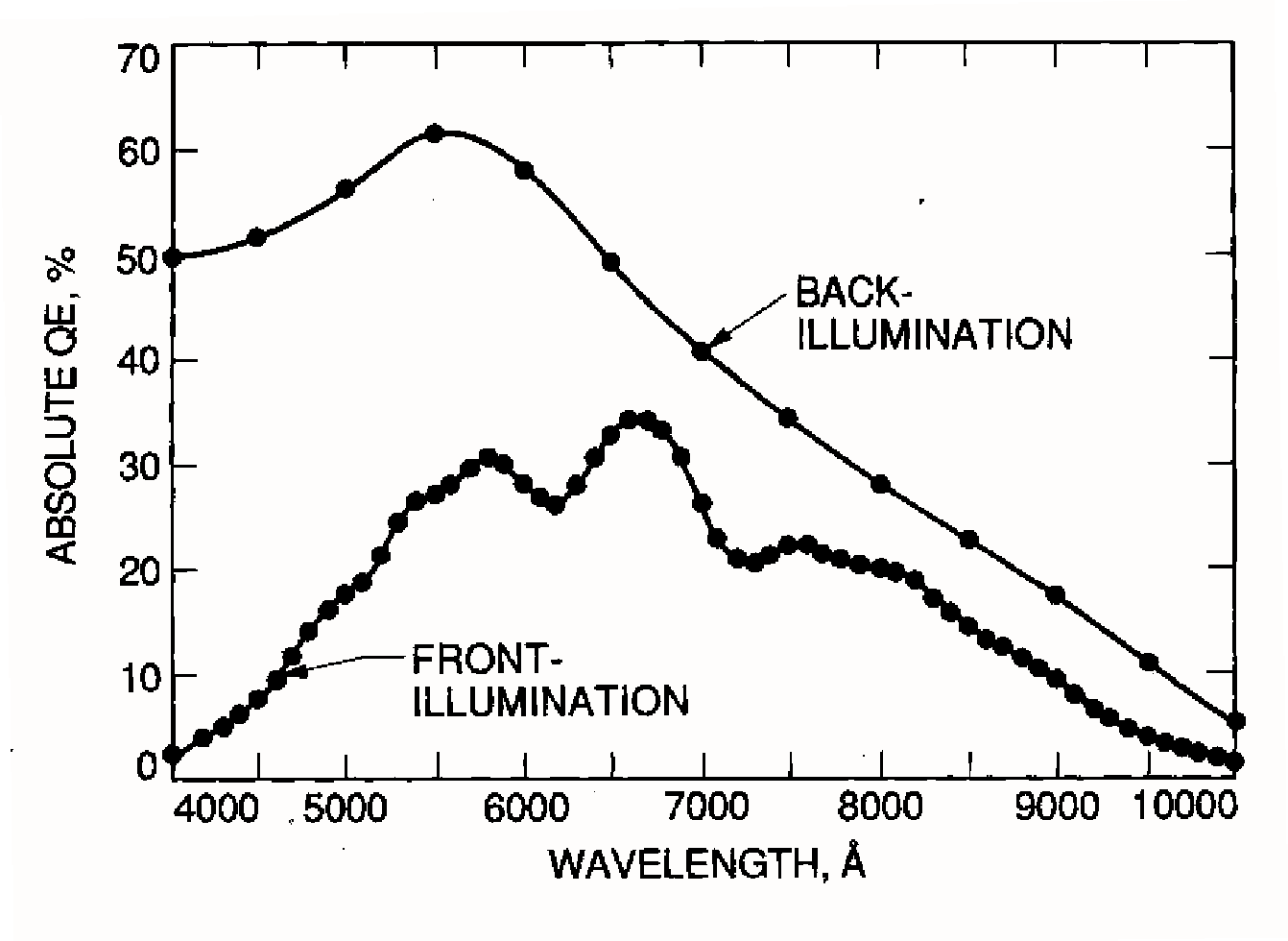


LUMIGEN QE TRANSFER

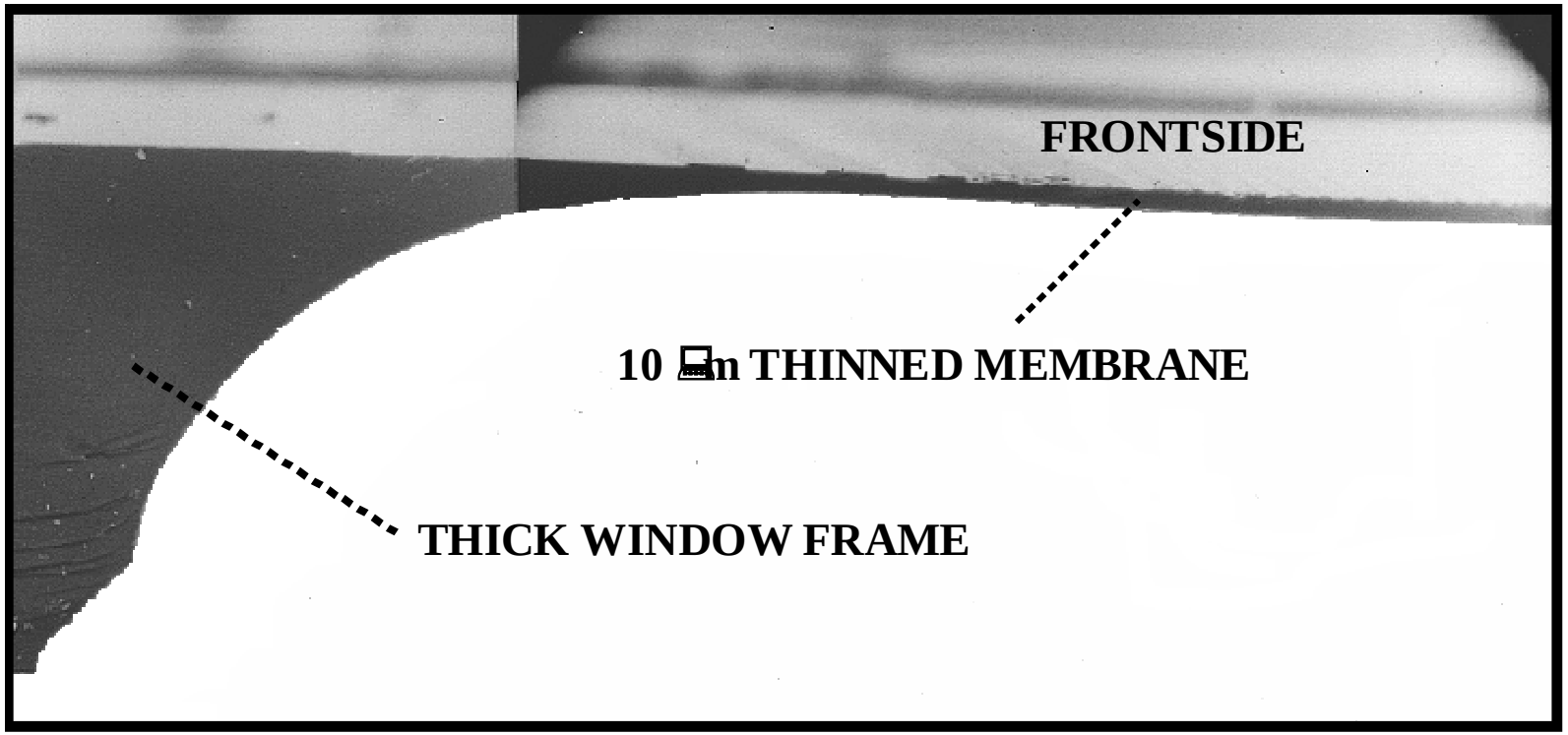
HUBBLE WF/PC II



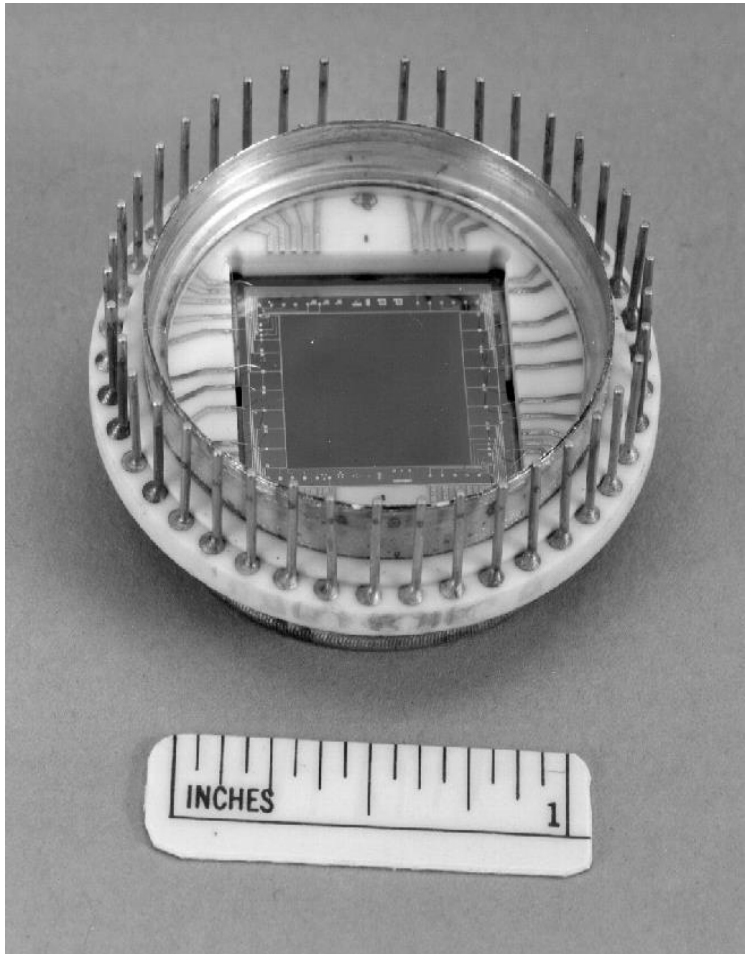
QE: FRONTSIDE vs BACKSIDE Illumination

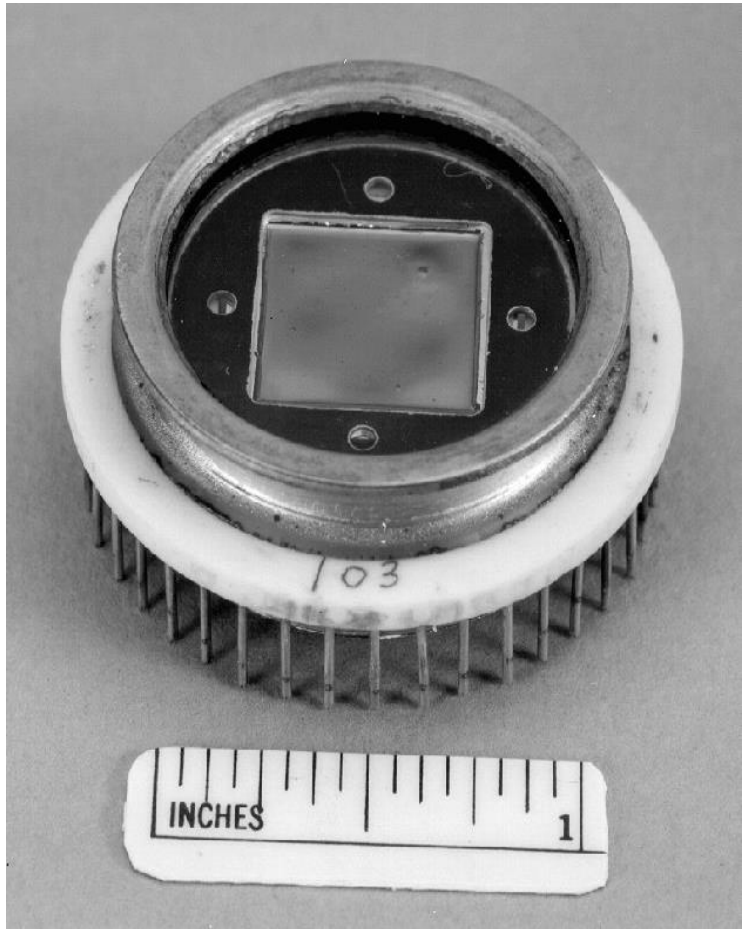


QE Boosting: Thinning for backside illumination

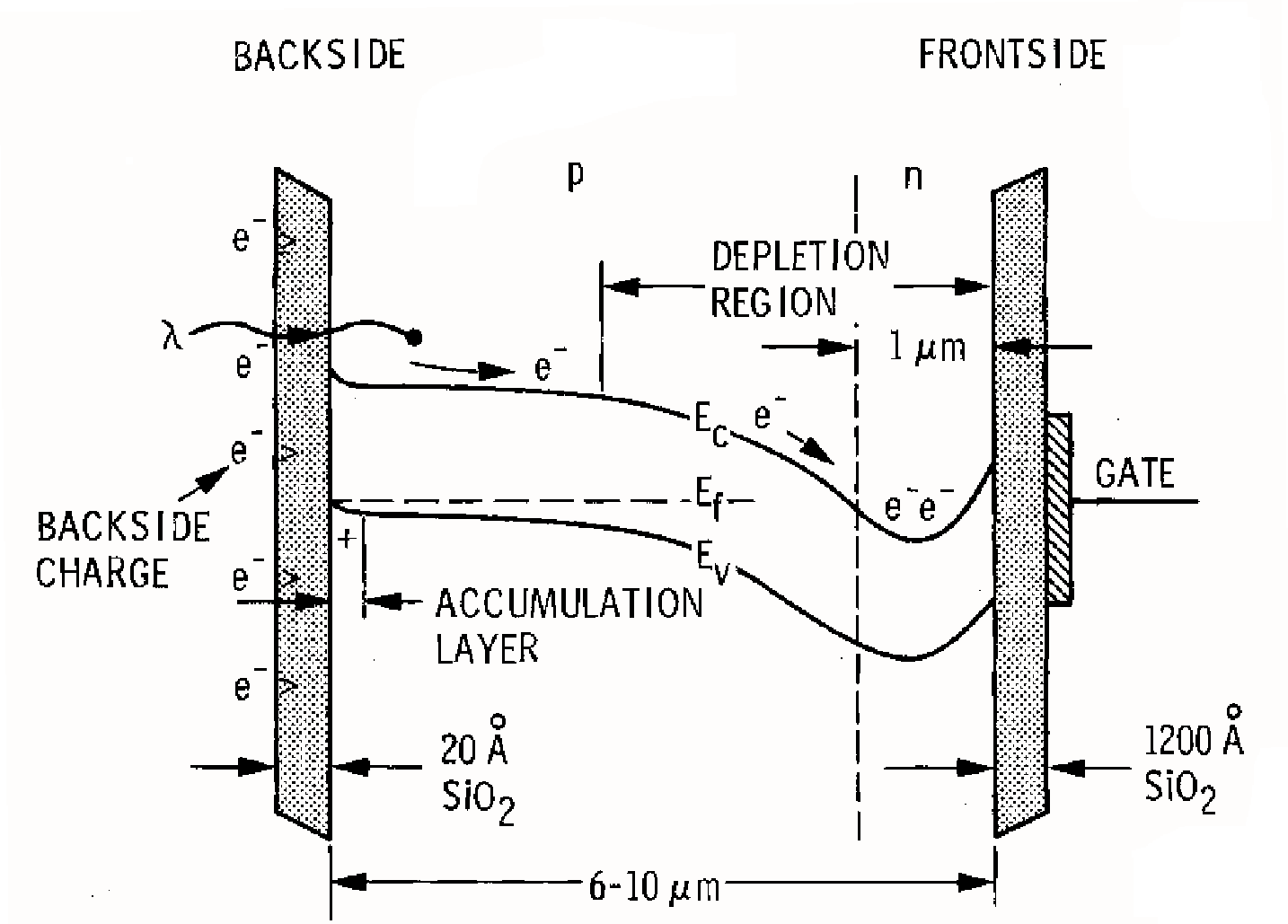


HUBBLE BACKSIDE ILLUMINATED CCD





QE Boosting: Accumulation layer for BSI



Need to avoid charge trapping at backside surface
Accumulation layer added to force electrons toward depletion region

Part 4

CHARGE COLLECTION

PIXEL PROBLEM AREAS

PIXEL INTEGRATION MTF

RELATED TO APERTURE SAMPLING

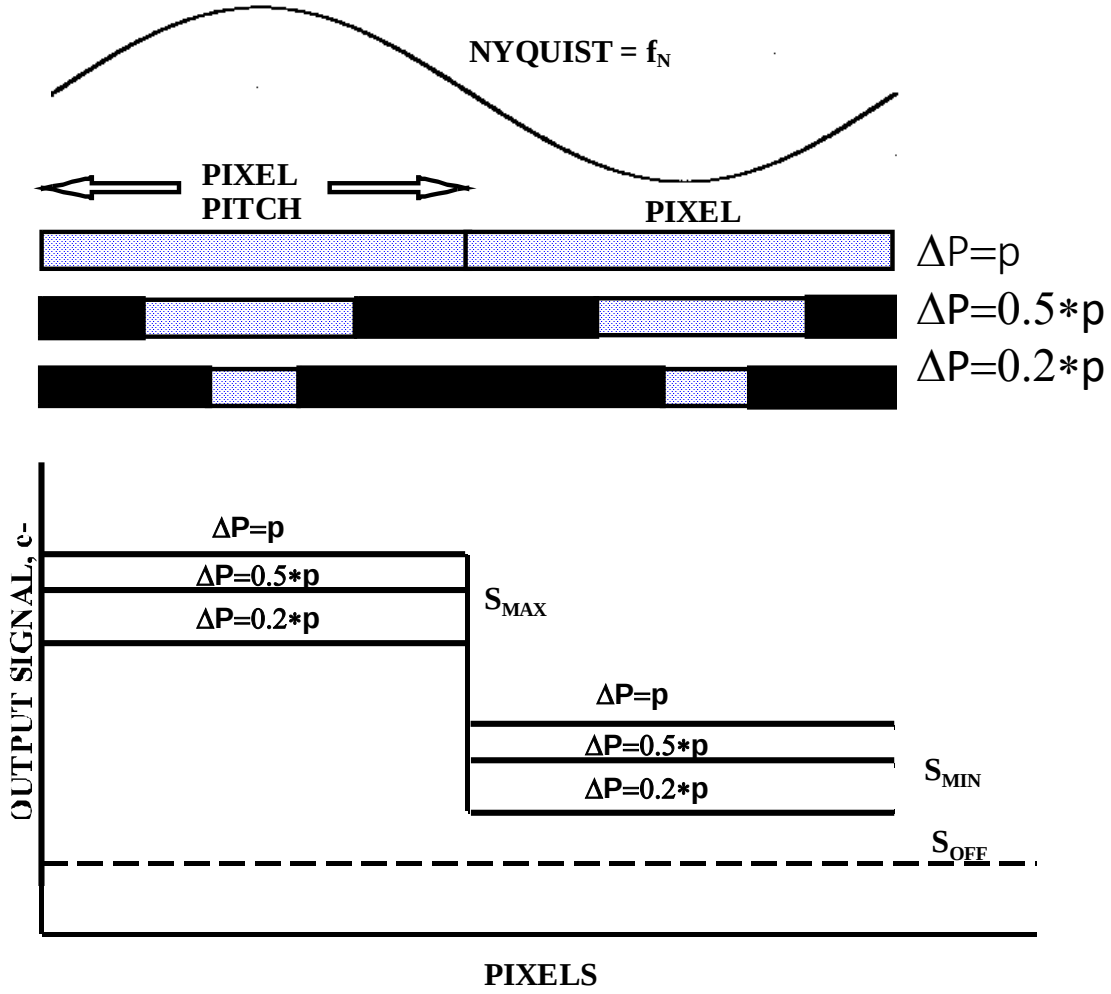
PIXEL DIFFUSION MTF

REGIONS IN THE PIXEL THAT ARE FIELD FREE

PIXEL CTE AND IMAGE LAG MTF

IMAGE SMEAR DUE TO INCOMPLETE TRANSFER OF CHARGE

MODULATION TRANSFER FUNCTION

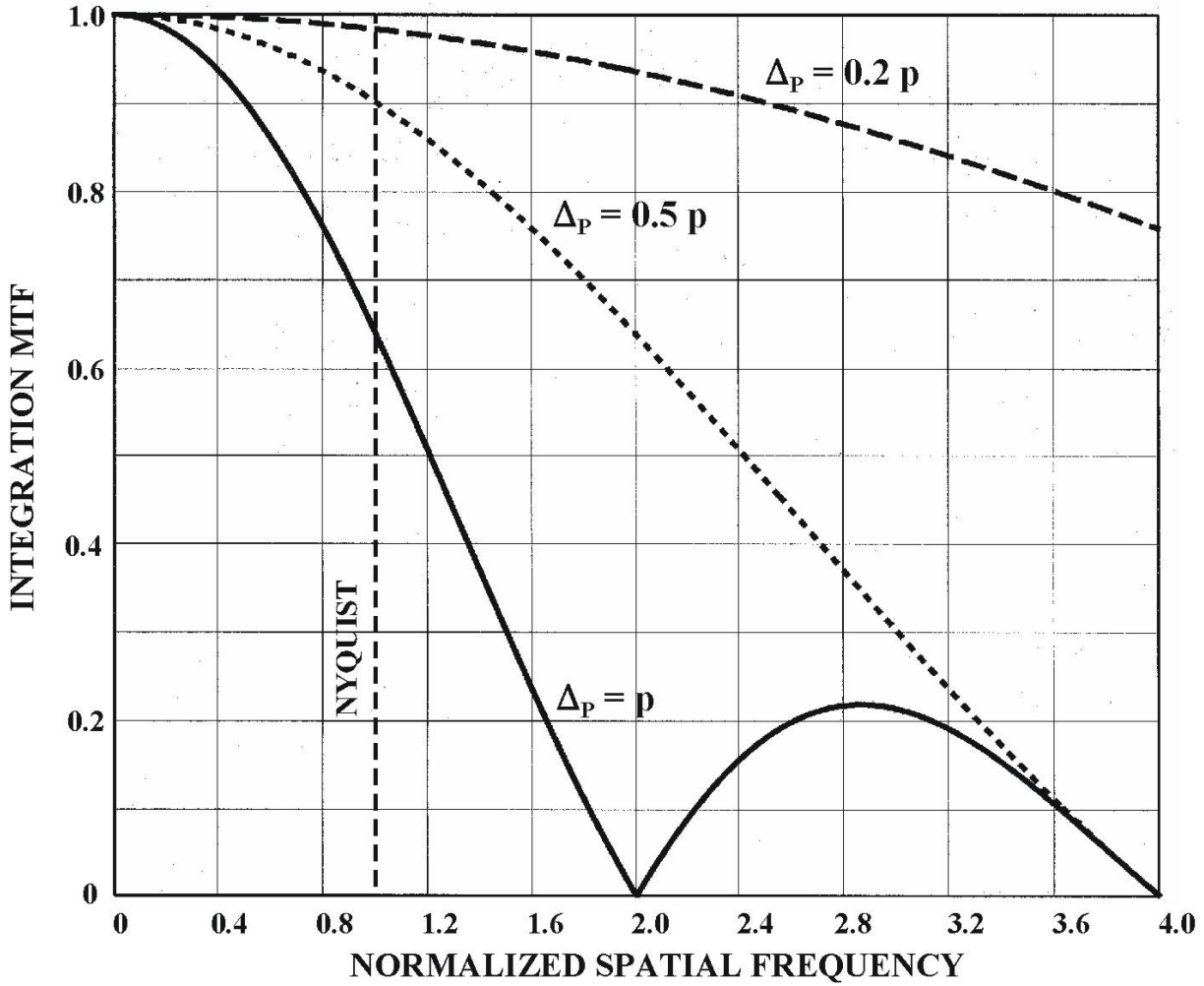


MODULATION TRANSFER FUNCTION

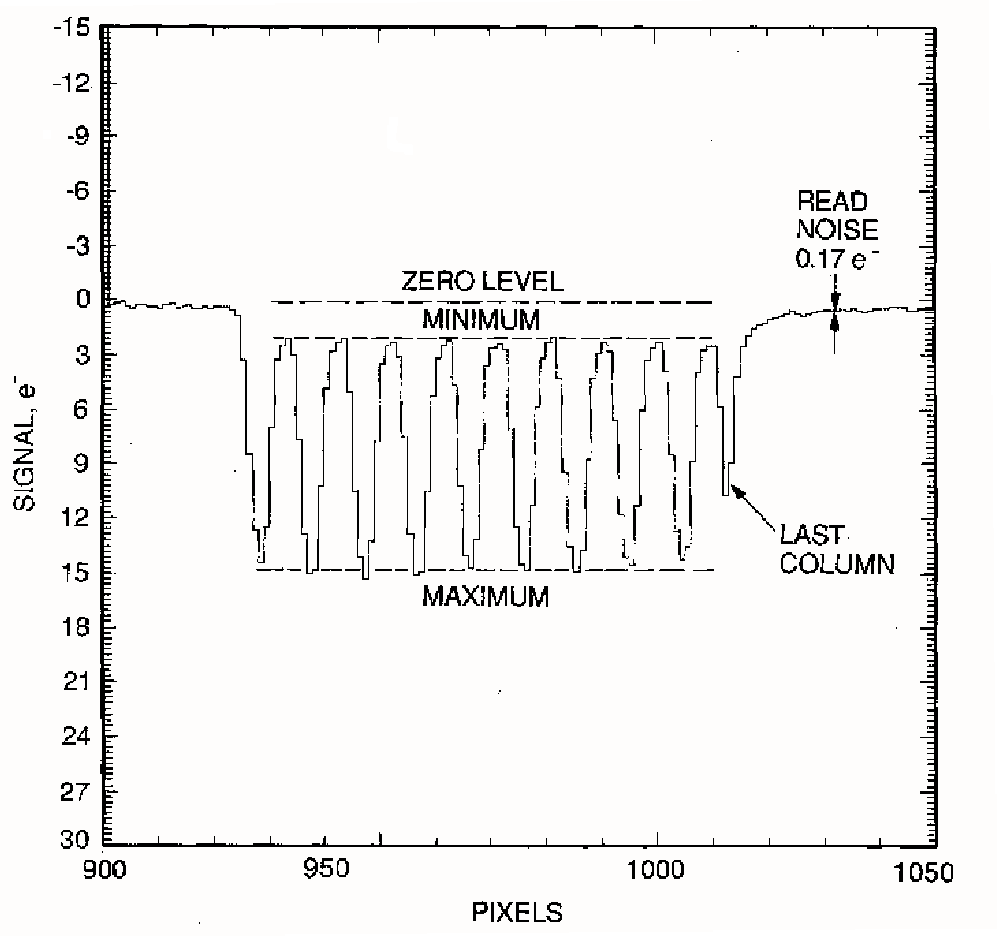
$MTF_i = SINC (\pi f \Delta P / 2 f_n d)$

Where:
MTF_i = Integration MTF
f = spatial frequency of image
ΔP = Pixel Aperture Opening
d = Pixel Pitch
f_n = Nyquist frequency

MODULATION TRANSFER FUNCTION



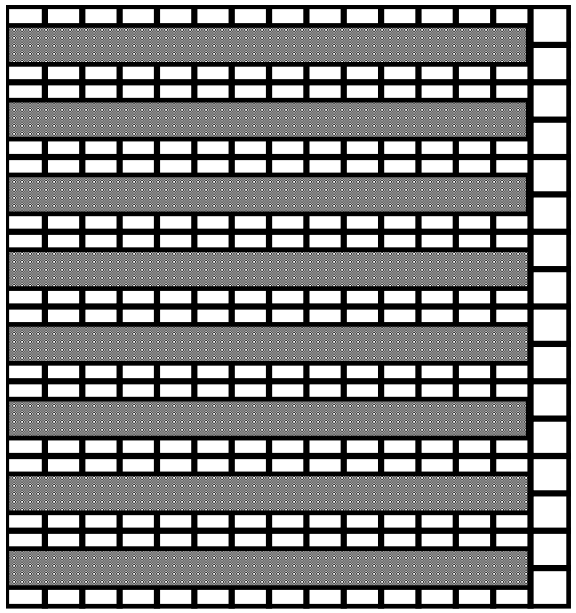
CONTRAST

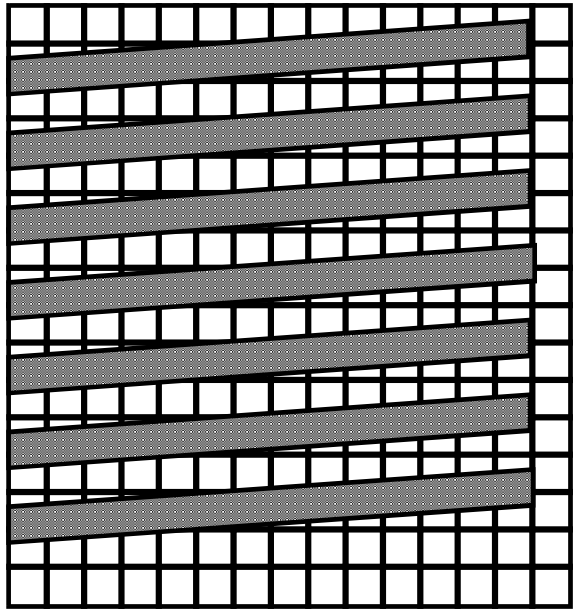


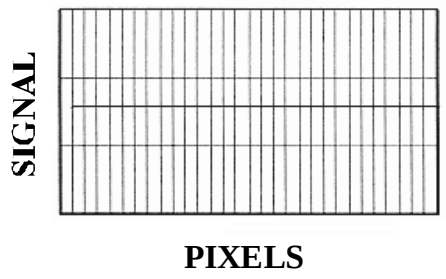
CONTRAST

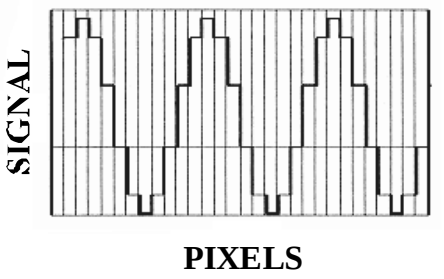
= Smax - Smin / Smax + Smin

SLANT BAR TARGET
(used for MTF measurements)

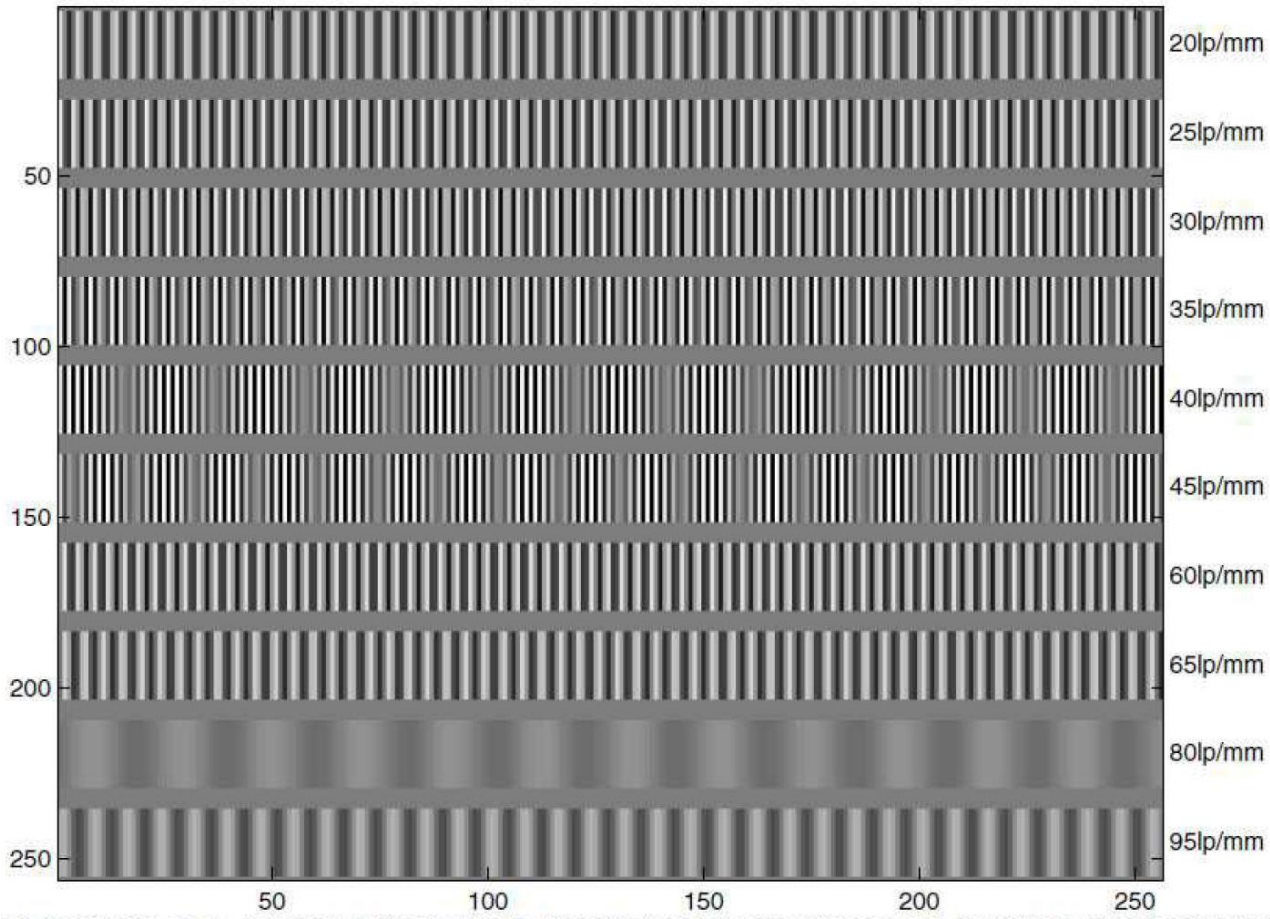








Aliasing



- Ignored effects
  - Optics MTF
  - Imager diffusion MTF
- Nyquist = 42 lp/mm
- 256 × 256 array

Like when you see a striped shirt on TV

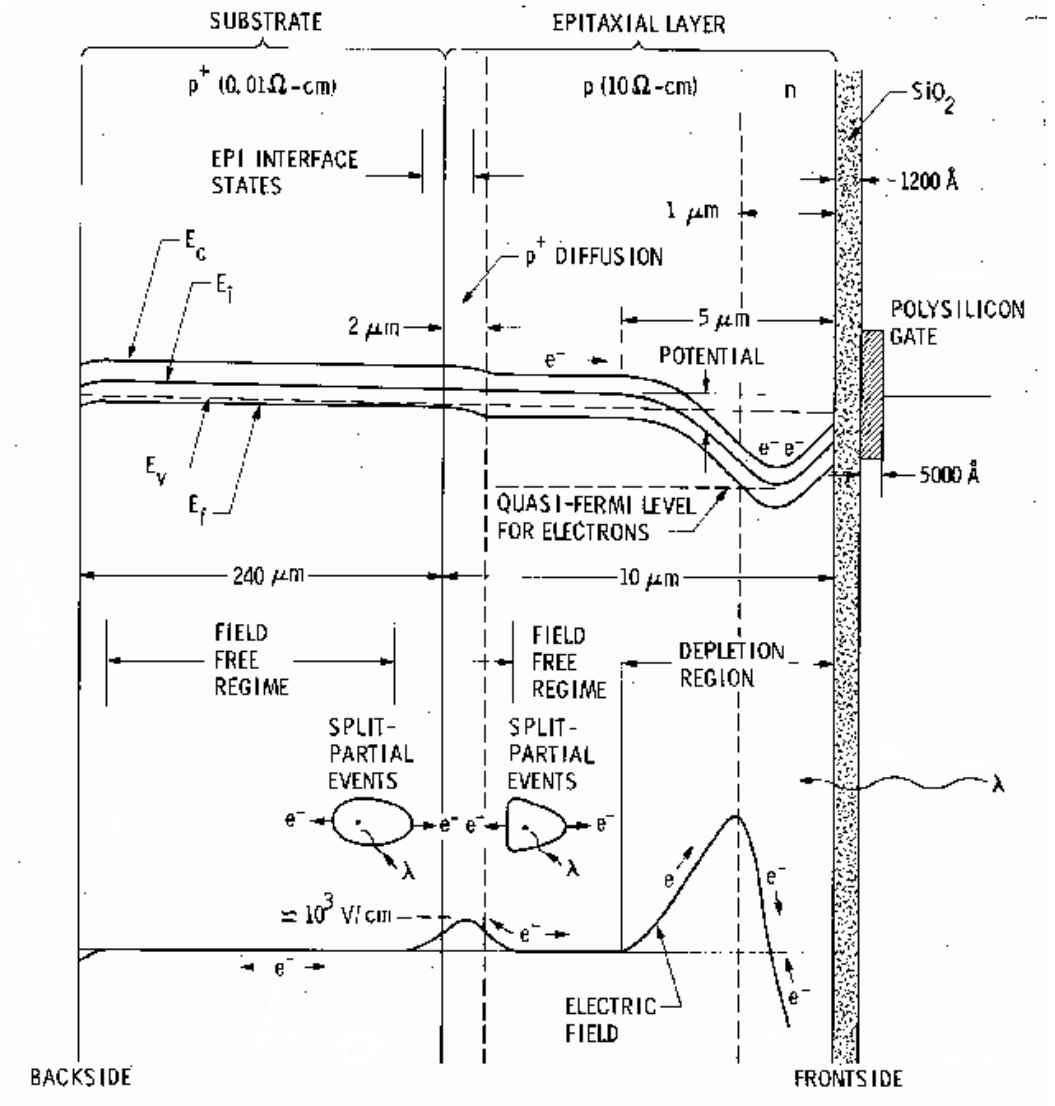
CHARGE DIFFUSION MTF

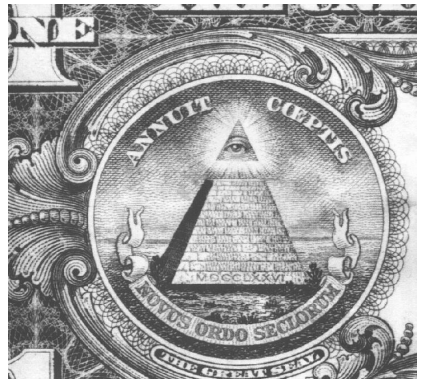
Charge generated in field free region may wind up in wrong pixel: diffuses randomly through device layer (epi or bulk substrate)

Images can be smeared depending on how much of the signal was generated in field free region

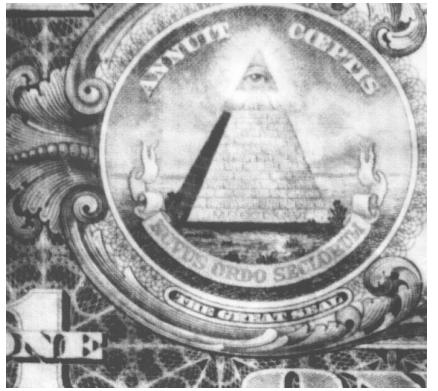
Depth of photon penetration is wavelength dependent: MTF will exhibit same dependency

Frontside illuminated: longer wavelengths may interact in field free region





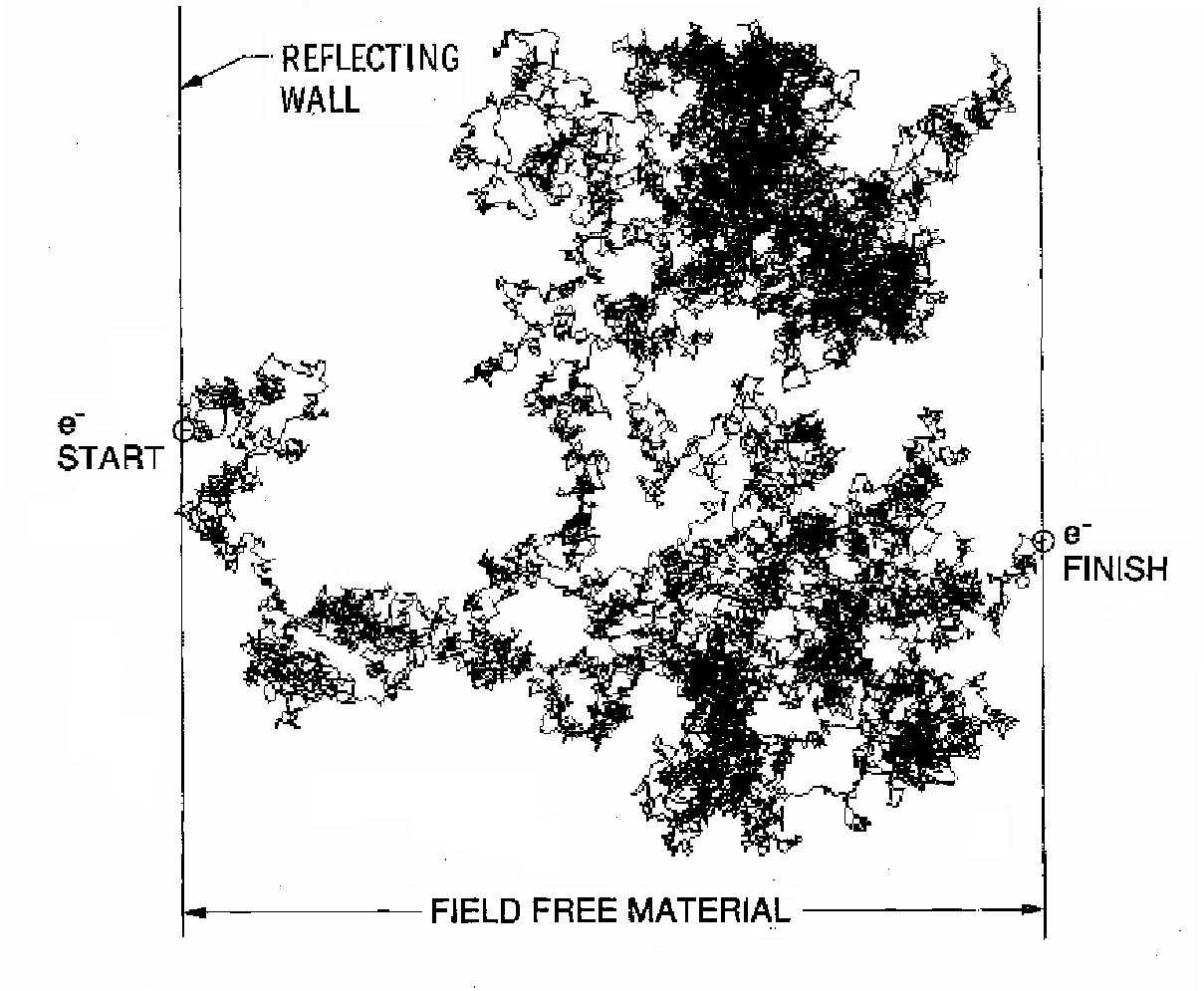
400nm light:
Little charge diffusion
High Diffusion MTF

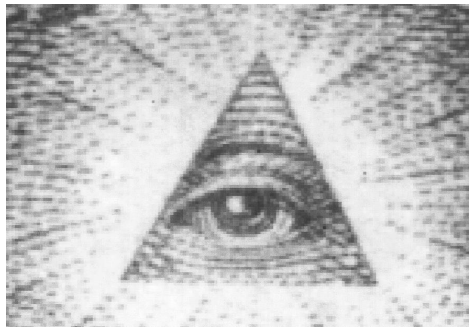


900nm light
Significant charge diffusion
Low Diffusion MTF

CHARGE DIFFUSION

Charge can easily wind up in wrong pixel if generated in field free region



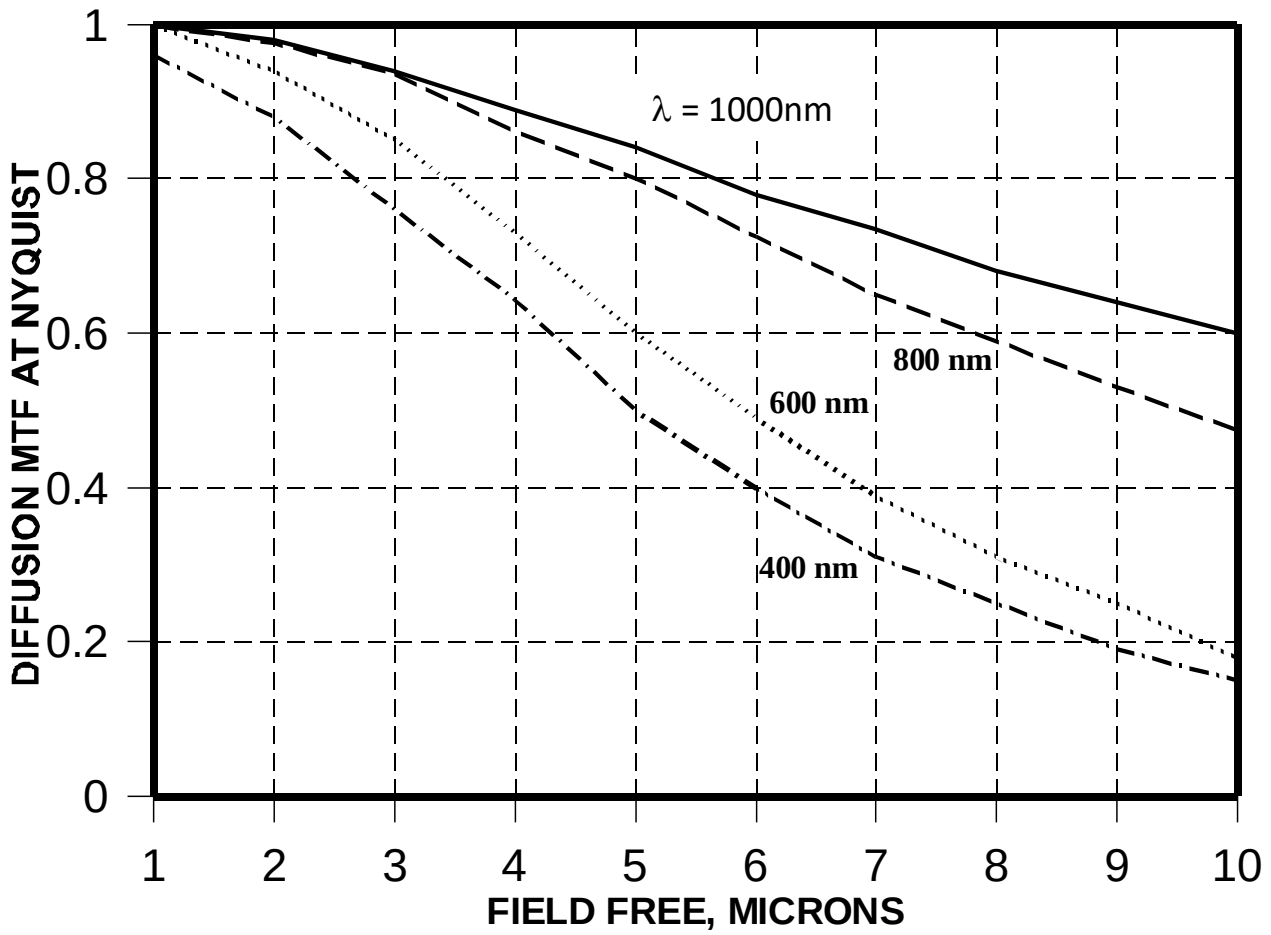


400nm light:
Little charge diffusion
High Diffusion MTF

900nm light
Significant charge diffusion
Low Diffusion MTF

DIFFUSION MTF vs FIELD FREE SILICON

BACKSIDE ILLUMINATION



Since light penetrates from backside, depletion region is deep in substrate: Long wavelength light penetrates to depletion region: high MTF with long wavelength

Short wavelength light may interact in field free region close to backside surface: poor MTF

BSI MTF @ long wavelength & degrades @ short wavelengths

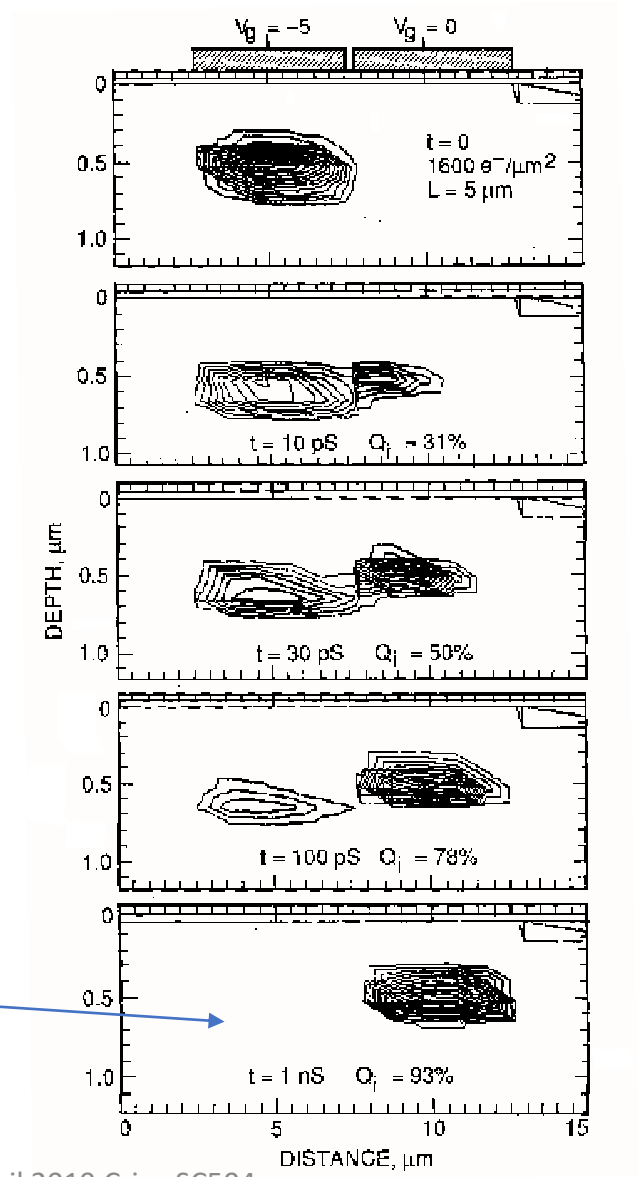
Part 5

CHARGE TRANSFER

CHARGE TRANSFER (Both CCD & 4T + CMOS)

CHARGE TRANSFER MECHANISMS. . .

1) SELF INDUCED DRIFT
2) FRINGING FIELD
3) THERMAL DIFFUSION



How much charge is left behind?
(Charge Transfer Efficiency)

X-RAY Analysis

USES. . . . .

e- / DN CALIBRATION

ABSOLUTE CHARGE TRANSFER EFFICIENCY (CTE)

CHARGE COLLECTION EFFICIENCY (POINT SPREAD)

X-RAY STANDARD

Iron-55

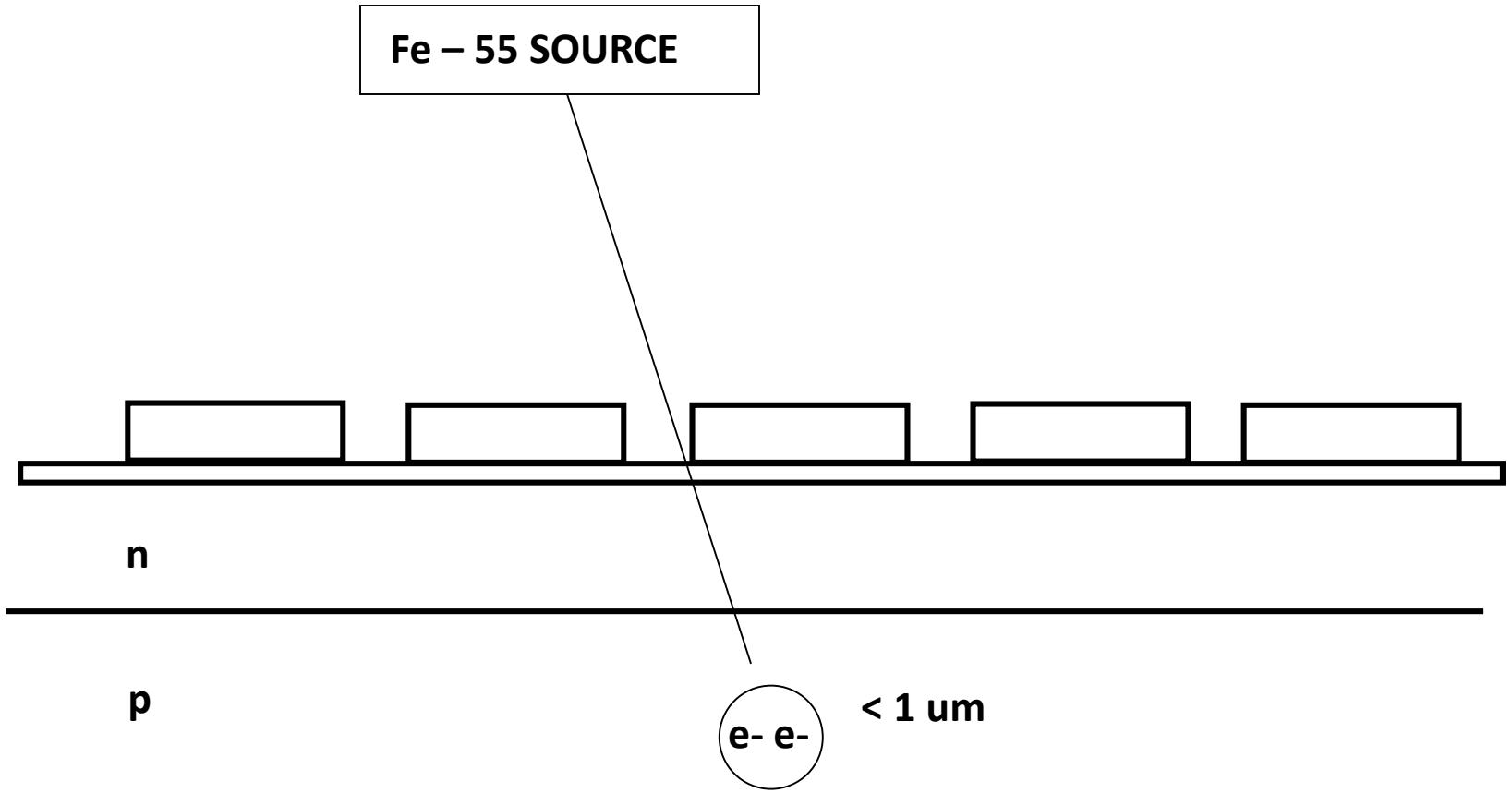
Mn x-ray emitter

1617 e- / x-ray

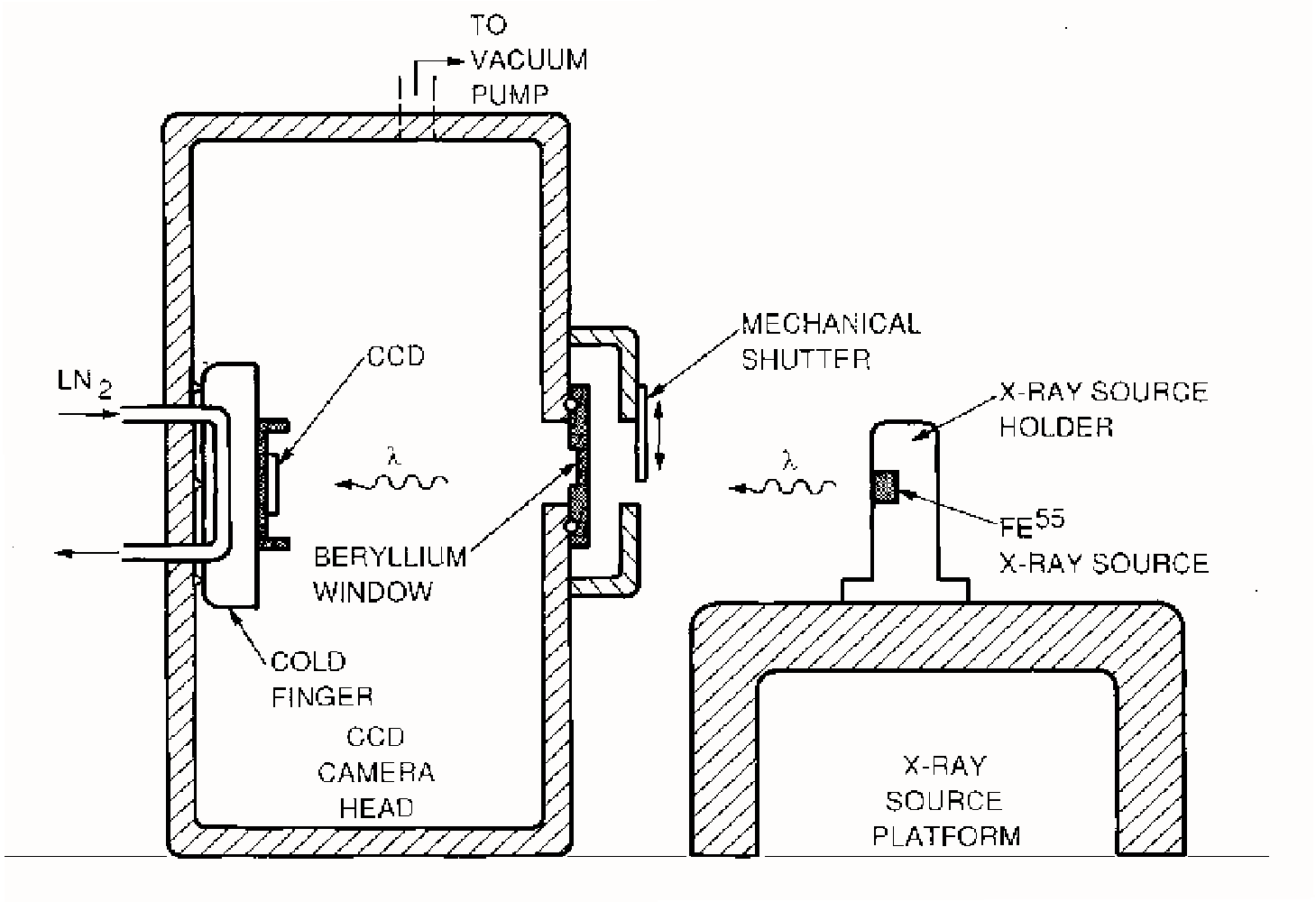
13 e- rms (Fano noise)

Electron cloud diameter < 1 micron

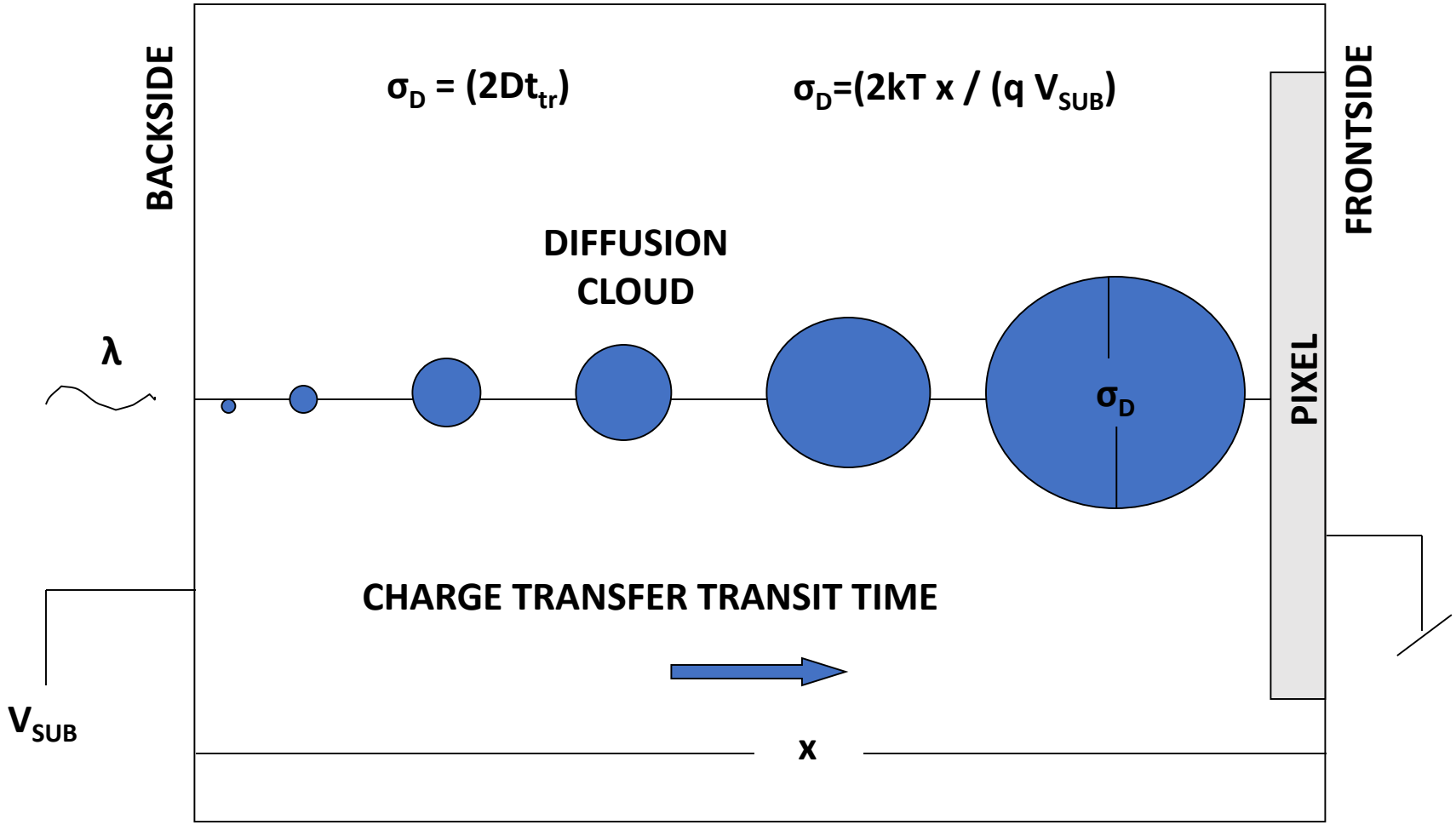
X-RAY INTERACTION



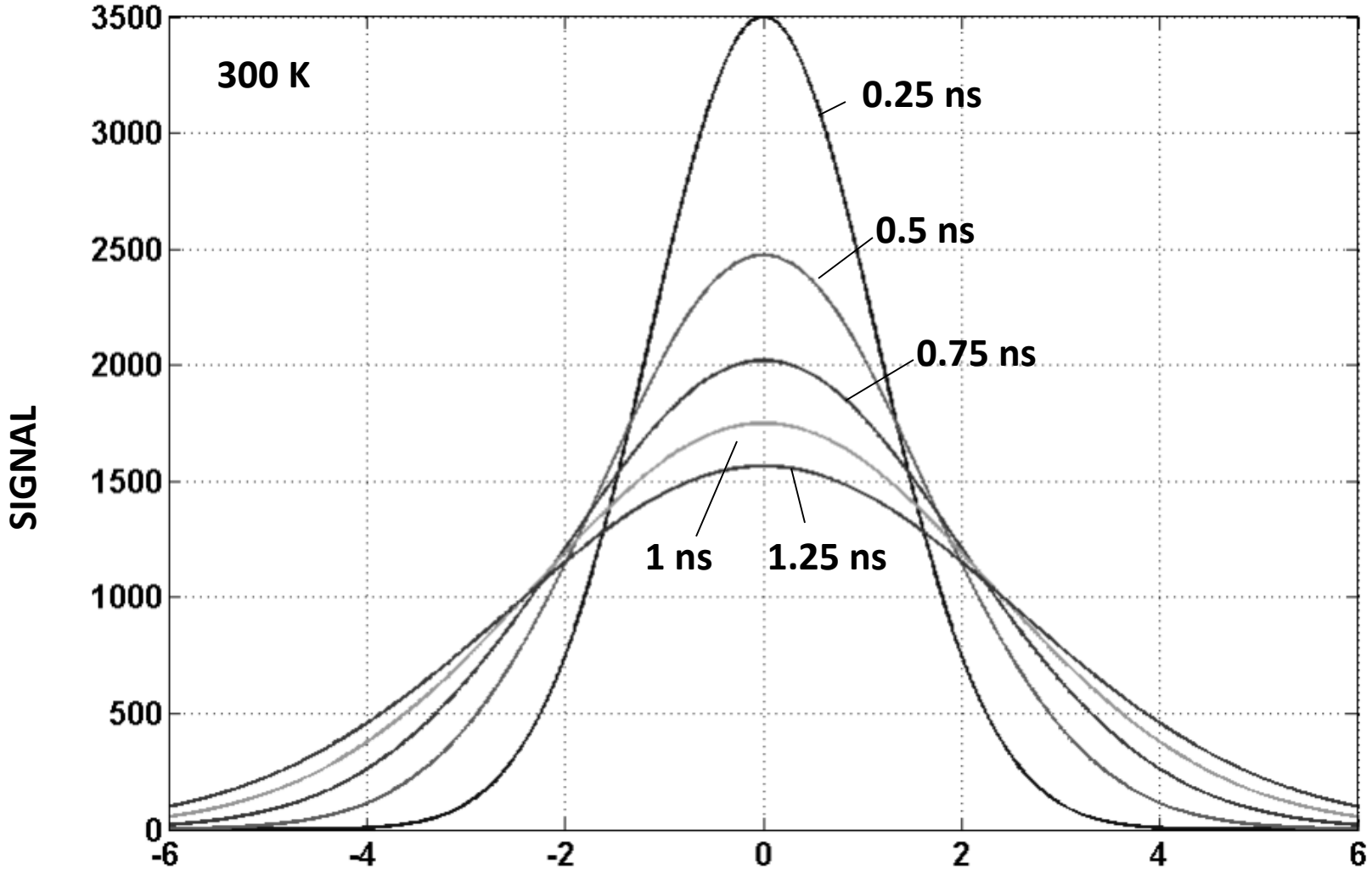
X-RAY FLAT FIELD SET UP



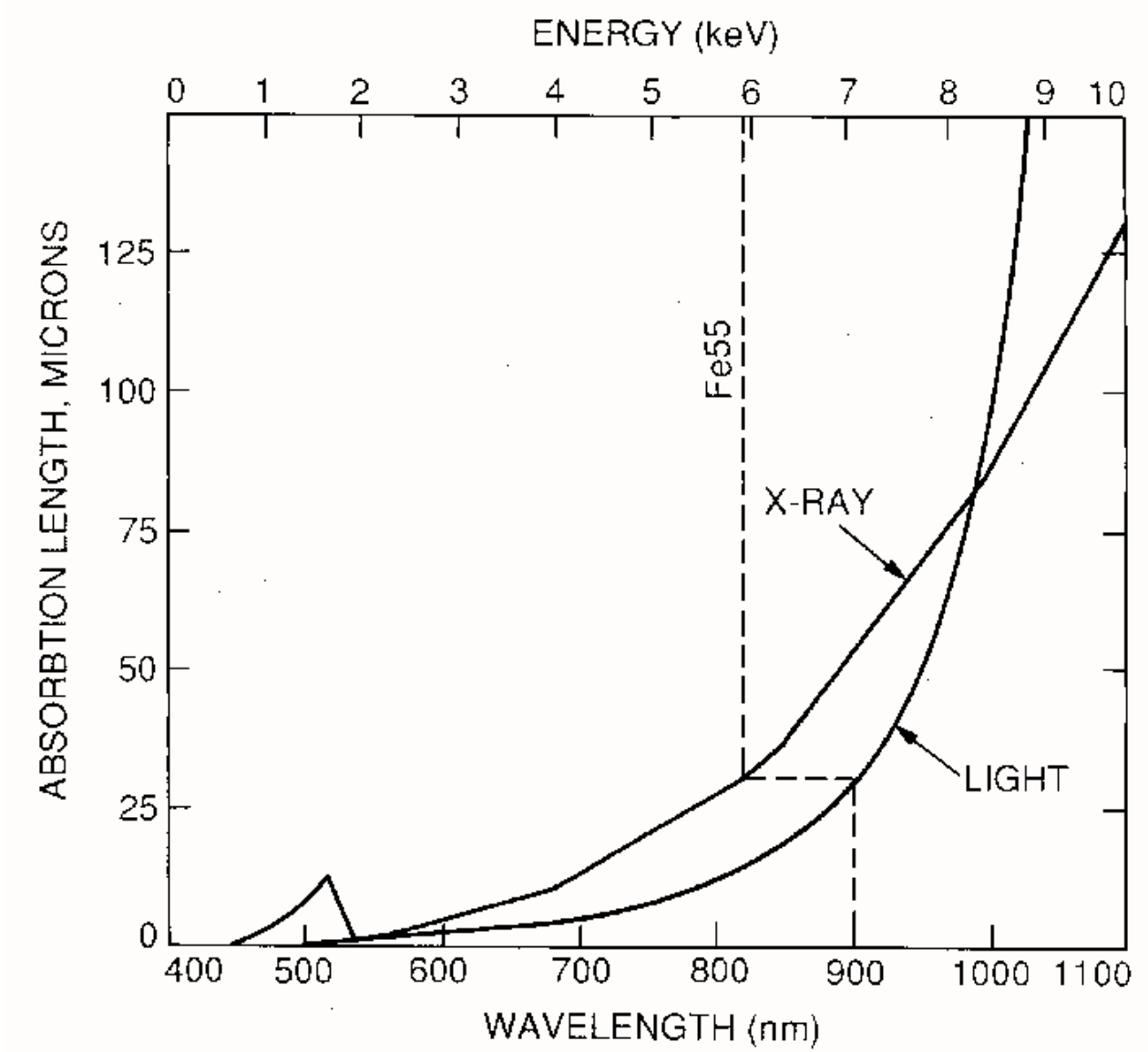
DIFFUSION vs TRANSIT TIME



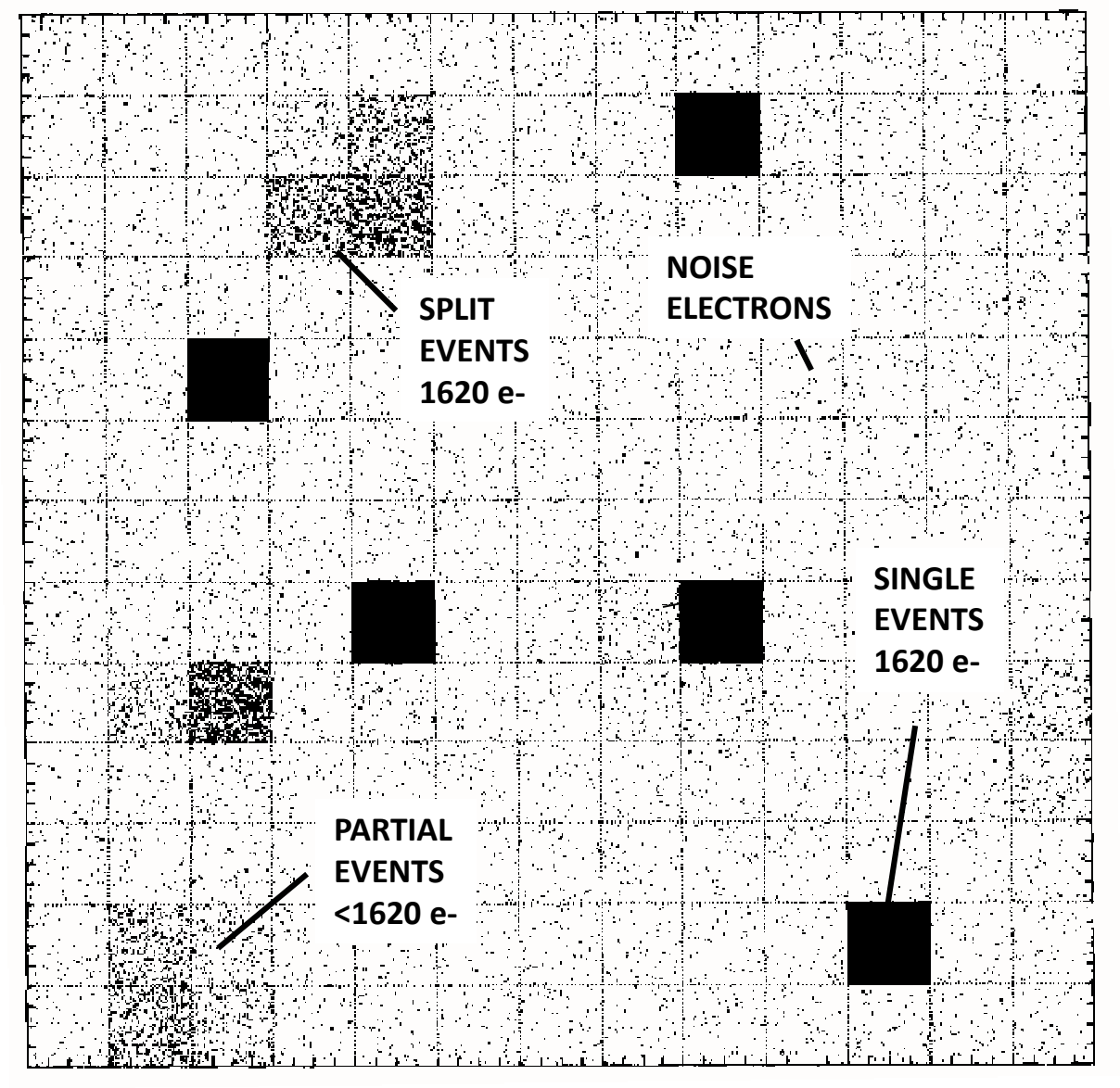
POINT SPREAD CHARGE DIFFUSION



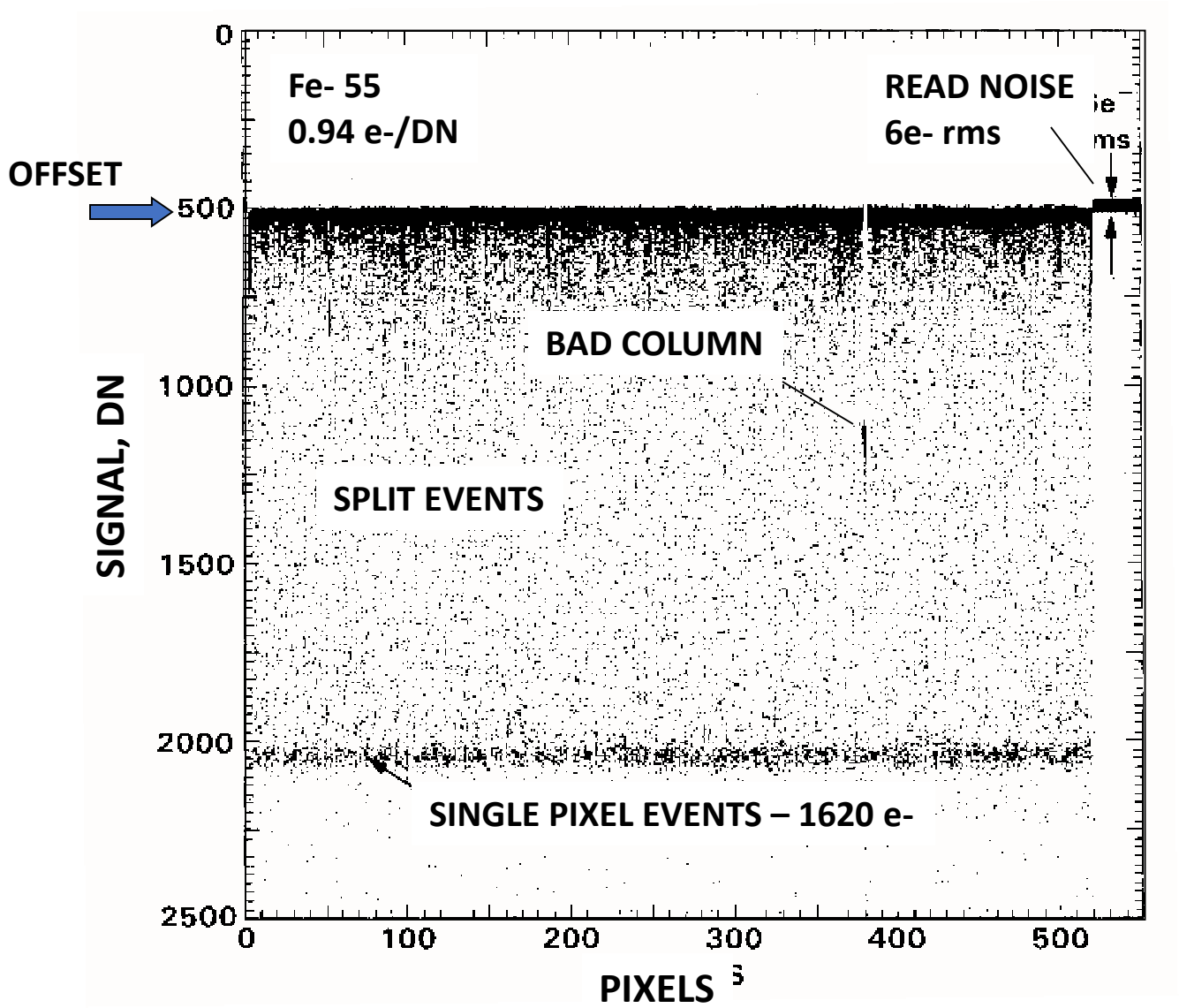
X-RAY ABSORPTION LENGTH



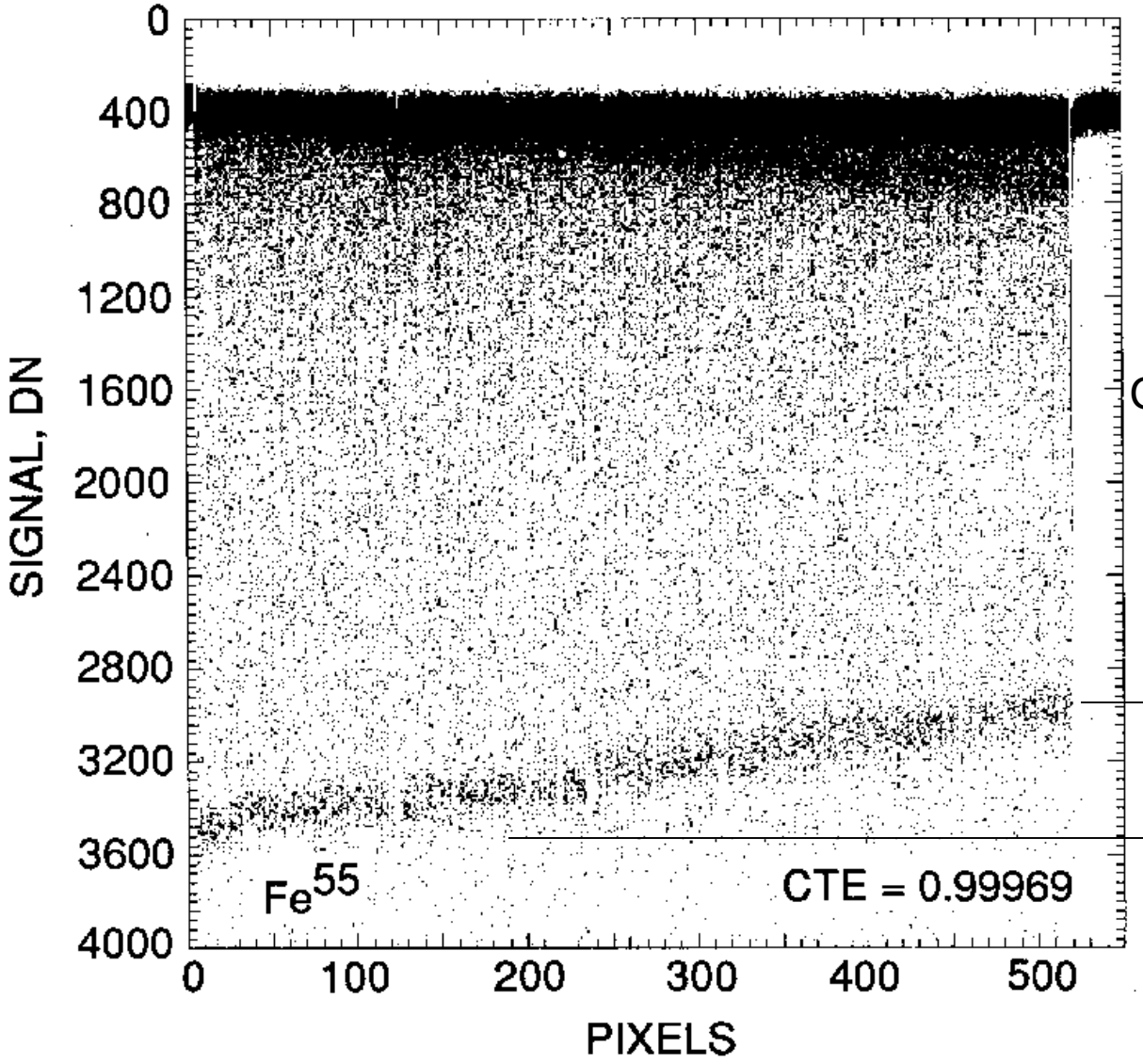
X-RAY EVENT IMAGE



X-RAY EVENT ROW STACKING



ABSOLUTE CTE MEASUREMENT



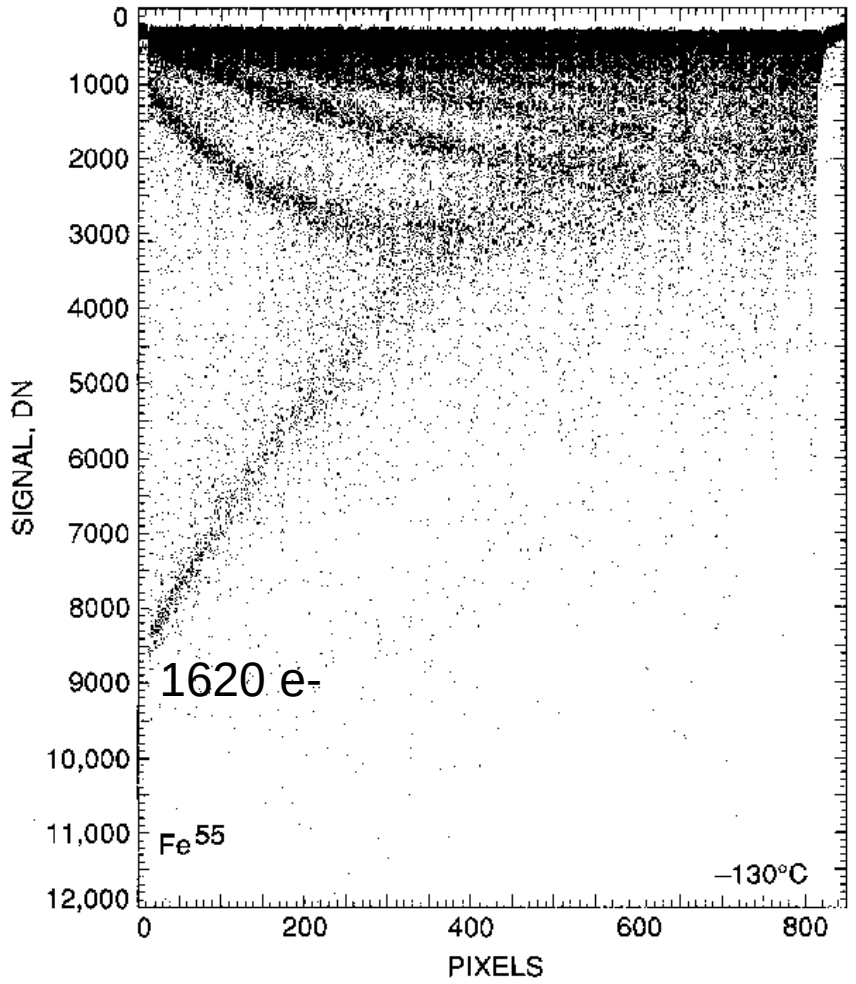
FIRST TRAILER

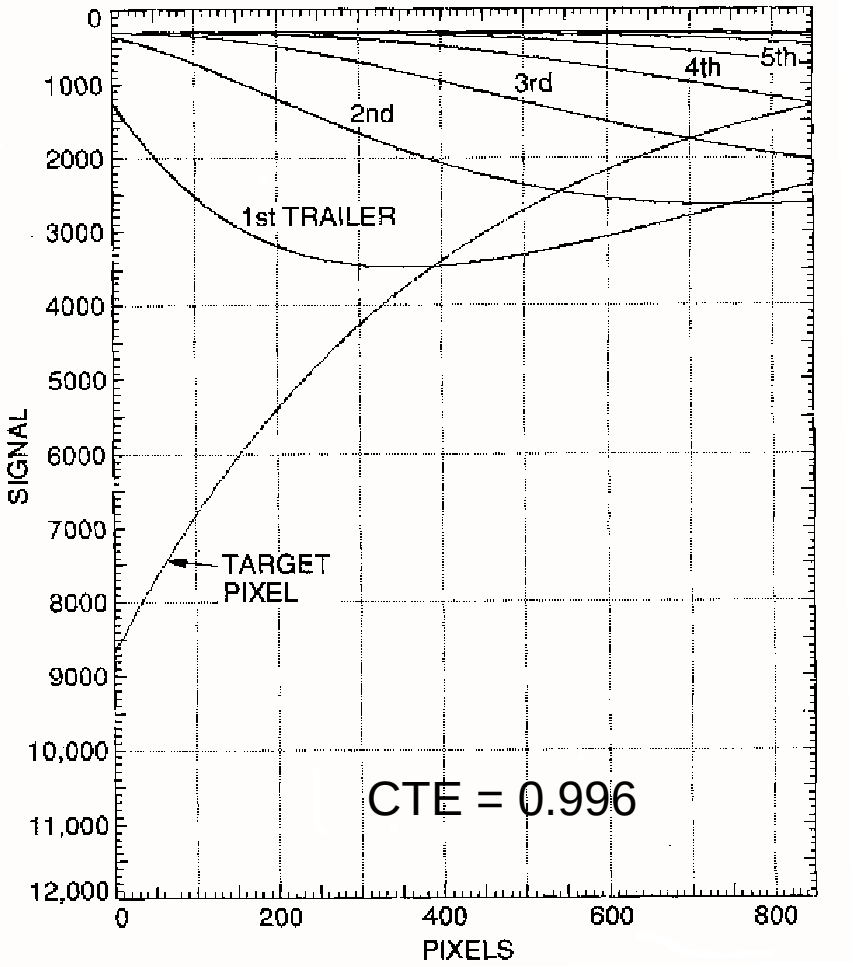
CTE = 1-261 / [1620 x 520]
= 0.99969

261 e-
LOSS

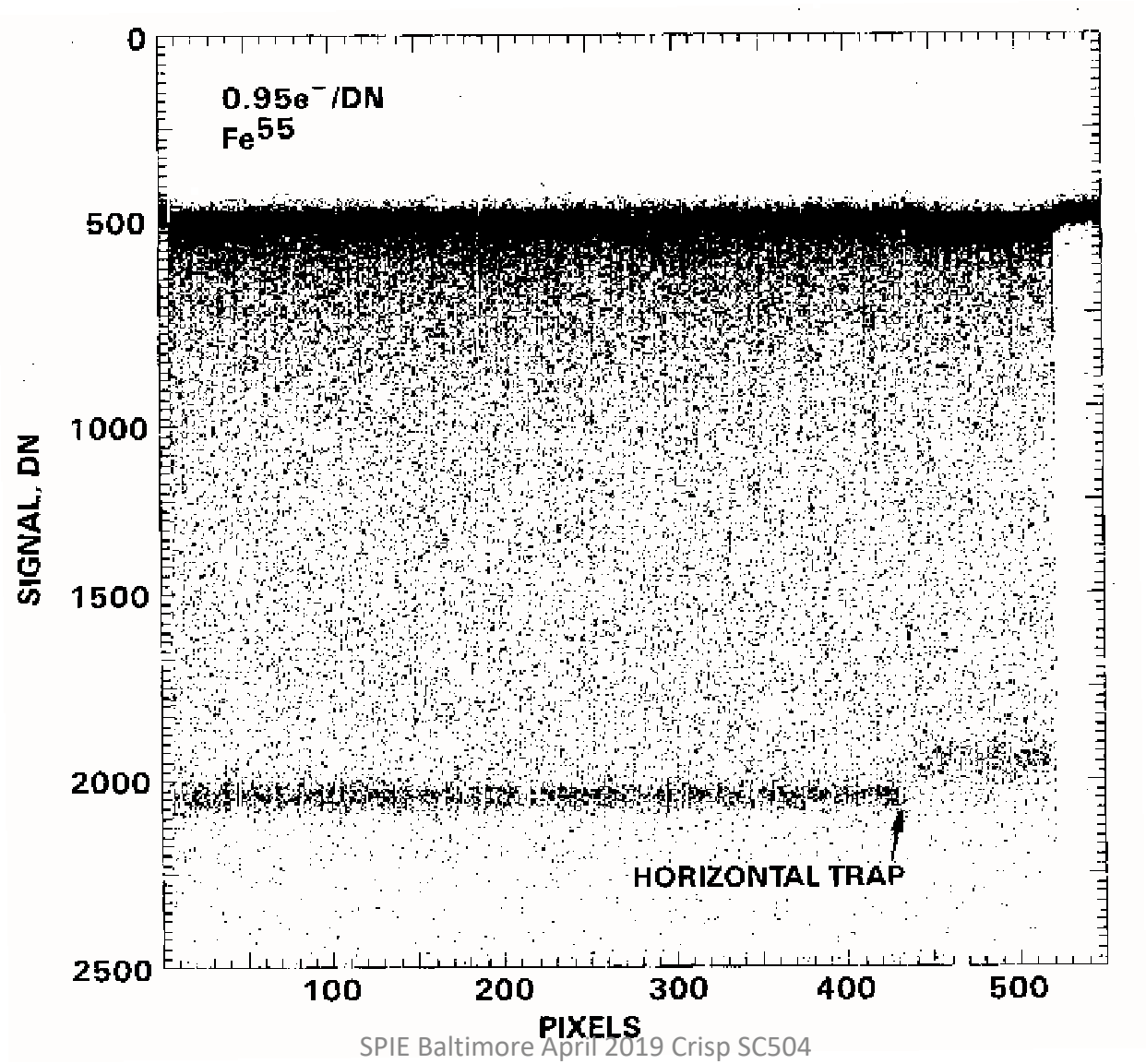
1620 e-

CCD CTE PROBLEMS
(SILICON)





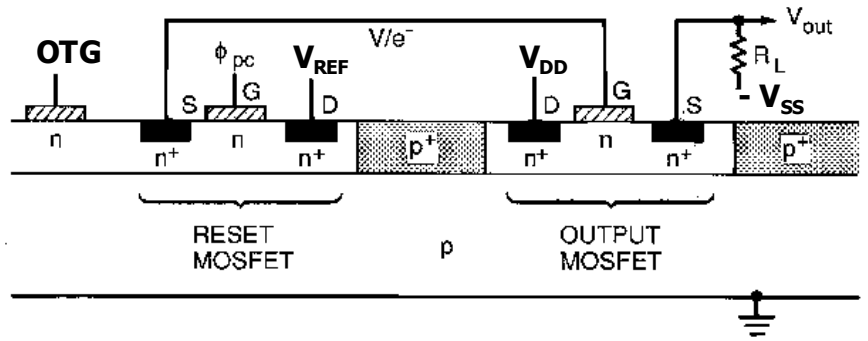
CCD CTE PROBLEMS
(TRAPS)

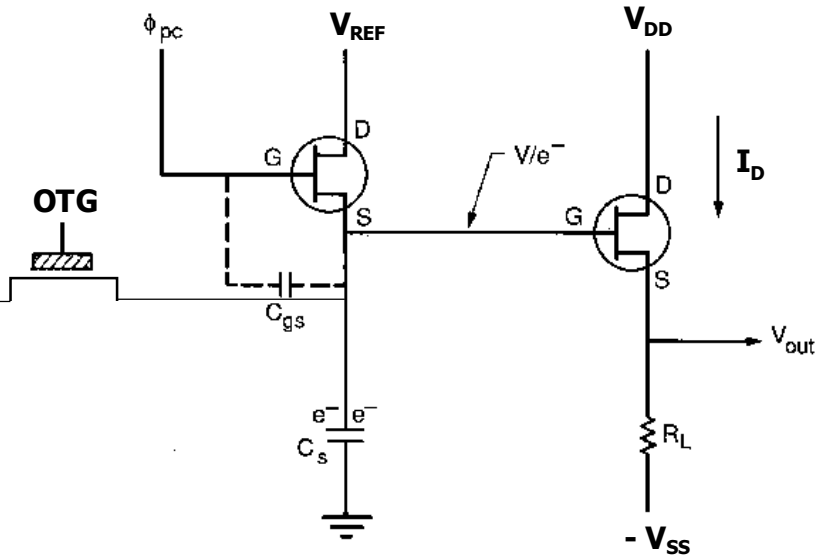


Part 6

CHARGE MEASUREMENT

OUTPUT AMPLIFIER





Charge path from horiz register

Part 6
NOISE TYPES

Shot Noise

Photo-electric Effect

Einstein's Nobel Prize (1921)

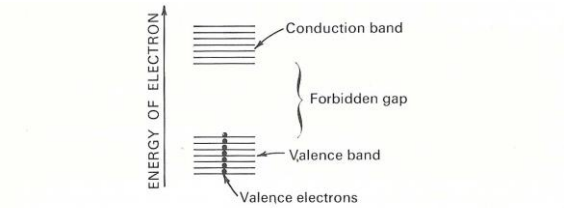
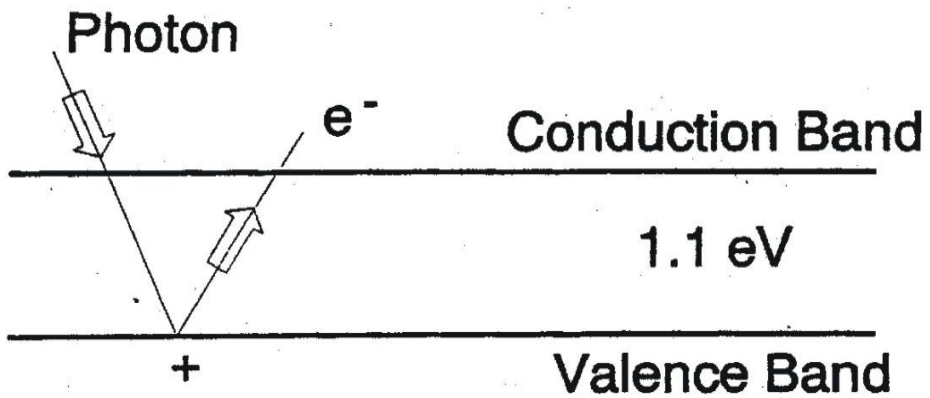


Fig. 4.1 Schematic energy band representation for electrons in a solid illustrating the energy bands and a forbidden gap.



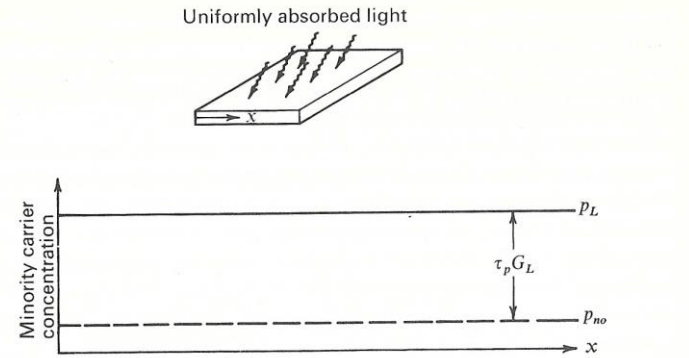
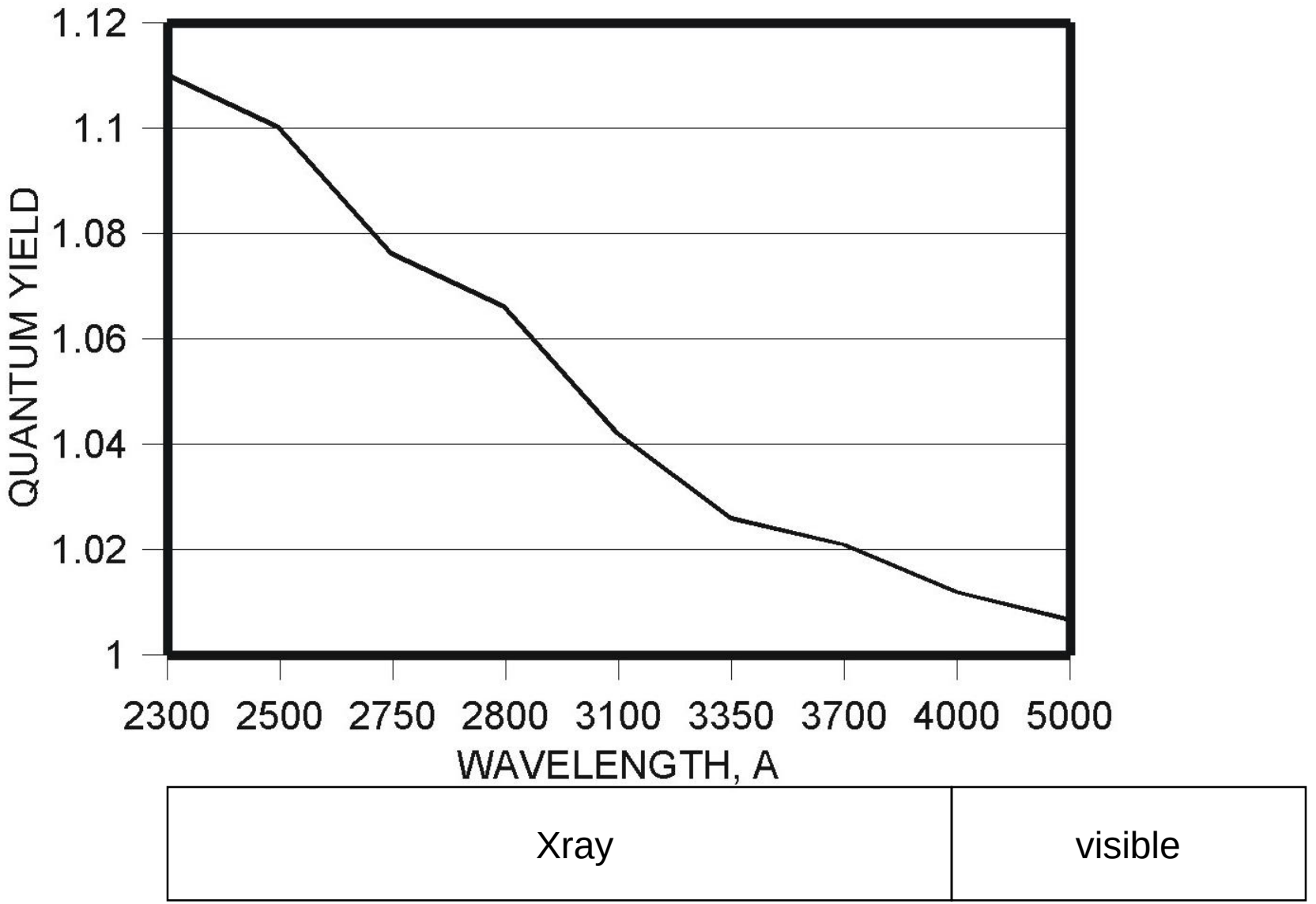


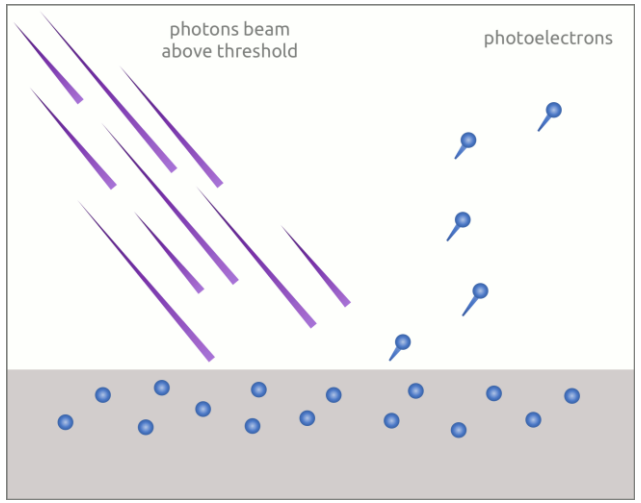
Fig. 5.2 Illustration of the steady-state minority carrier distribution in a uniformly illuminated semiconductor sample, in the absence of surface recombination.

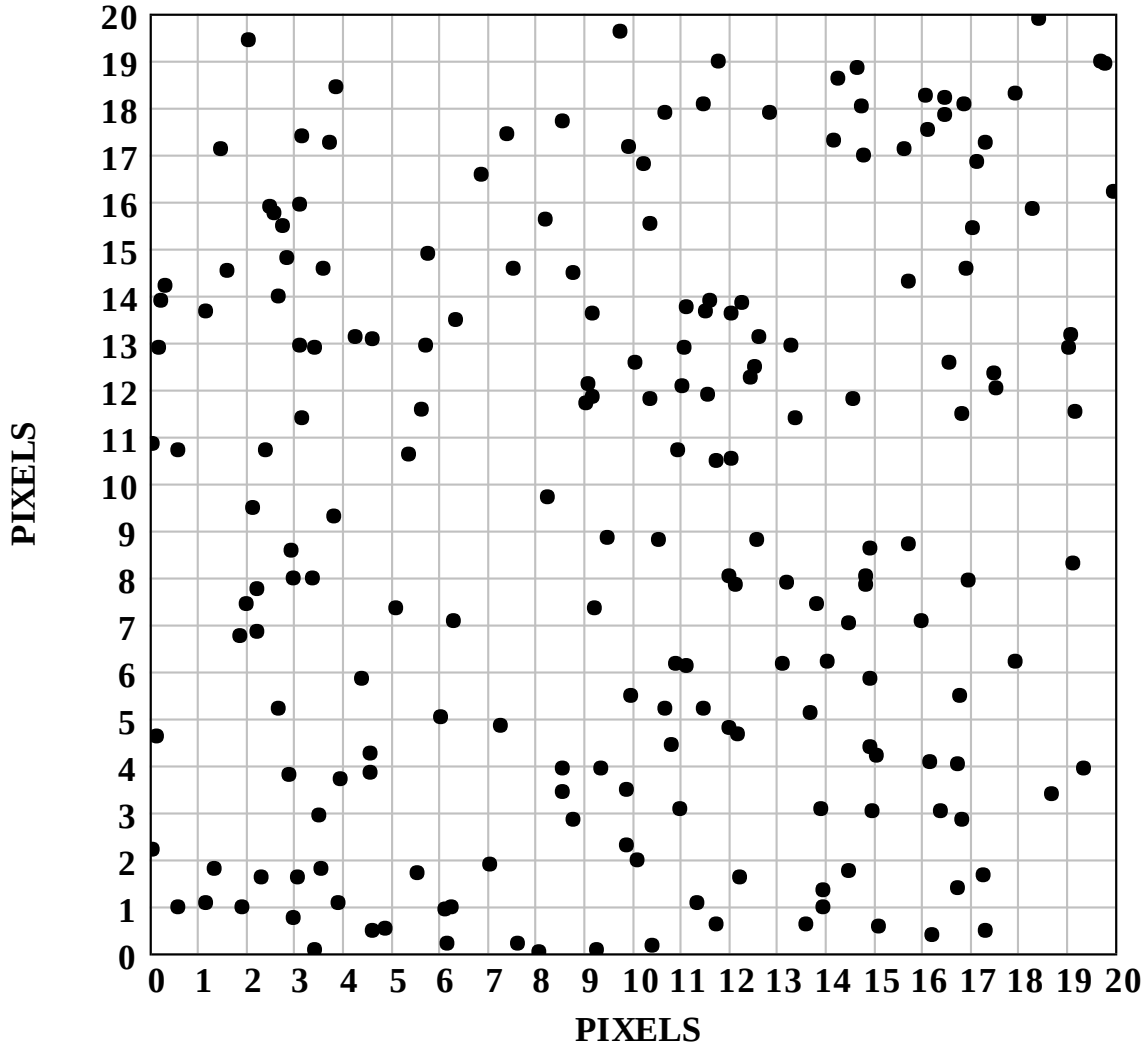
- **4000 A < λ < 10,000 A , e - = 1**
- **1 A < λ < 1000 A , e - = eV/ 3.65 eV/e-**

Quantum Yield

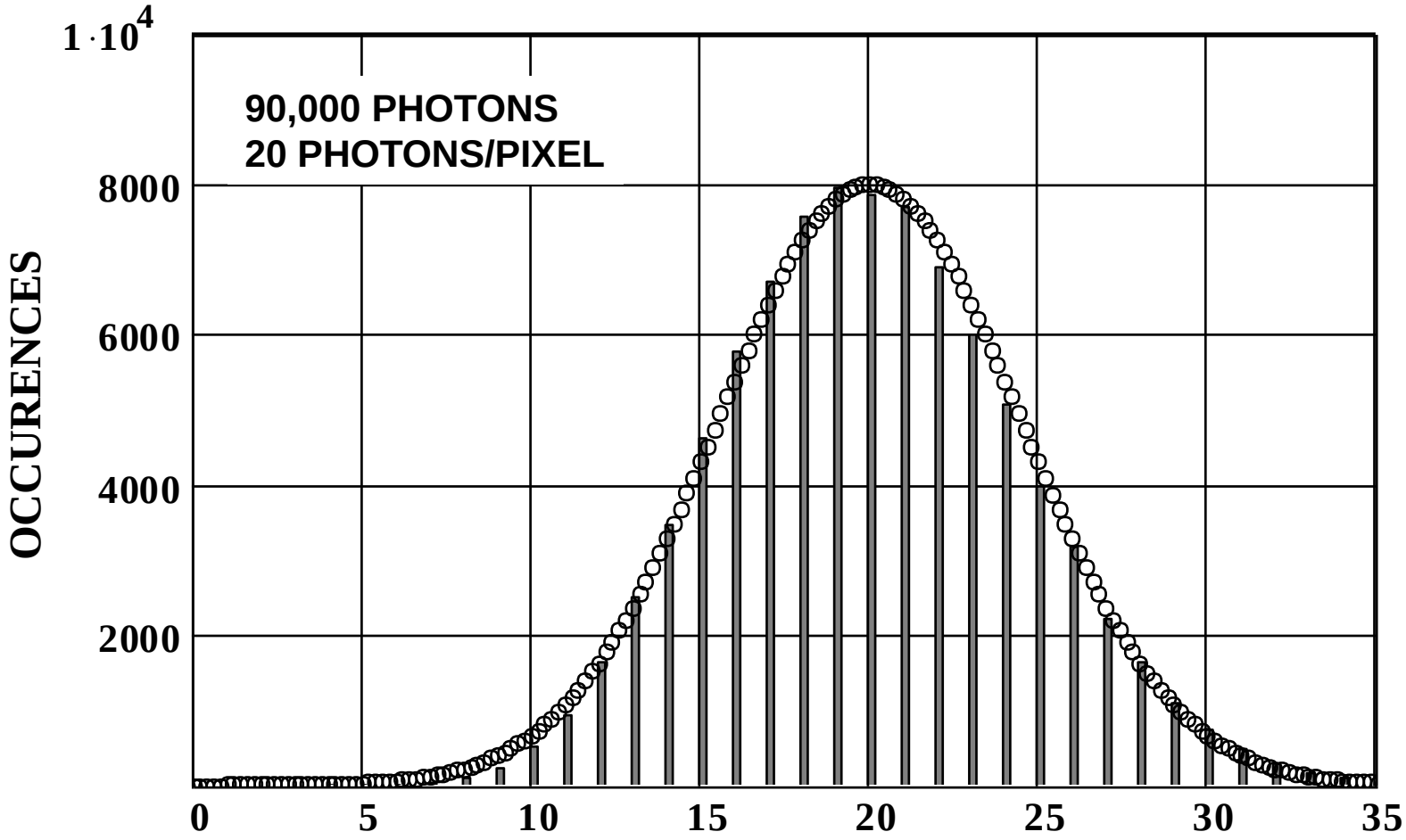


PHOTON STATISTICS





PHOTON STATISTICS



SHOT NOISE

$$\sigma_{\mathrm{SHOT}}(\mathrm{photons}) = (P)^{\frac{1}{2}} \qquad \text{(photons)}$$

Shot noise of photons interacting with silicon in photon units:

$$\sigma_{\mathrm{SHOT}}(\mathrm{photons}) = (P_I)^{\frac{1}{2}} \qquad \text{(photons)}$$

In electron units:

$$\sigma_{\mathrm{SHOT}}(\mathrm{e}-) = \eta_i (P_I)^{\frac{1}{2}} = (\eta_i^2 * S(e-)/\eta_i)^{\frac{1}{2}} = (\eta_i * S(e-))^{\frac{1}{2}} \qquad \text{(electrons)}$$

$S(e-) = \eta_i P_I$

$P_I = S(e-)/\eta_i$

where

σ_{SHOT}(e-) = shot noise (rms e-)
η_i = quantum yield (e-/interacting photon)
P_I= interacting photons/ pixel
S(e-) = signal (e-)

SNR for Quantum Yield of 1 and for >> 1

$$Noise(e-) = (\eta_i * S(e-))^{\frac{1}{2}}$$ (electrons)

SNR = $S(e-)$ / $(\eta_i * S(e-))^{\frac{1}{2}}$ (dimensionless)

For η_i=1 (visible light, silicon)

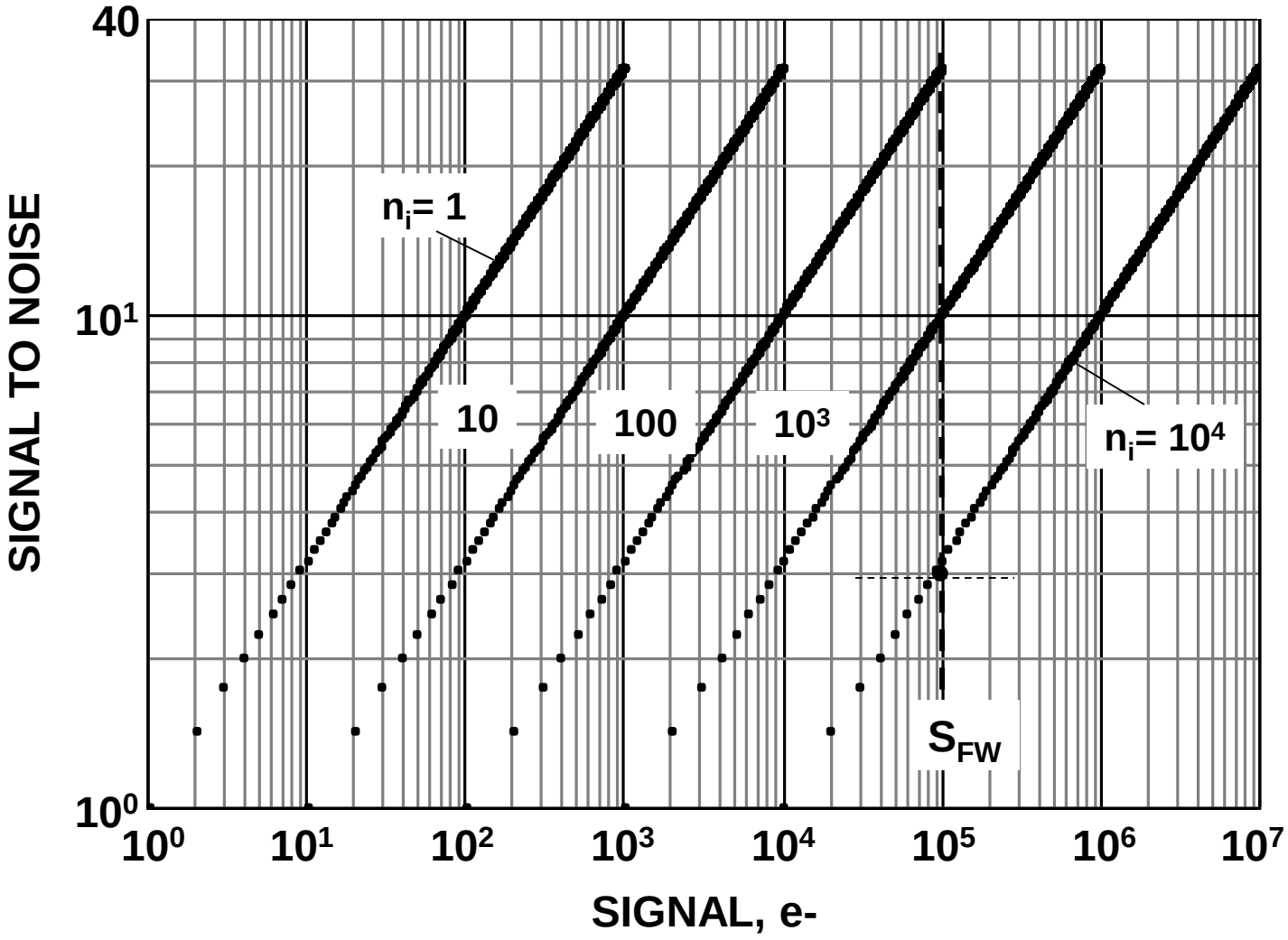
SNR = $S(e-)$ / $(1 * S(e-))^{\frac{1}{2}} = (S(e-))^{\frac{1}{2}}$ (dimensionless)

For η_i=1620 (Fe_{55} Soft Xray in Silicon)

SNR = = $S(e-)$ / $(1620 * S(e-))^{\frac{1}{2}} = (S(e-)/1620)^{\frac{1}{2}}$ (dimensionless)

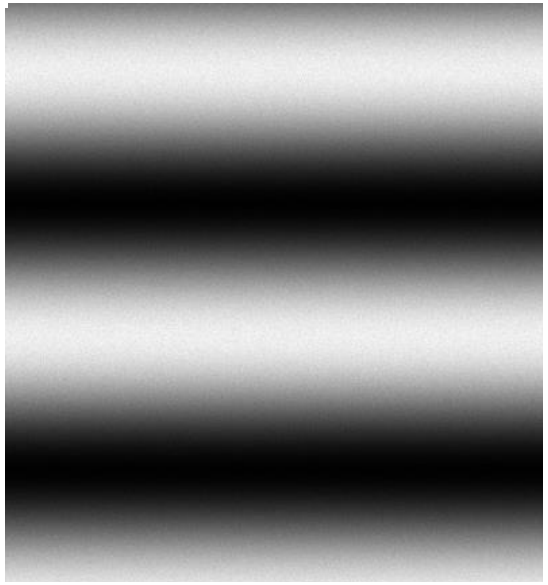
XRAY and other η_i >1 images are significantly noisier than visible light images

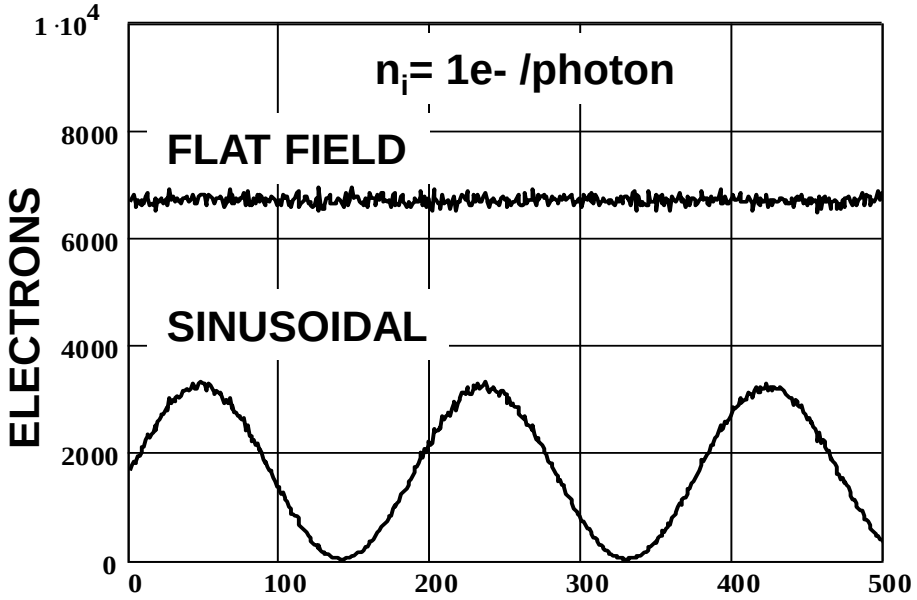
SIGNAL TO NOISE vs QUANTUM YIELD



SIGNAL TO NOISE vs QUANTUM YIELD

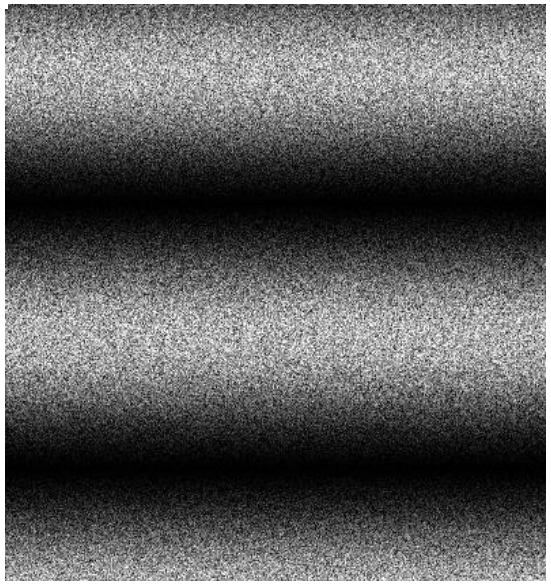
Standard Visible Light:
Ni = 1 e-/photon

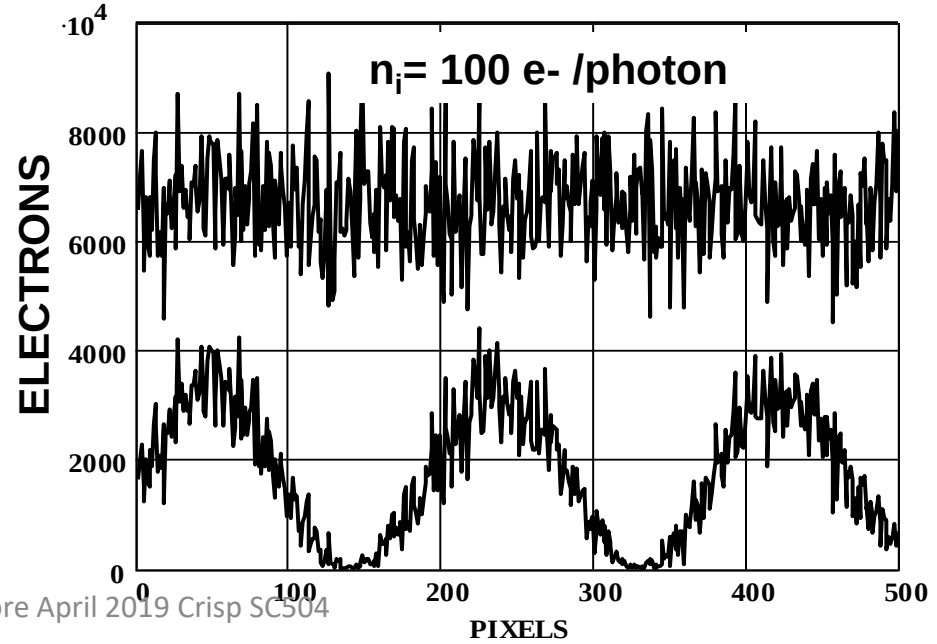




Ni >> 1 e-/photon

Direct X-RAY CCD/CMOS Electron multiplying - CCD/EM-CMOS and EM films, all suffer from this shot noise limitation issue





Read Noise

READ NOISE

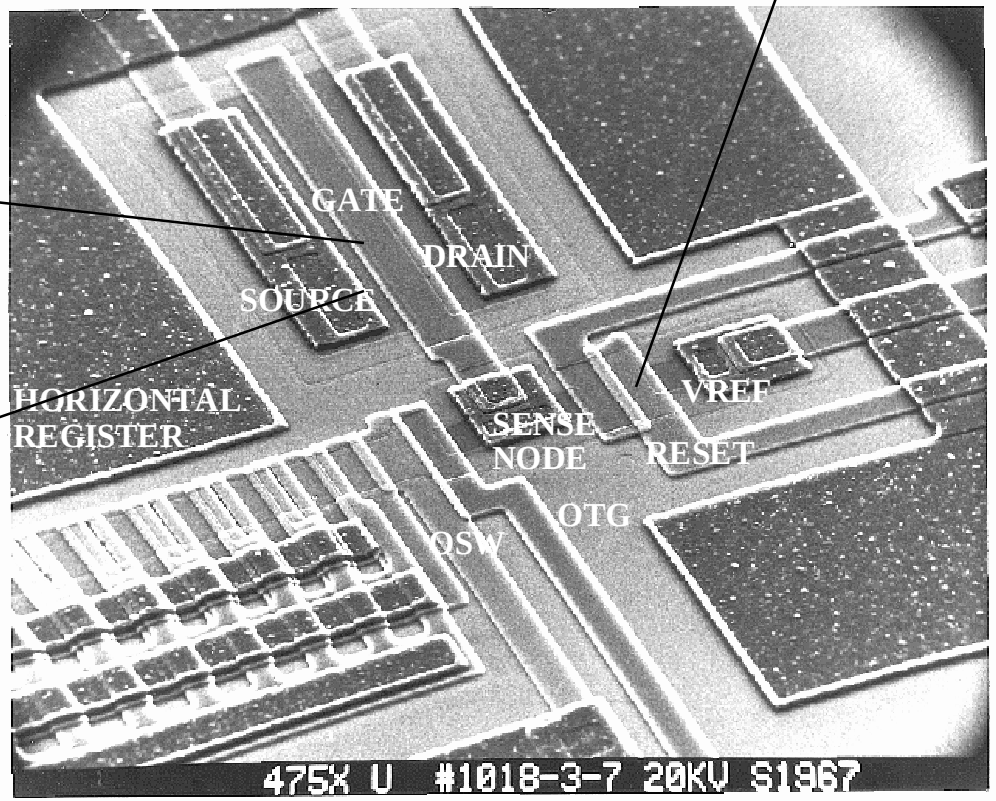
- **READ NOISE (rms e-) REPRESENTS THE “UNCERTAINTY” IN MEASURING PIXEL CHARGE**
- **CHARGE GENERATION, COLLECTION AND TRANSFER CAN BE NOISELESS PROCESSES. SIGNAL PROCESSING CAN ALSO BE A NOISELESS PROCESS**
- **THE SOURCE FOLLOWER AMPLIFIER IS THE ONLY FUNDAMENTAL NOISE SOURCE**

OUTPUT AMPLIFIER NOISE SOURCES

kTC RESET NOISE

SF FLICKER NOISE =
INTERFACE ELECTRON TRAPS
WITHIN SOURCE FOLLOWER CHANNEL

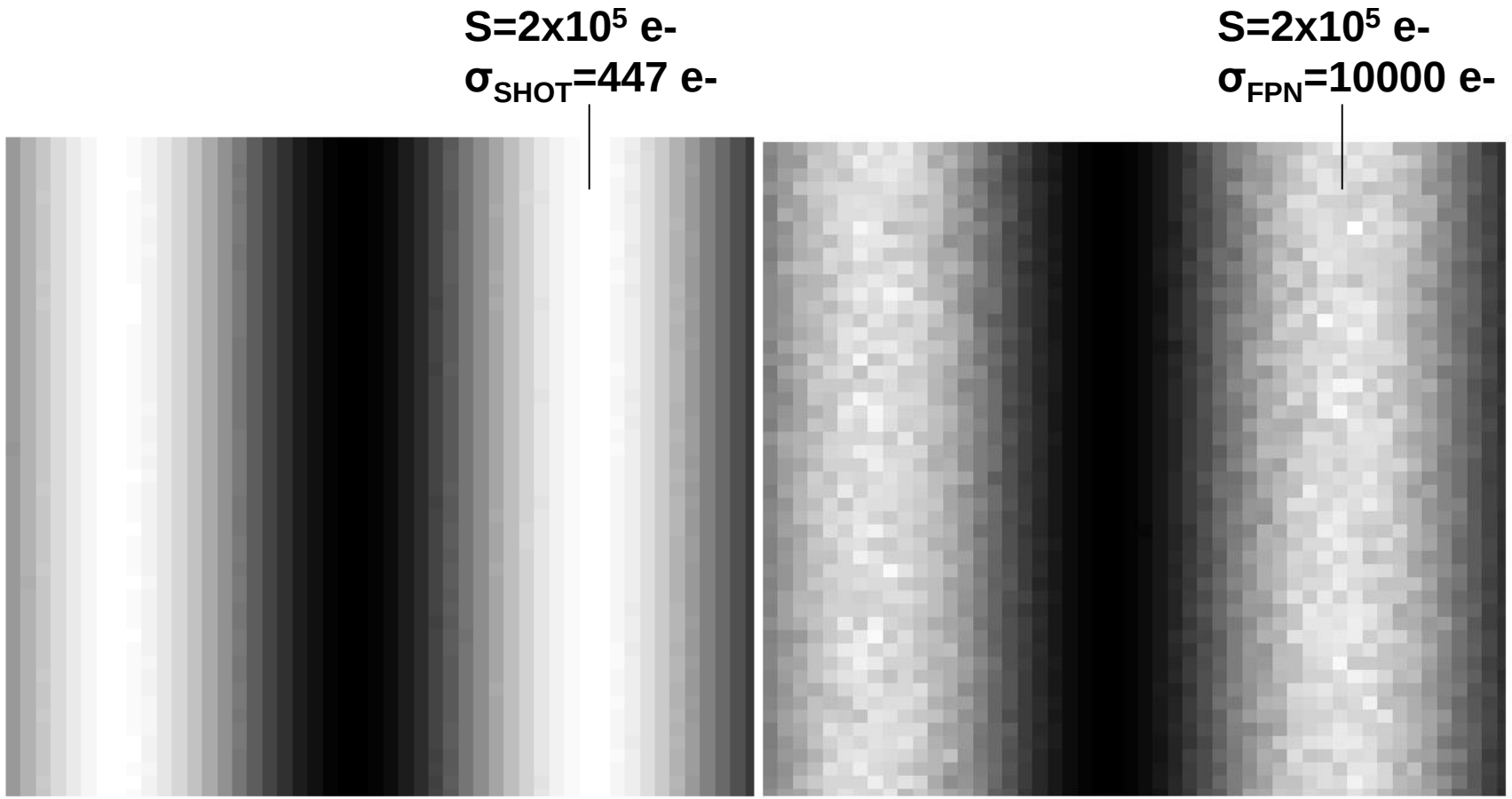
SF WHITE NOISE=
THERMAL ELECTRON MOTION
WITHIN SOURCE FOLLOWER CHANNEL



SF FLICKER AND WHITE NOISE
DEPENDENT ON MOSFET SIZE
AND BIAS CURRENT
(THE LARGER THE BETTER)

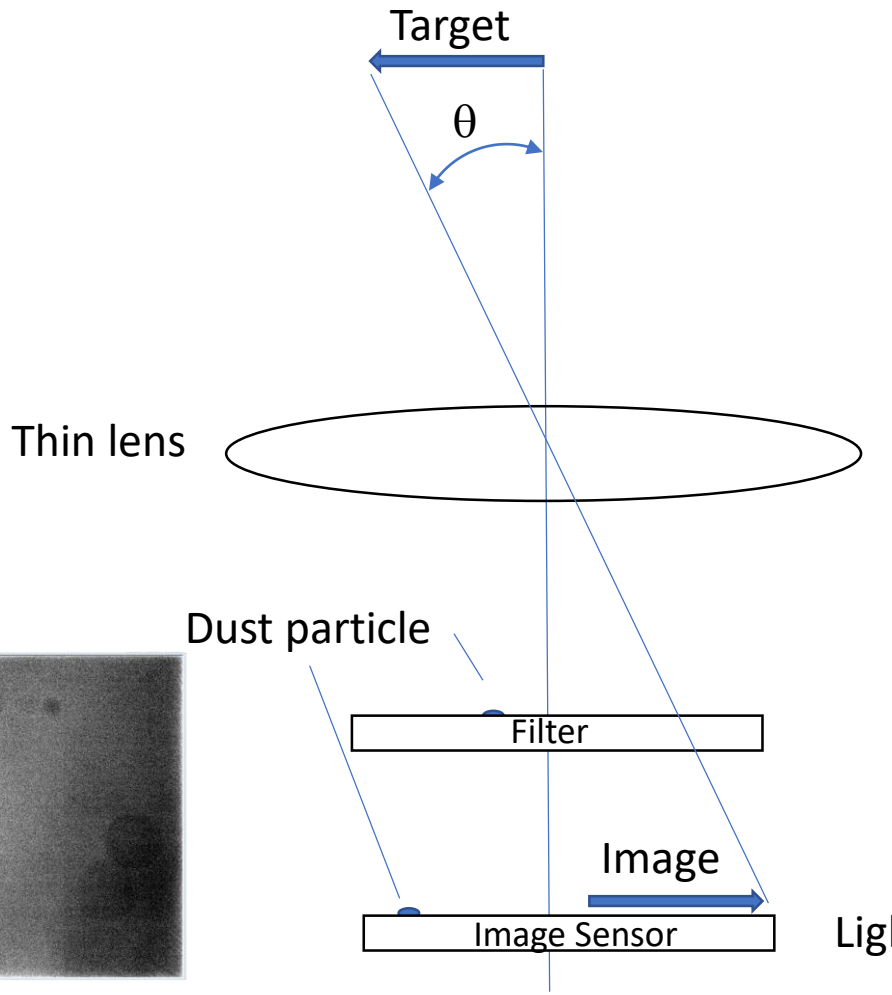
Fixed Pattern Noise

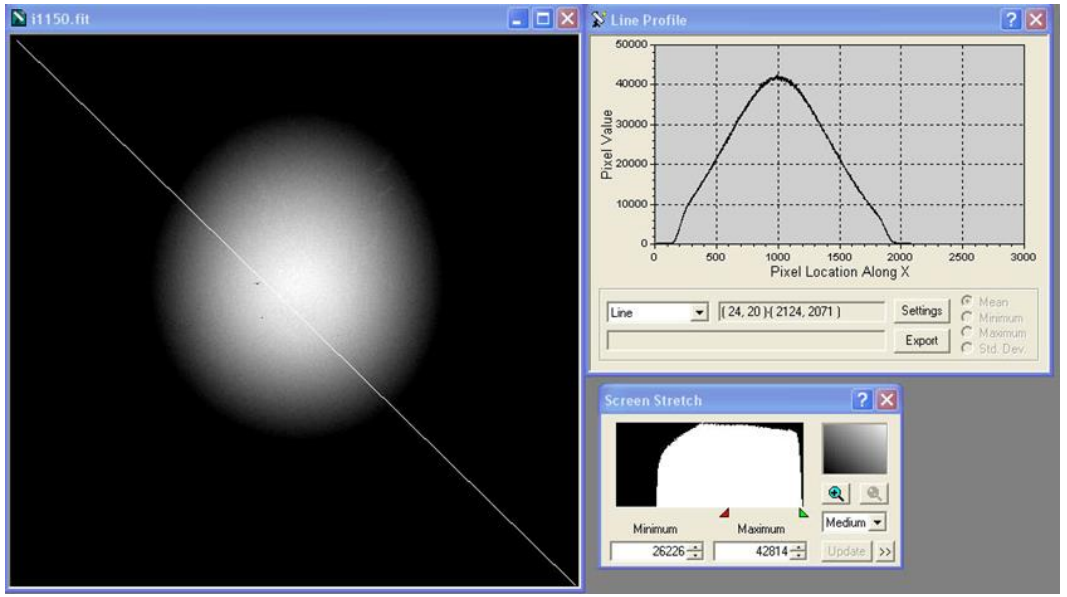
Same Signal Level: Shot Noise vs Fixed Pattern Noise



Each pixel has slightly different light response leading to FPN

Optical FPN





$Cos^4(\theta)$ roll off + mechanical vignetting

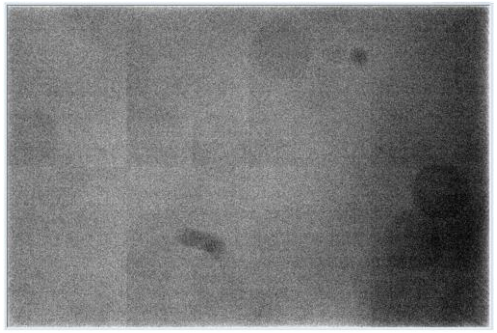
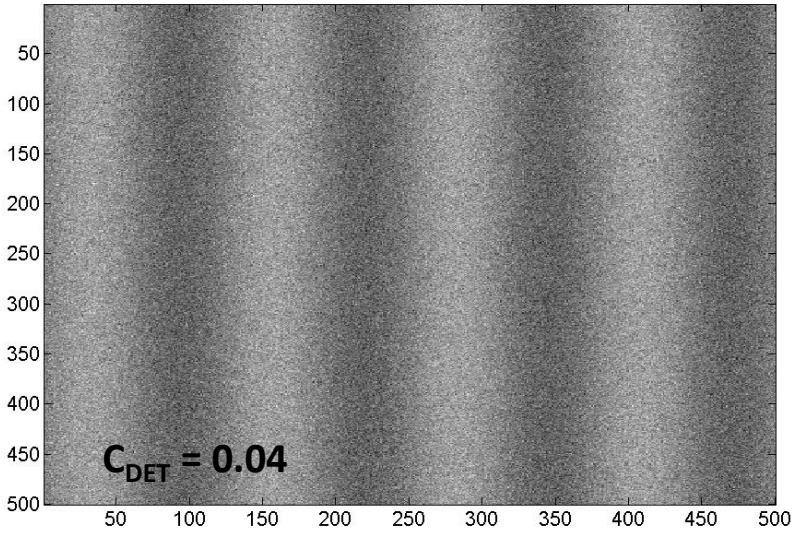


Image of white/featureless background
Shows Optical FPN and Sensor FPN along with dust particles

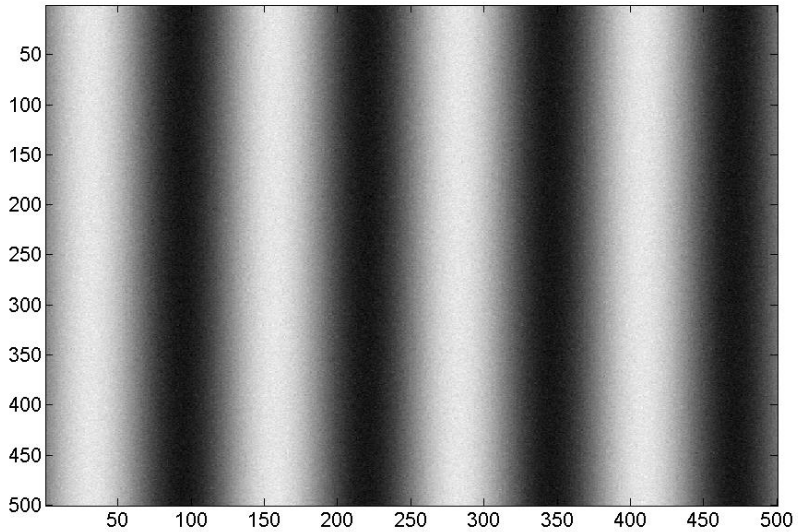
Light flux intensity rolls of as $Cos^4(\theta)$

FLAT FIELDING removes FPN

RAW

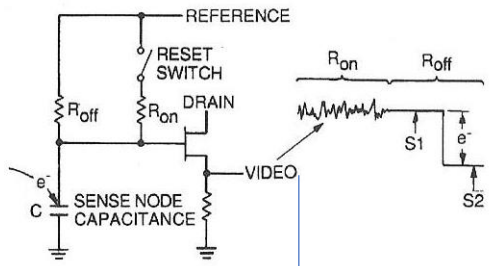


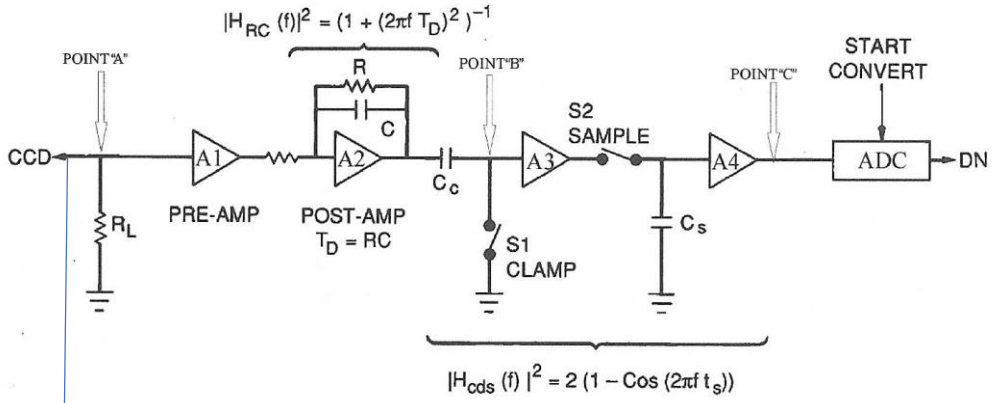
CORRECTED

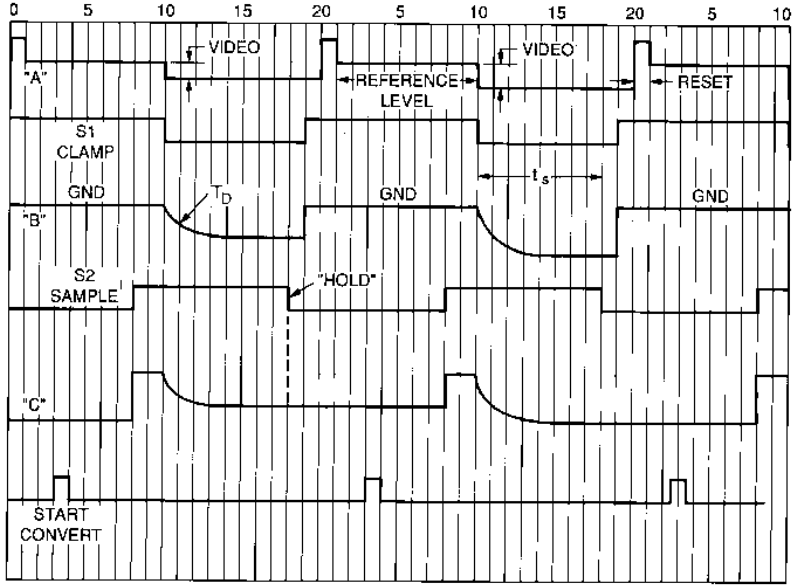


Reset Noise

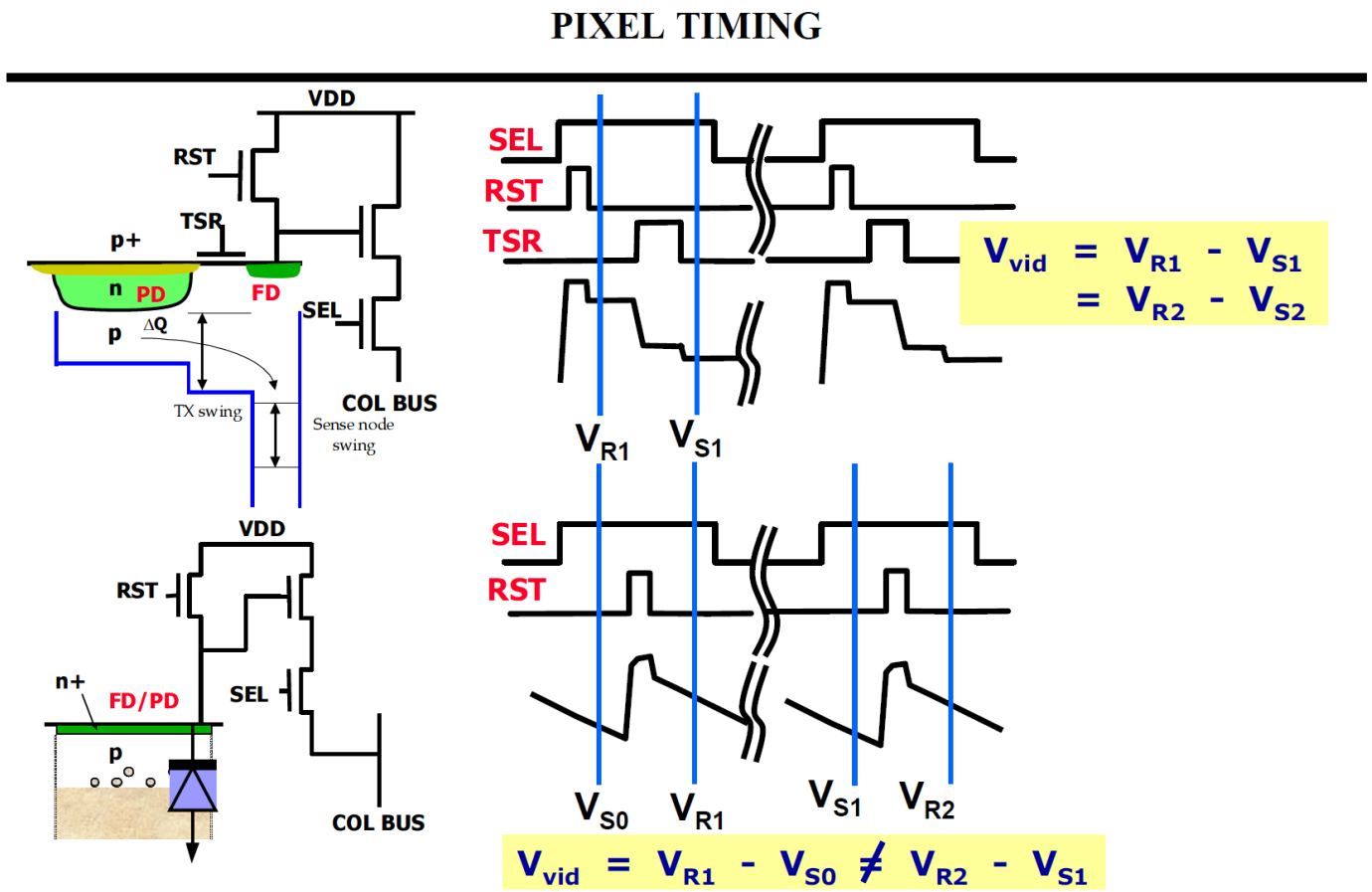
CORRELATED DOUBLE SAMPLER (CDS): Practical Reset Noise Removal for CCD



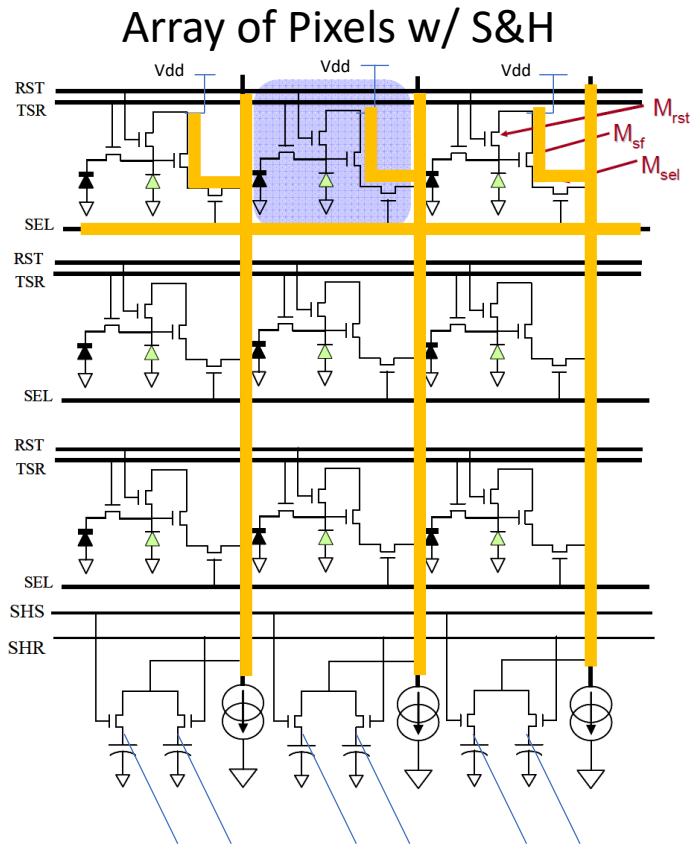




3T Pixel cannot remove Reset Noise: Charge Transfer Pixel can



4T Pixel used in progressive scan



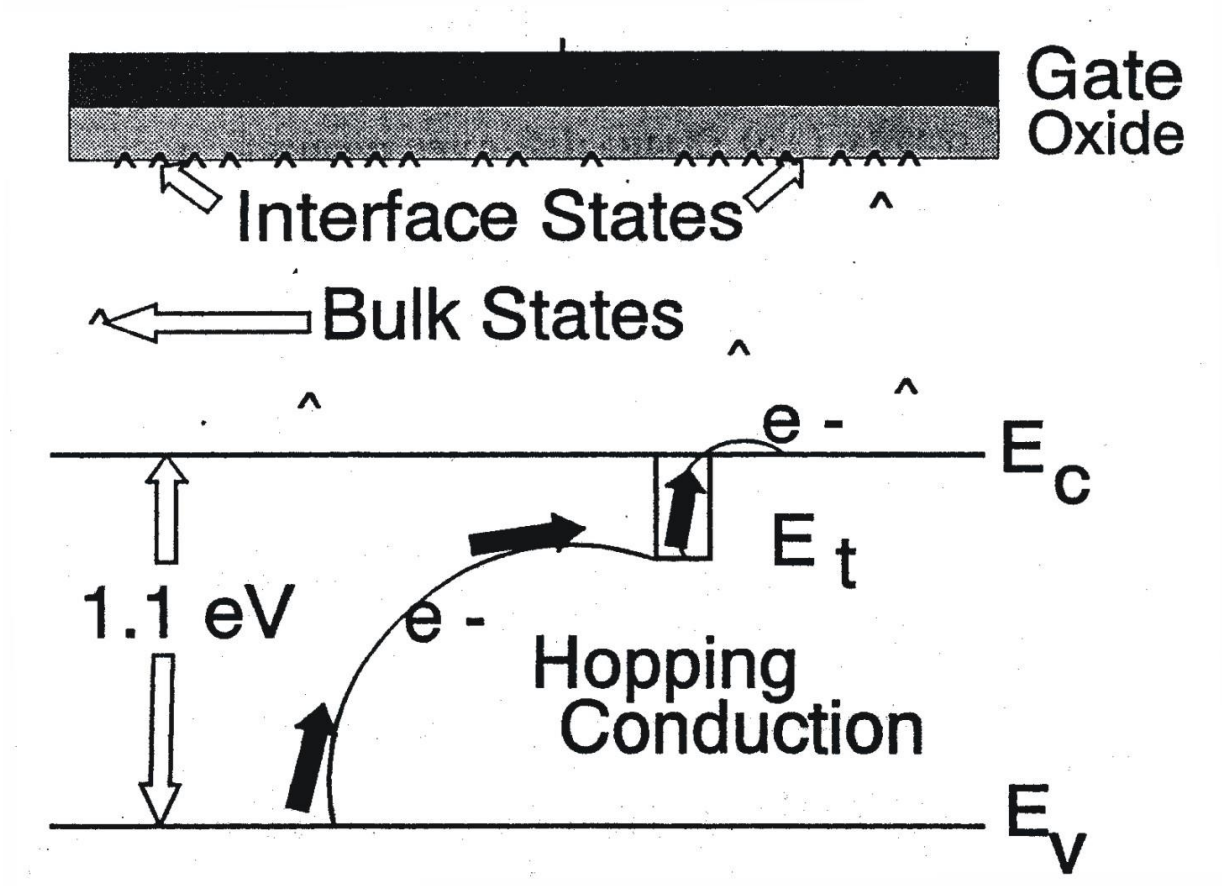
To multiplexer & pipelined A/D subsystem

Correlated signal processing

- Global reset photo region and sense node
- A row at time, sample, digitize and store the reset levels for each pixel
- Integrate and expose
  - First row
    - Reset sense node
    - Transfer charge from photo region to sense node
    - Sample, digitize and store the video levels for each pixel
  - Second row. . etc.
    - Reset sense node
    - Transfer charge from photo region to sense node
    - Sample, digitize and store the video levels for each pixel
- Difference the reset and video levels by computer

Dark Noise

THERMAL DARK CURRENT



DARK CURRENT EQUATION

$$D = 2.5x10^{15} P_S N_{DC} T^{1.5} e^{-E_g/(2kT)}$$

D = (e-/sec/pixel)
P_S = pixel size (cm^2)
N_{DC} = dark current figure of merit (nA/cm^2)
T = operating temperature (K)
k = Boltzmann's constant (8.62×10^{-5}) (eV/K)
E_g = silicon band-gap energy (eV) where:

$$E_g = 1.11557 - \frac{7.021x10^{-4} T^2}{1108 + T} \quad \text{(eV)}$$

DARK CURRENT NOISE SOURCES

DARK CURRENT SHOT NOISE $D_{SN} = (D(e\text{-})\ t_I\ )^{1/2}$

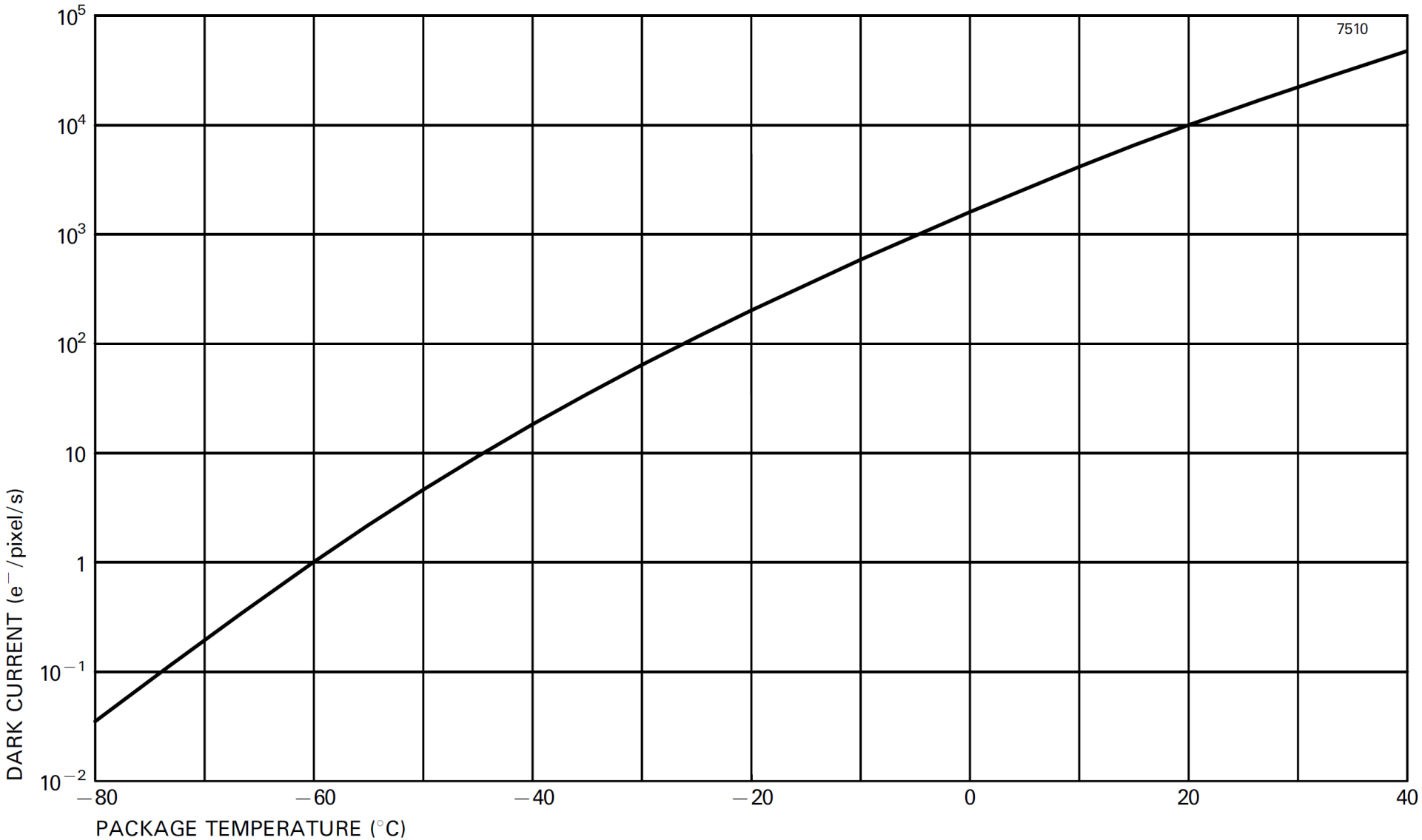
DARK CURRENT FPN $D_{FPN} = D(e-)t_I D_N$

DARK CURRENT FPN FACTOR $D_N = \frac{N_{FPN}(DN)}{S(DN)}$

t_i = INTEGRATION TIME
D_N IS THE DARK CURRENT FPN FACTOR

ONSET OF DARK FPN = $1/D_N^2$

TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



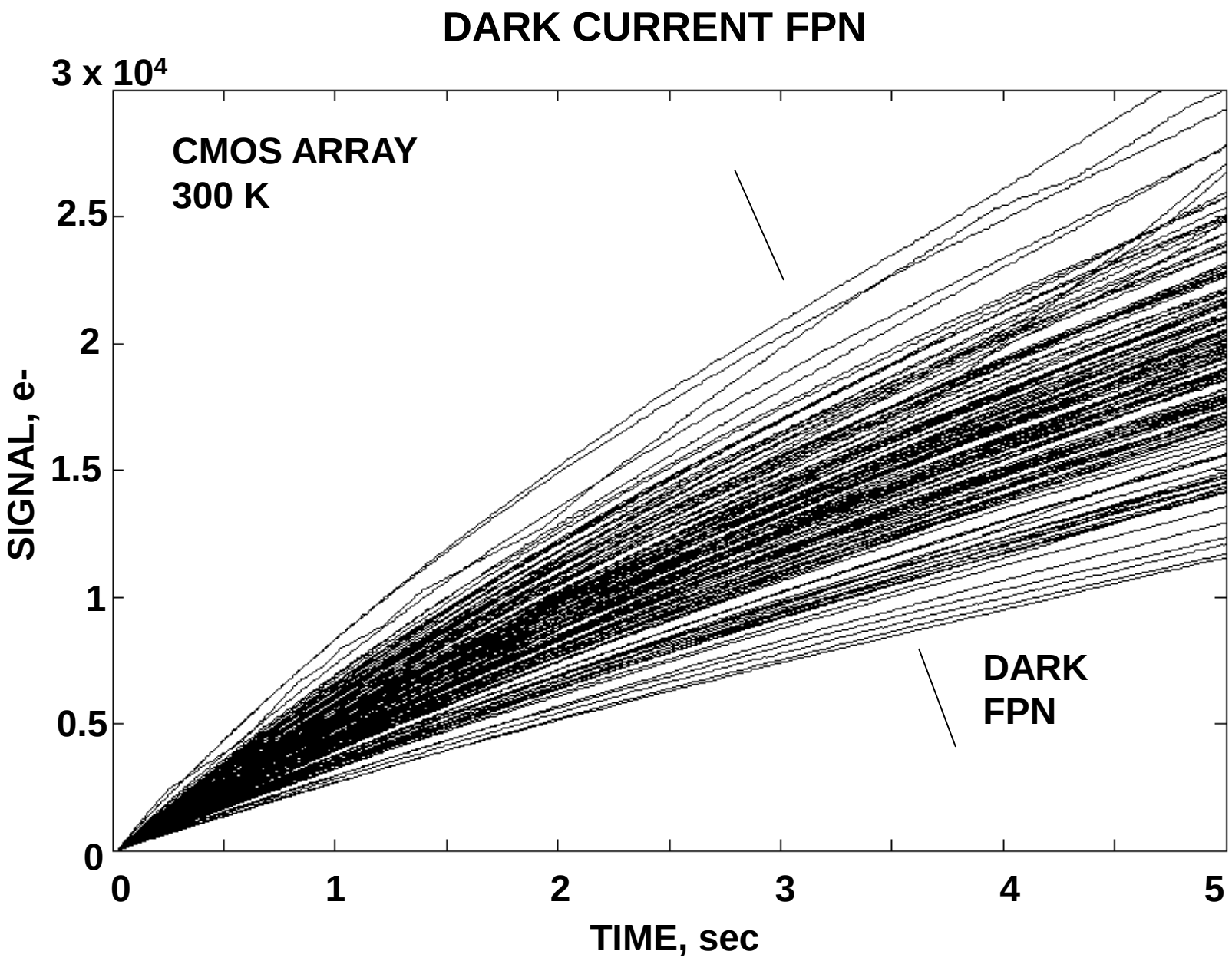
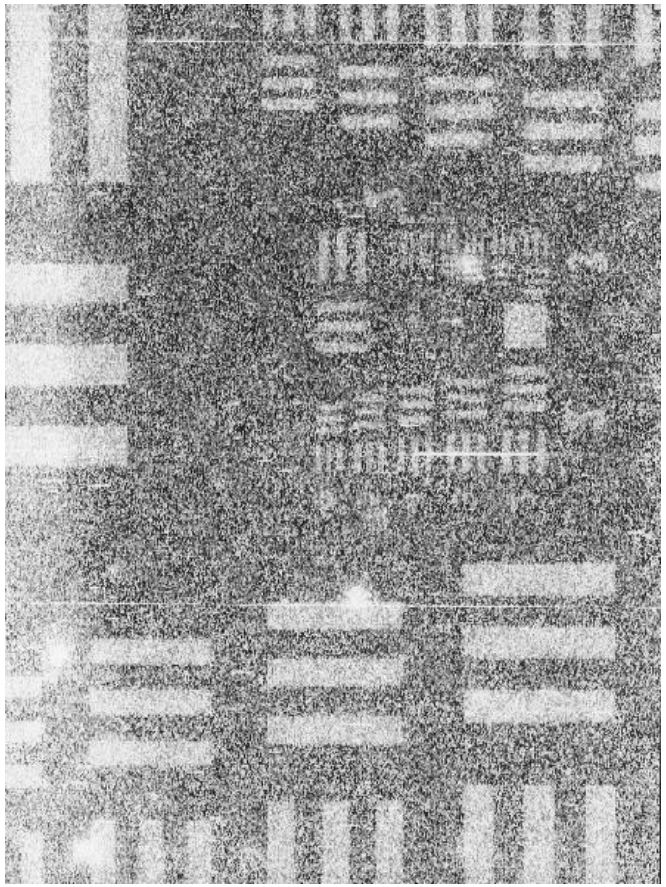
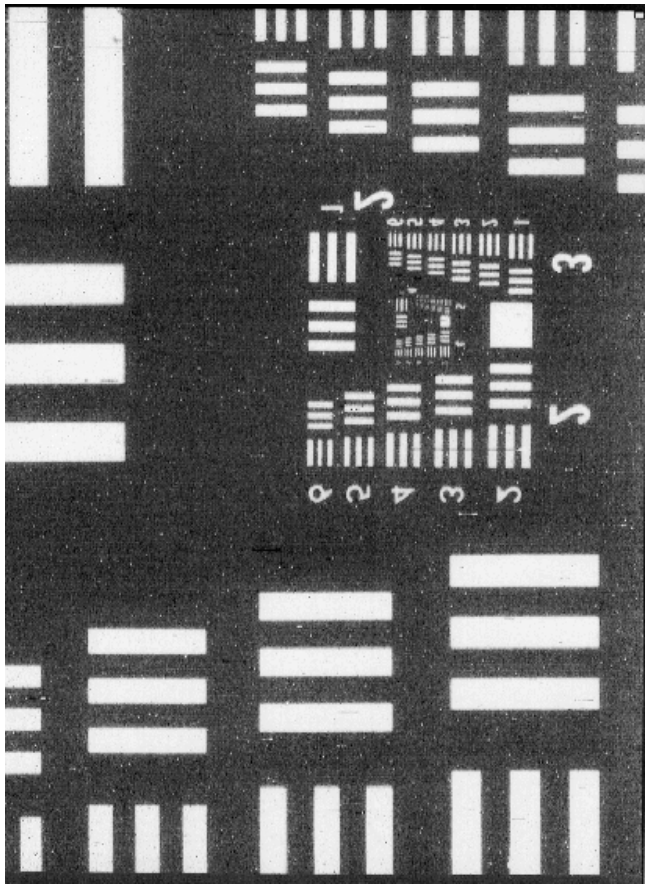

DARK CURRENT FPN
3 x 10^4
CMOS ARRAY
300 K
2.5
2
1.5
1
0.5
0
SIGNAL, e-
DARK
FPN
0
1
2
3
4
5
TIME, sec

Image Degraded by Dark Signal NonUniformity

(2 MINUTE EXPOSURE)



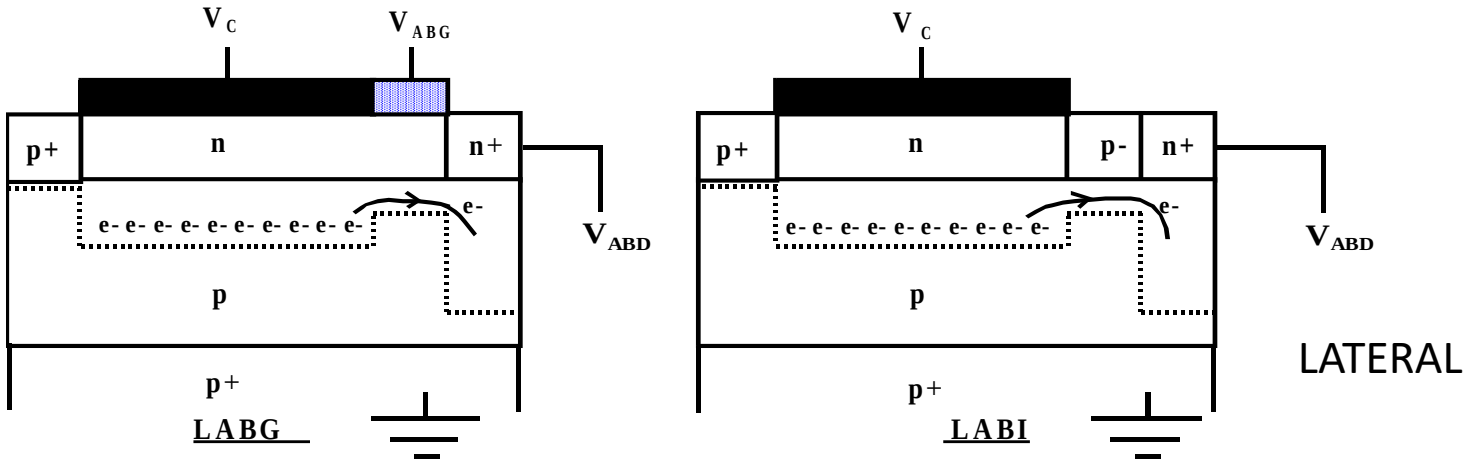
RAW IMAGE



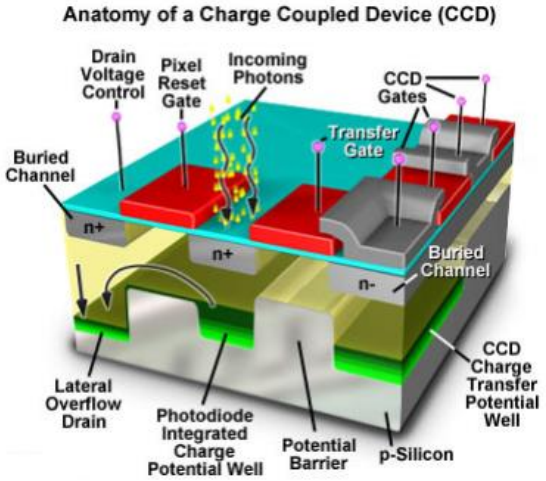
DESPIKED IMAGE
(subtract Dark Frame from Image)

Blooming

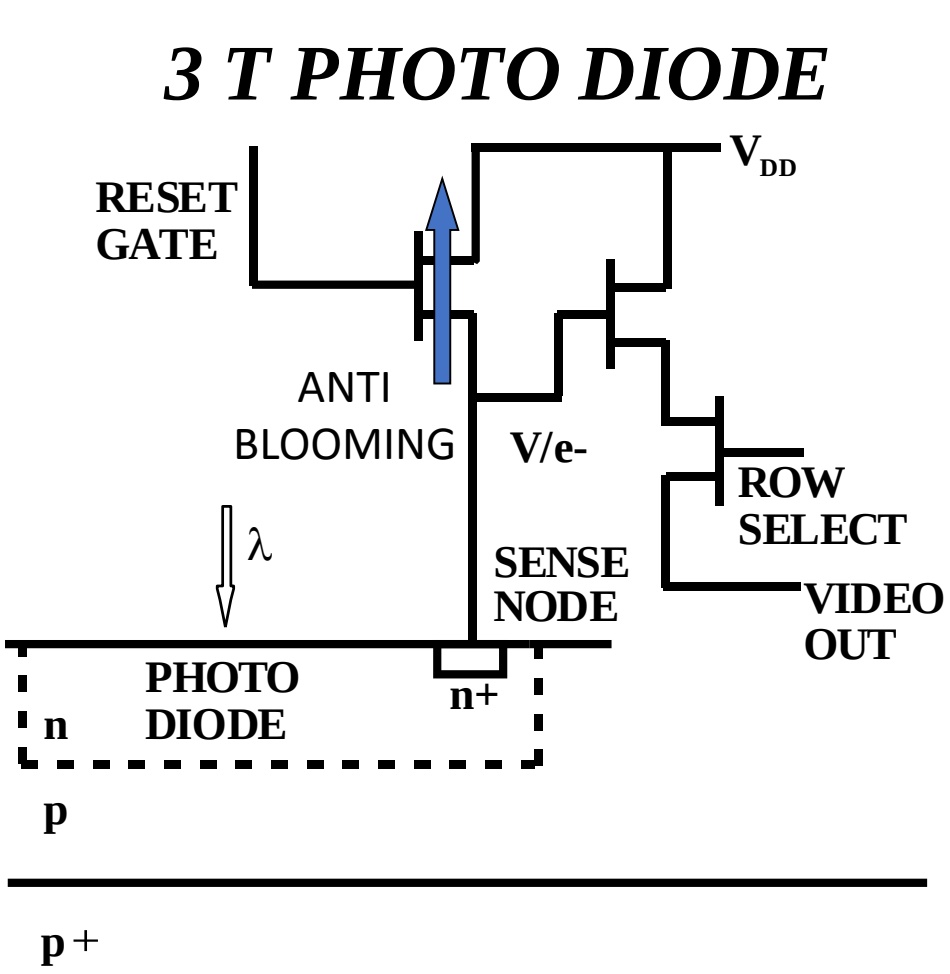
CCD ANTIBLOOMING

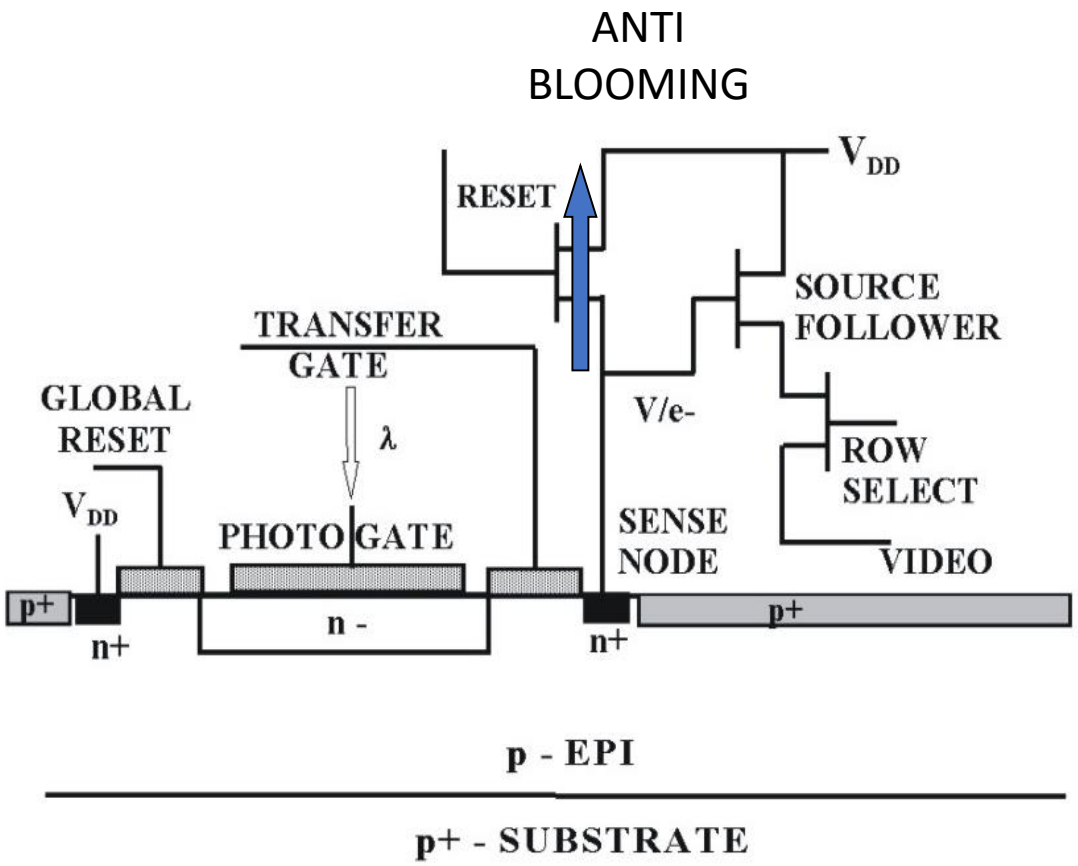


Bloomed Anti-Blooming



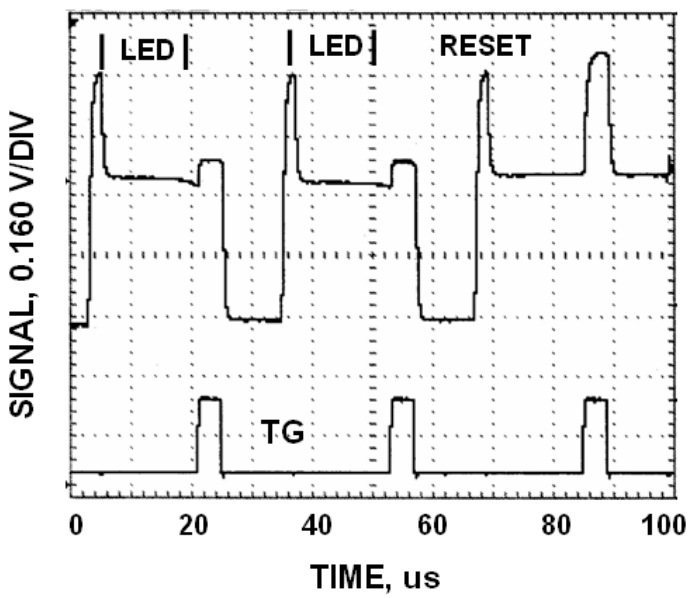
CMOS ANTIBLOOMING

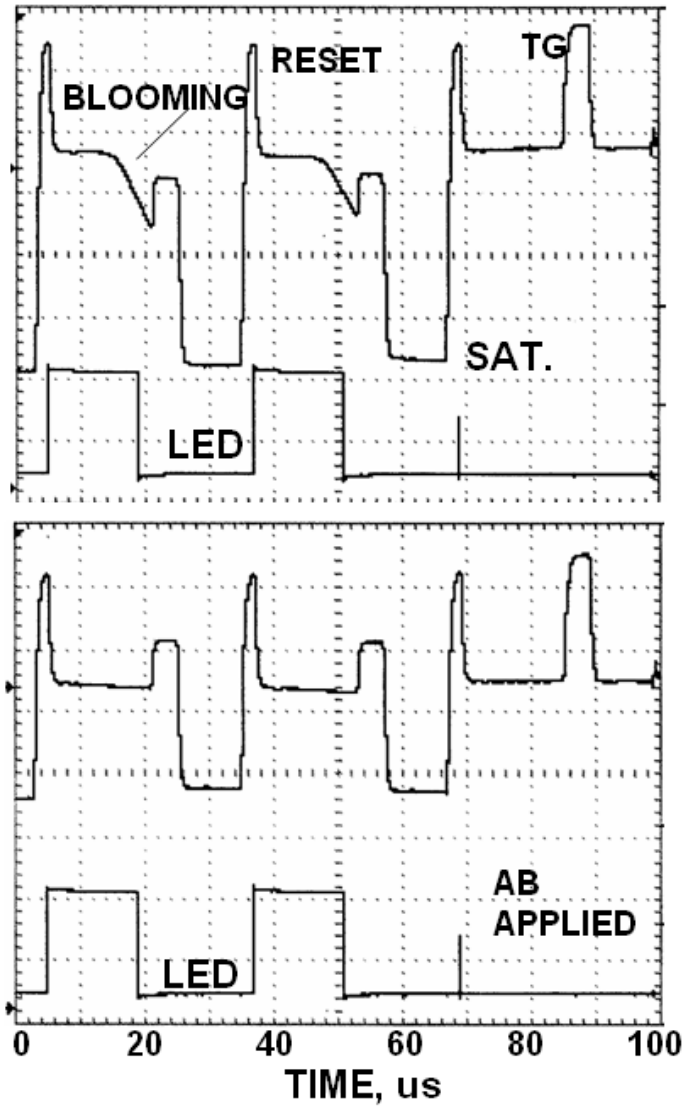




CMOS SENSE NODE BLOOMING
(CHARGE COUPLED PIXELS)

CMOS SENSE NODE BLOOMING
(CHARGE COUPLED PIXELS)



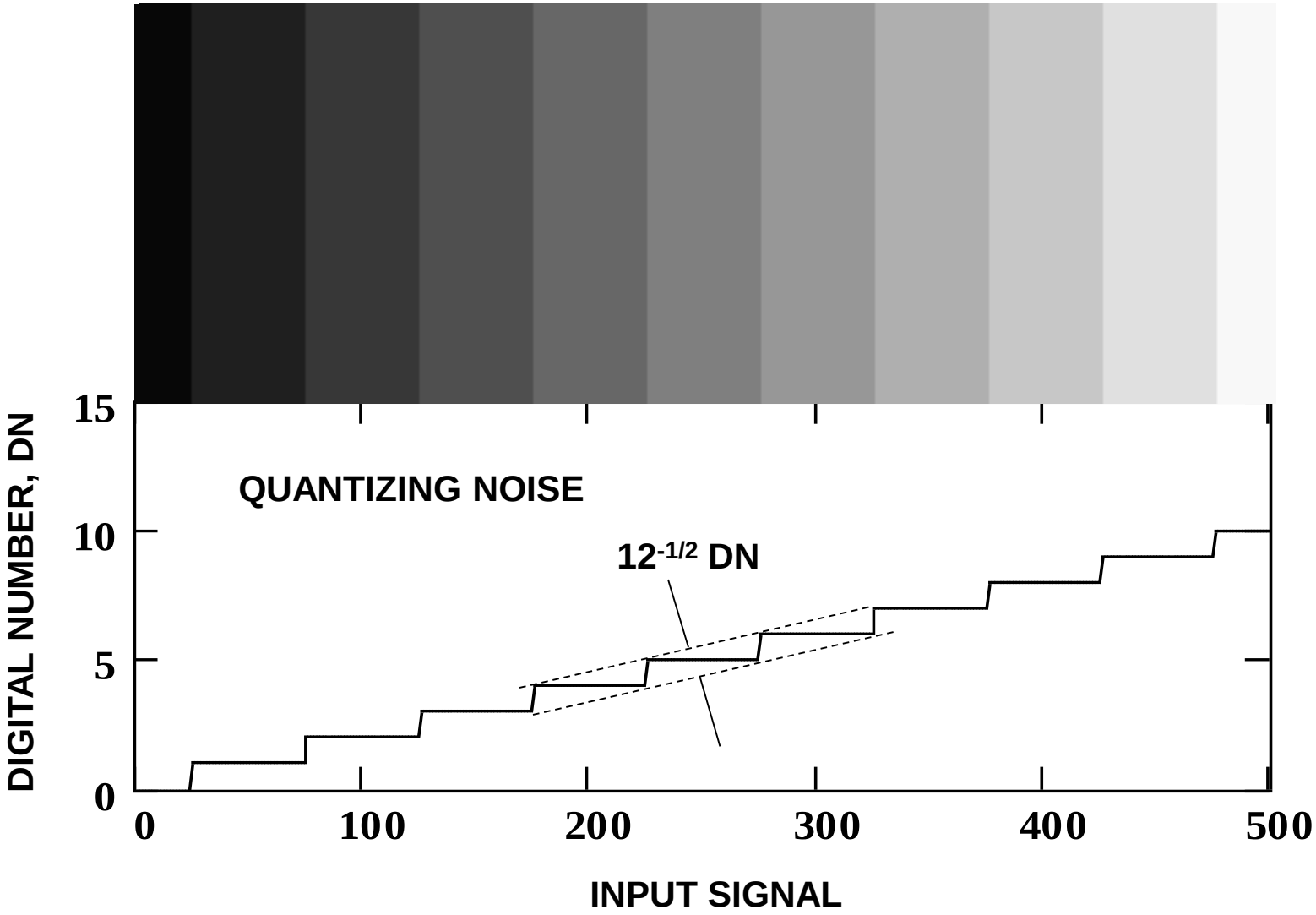


SENSE NODE
BLOOMING
LOW LEVEL

ANTI BLOOMING

Quantizing Noise

ADC QUANTIZING NOISE



ADC QUANTIZING NOISE

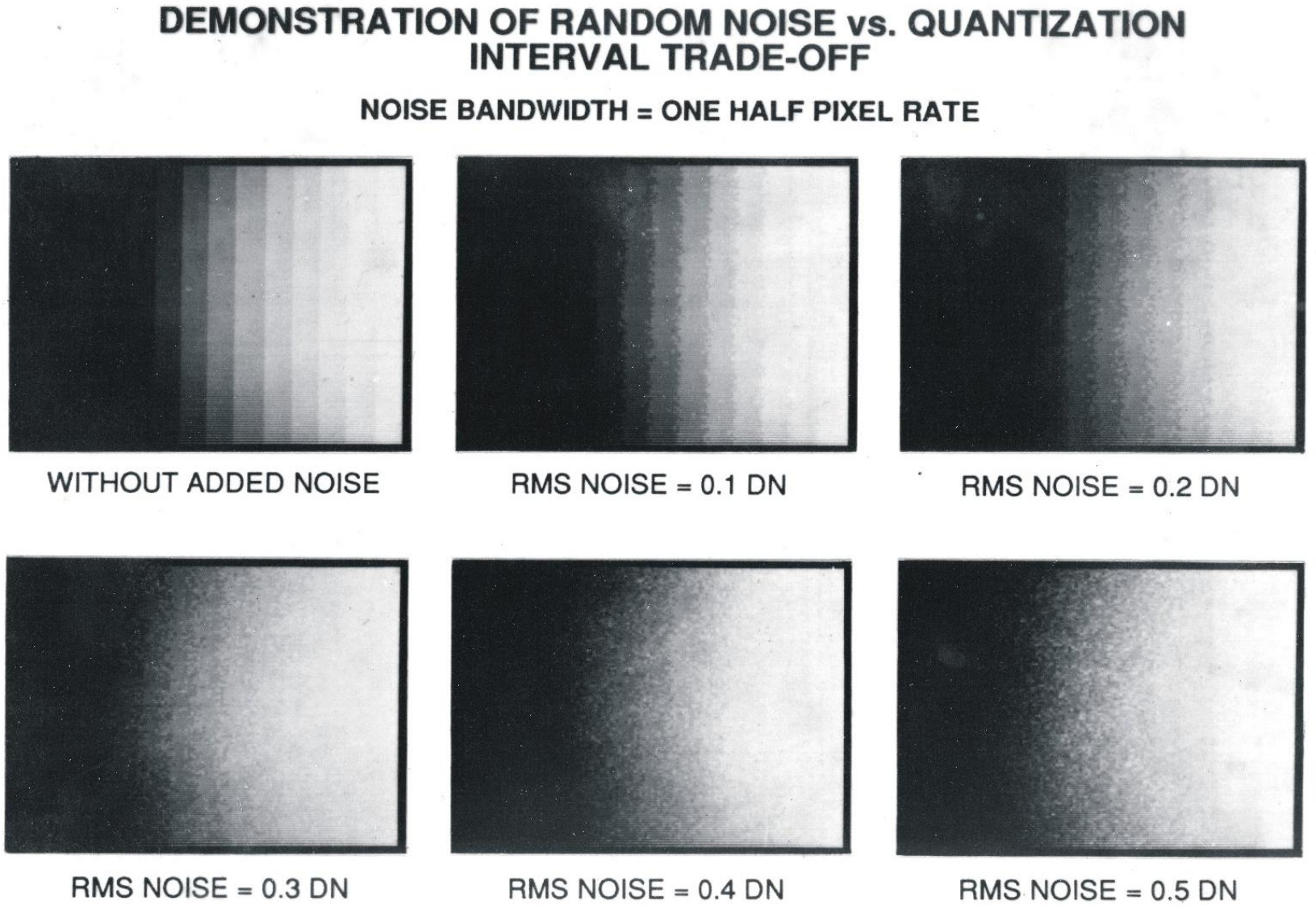


Image Quality vs Bit Depth

10 BIT

5 BIT

4 BIT

10 BIT CMOS VGA
10 BIT TO 5 BIT

Residual Image

Residual Image

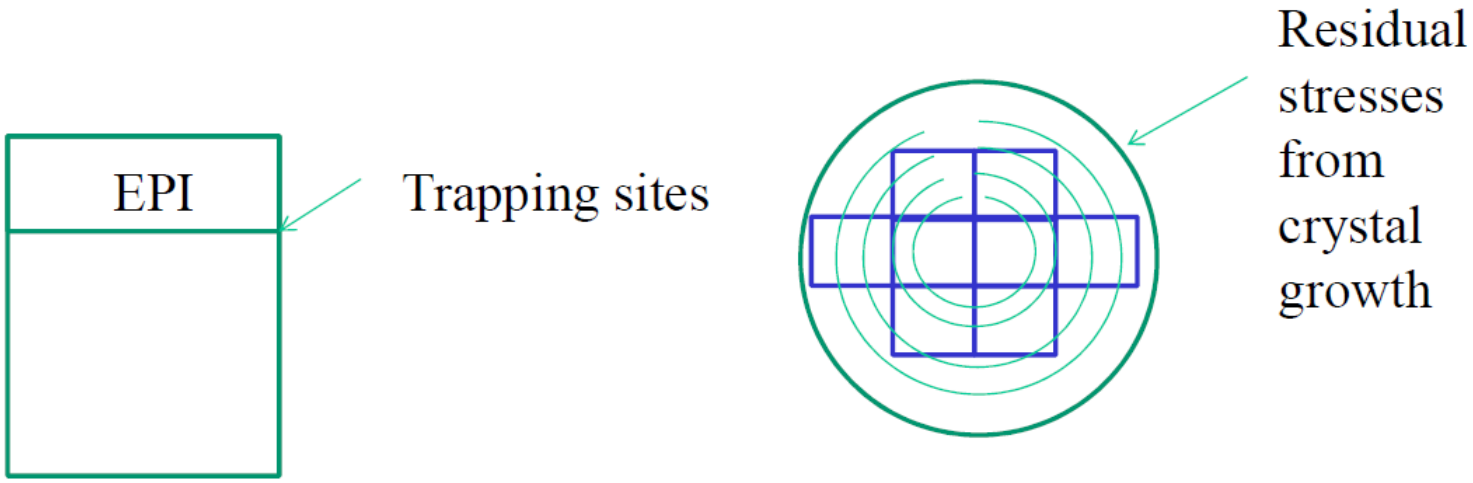
Image

5 Minute Dark
Immediately
following
image

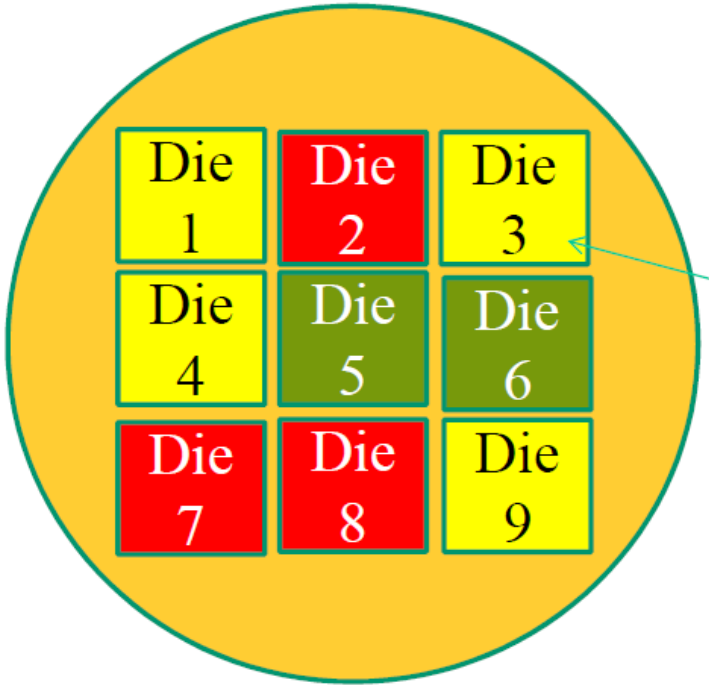
5 Minute Dark
One hour
following
image

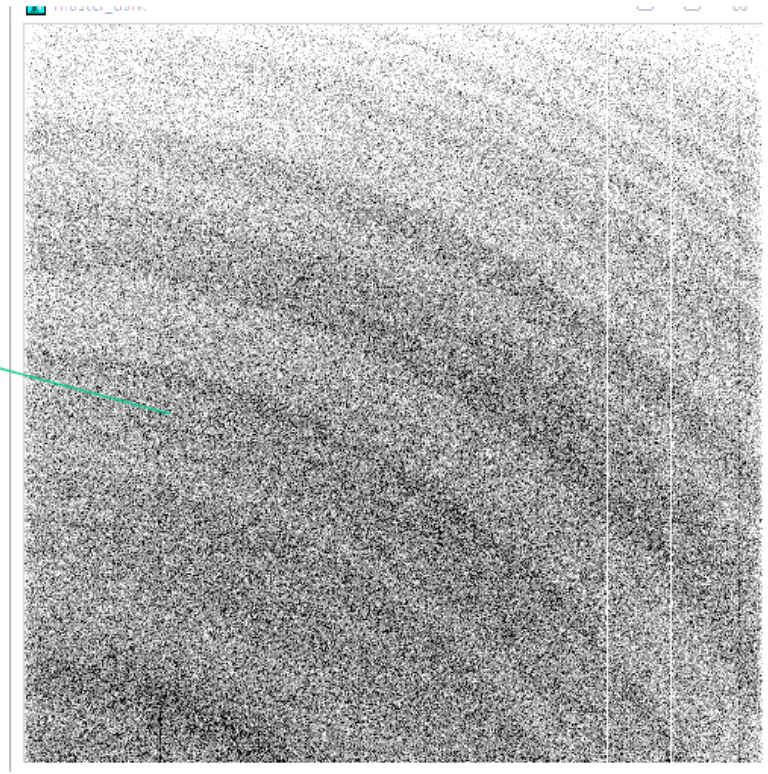
Residual Image: Charge Trapping Sources

- Epi interface trapping sites
  - Spectral dependence
- Stress-induced trapping sites in lattice from crystal growth process
  - Swirling shapes in darks
- Random bulk defects in crystal lattice
  - No spectral dependence or swirling shapes



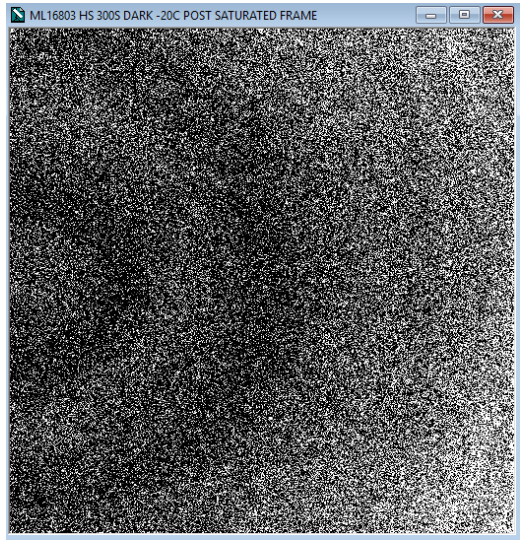
Wafer Mapping Example



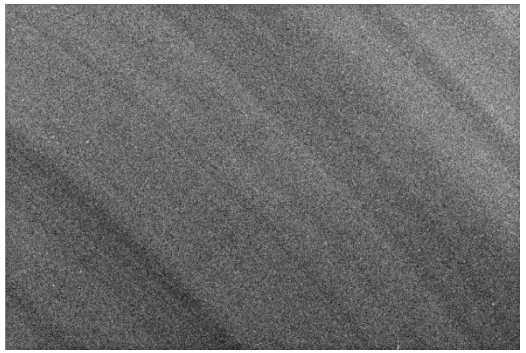


Careful wafer mapping of where die were on wafer shows circular trap distribution indicating related to crystal growth process

Kodak KAF16803



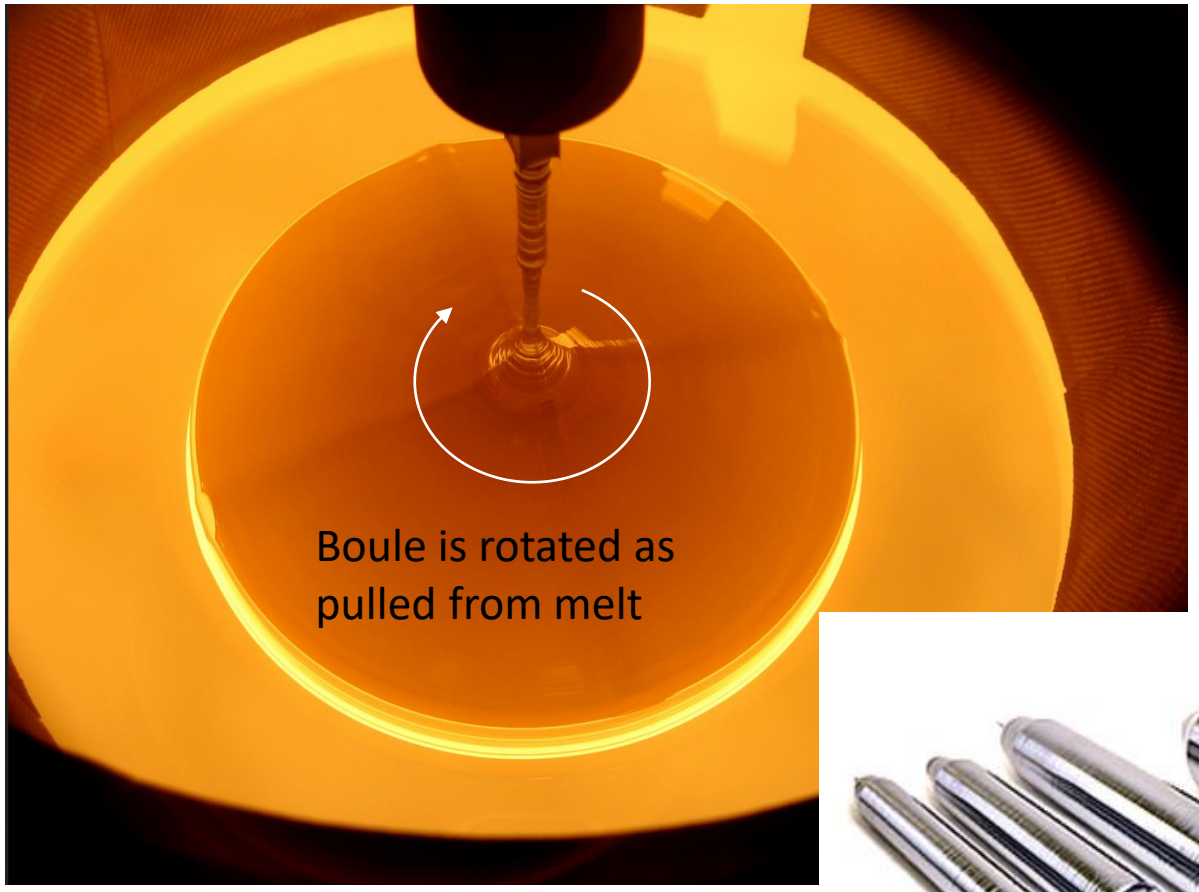
ON-Semi KAF16803



Kodak KAF3200

Light-Flooded Dark Images reveal nonuniform trapping site distribution

Silicon Boule Manufacturing (Czochralski Process)



Microstresses induced by rotation

Wafers sliced from Boule

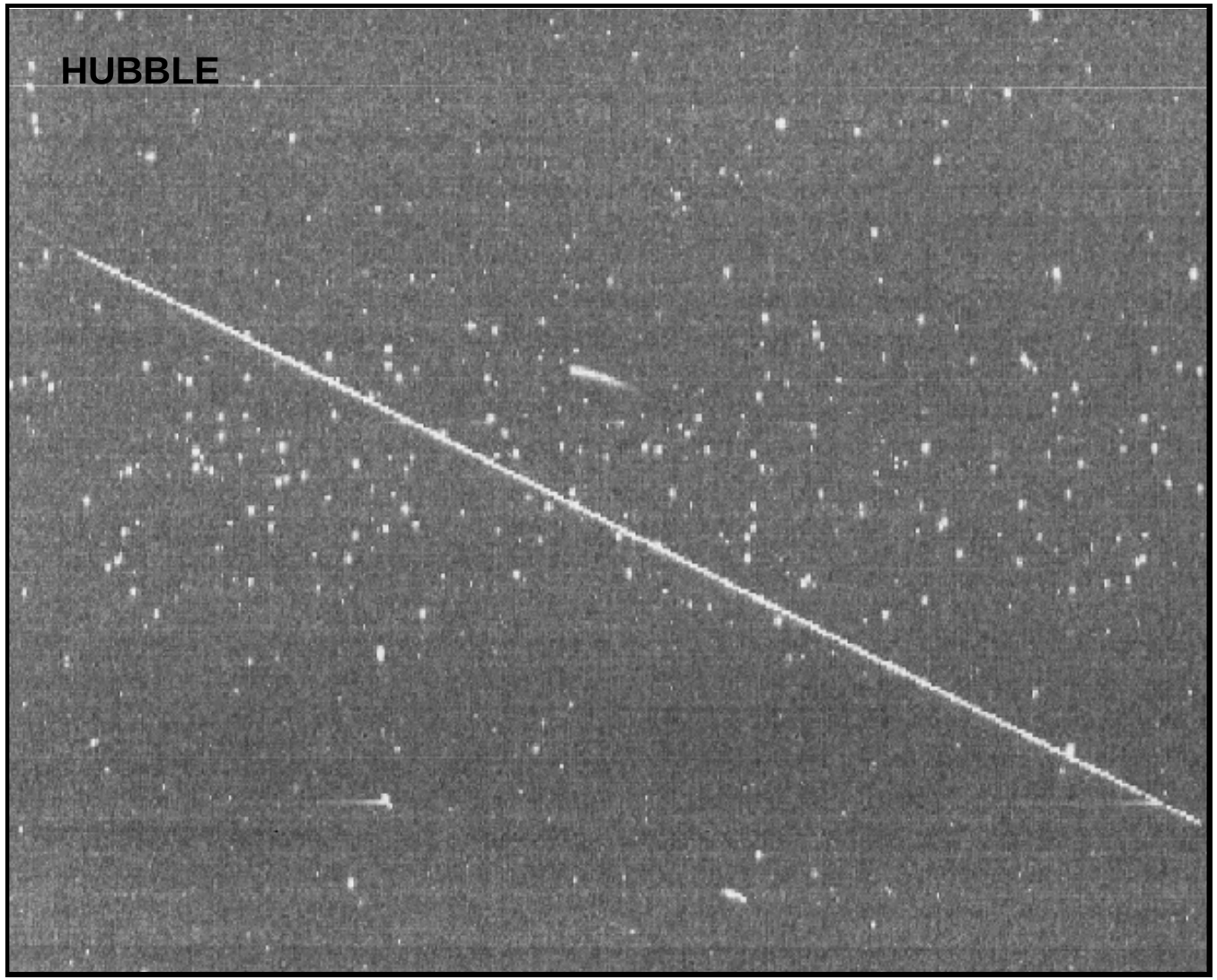
High Energy Particles

COSMIC RAYS - SOLAR PARTICLES

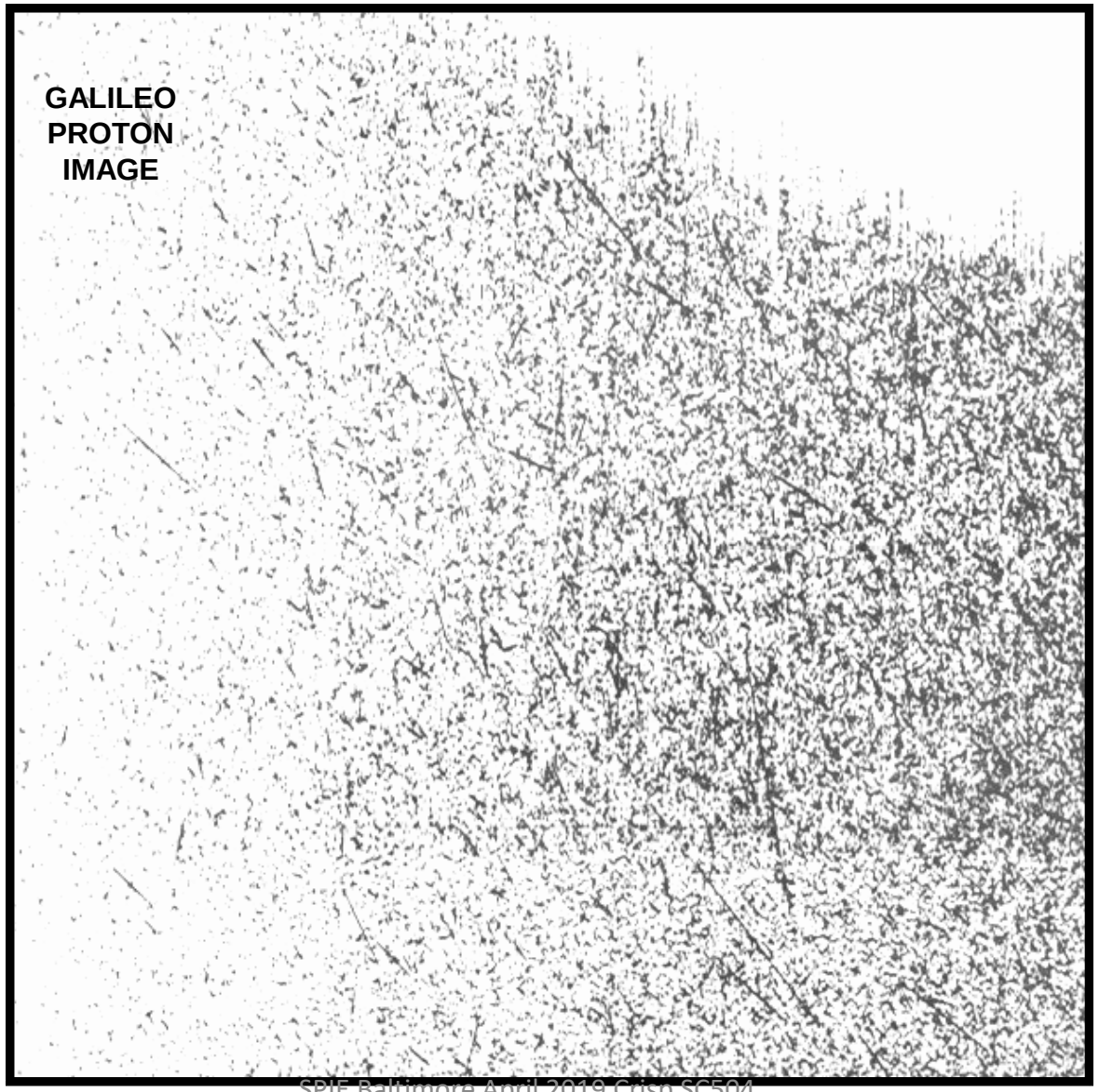
Random Radiaton hits are common with long exposures & non-terrestrial imaging

If image target is non-changing (ie Astronomical), combining multiple images using sigma-reject algorithm can eliminate random hits

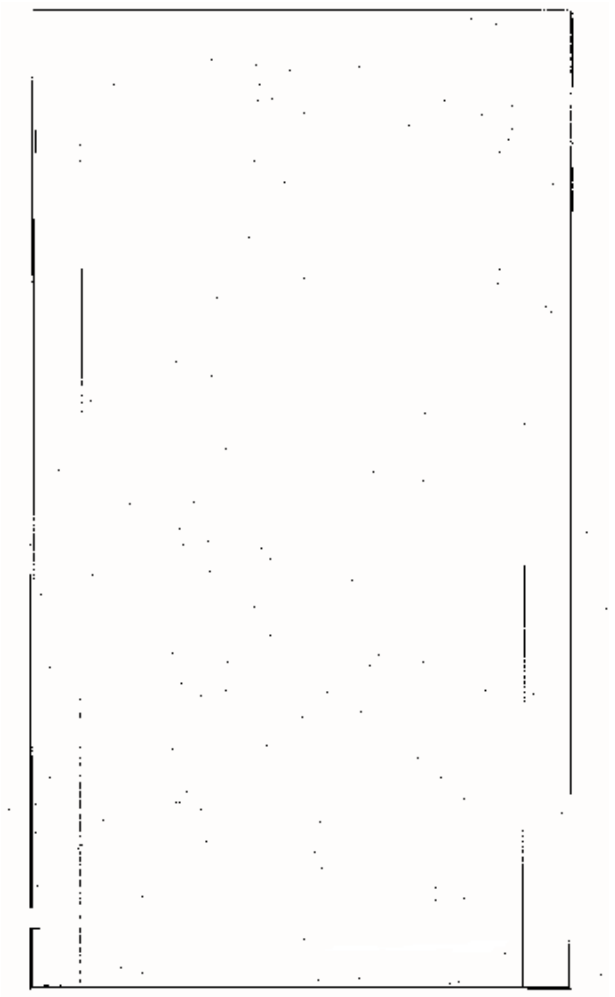
If sensor has RBI/Charge Trapping issues, radiation hits may accumulate via trapping & decay slowly for cooled sensors



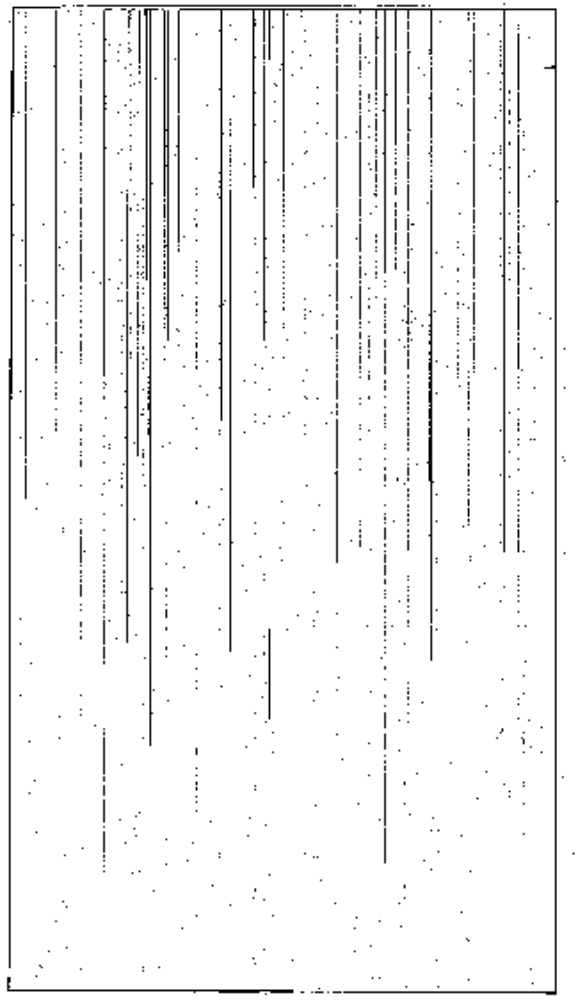
COSMIC RAYS - SOLAR PARTICLES



RADIATION INDUCED DARK CURRENT SPIKES



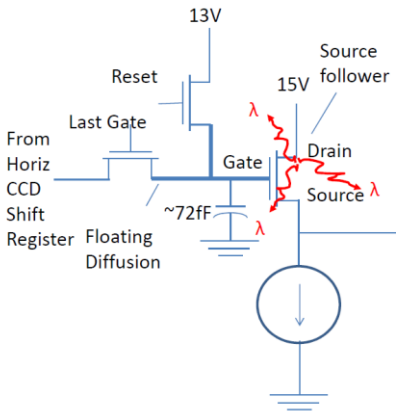
GALILEO BEFORE LAUNCH

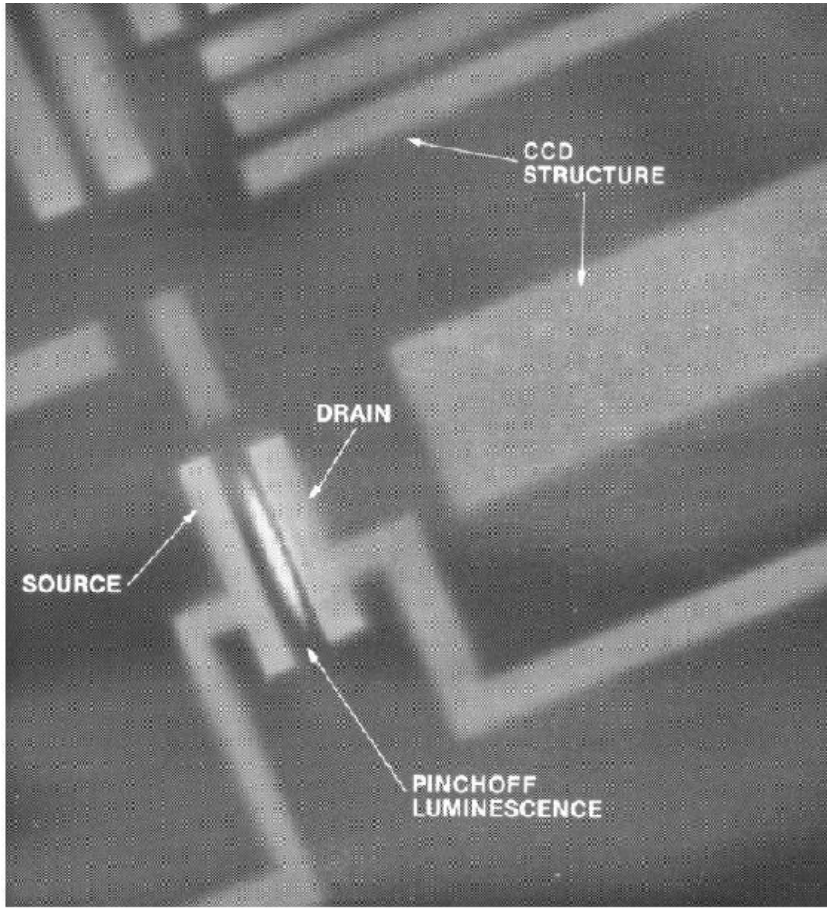


AFTER 1.5 YEARS IN SPACE

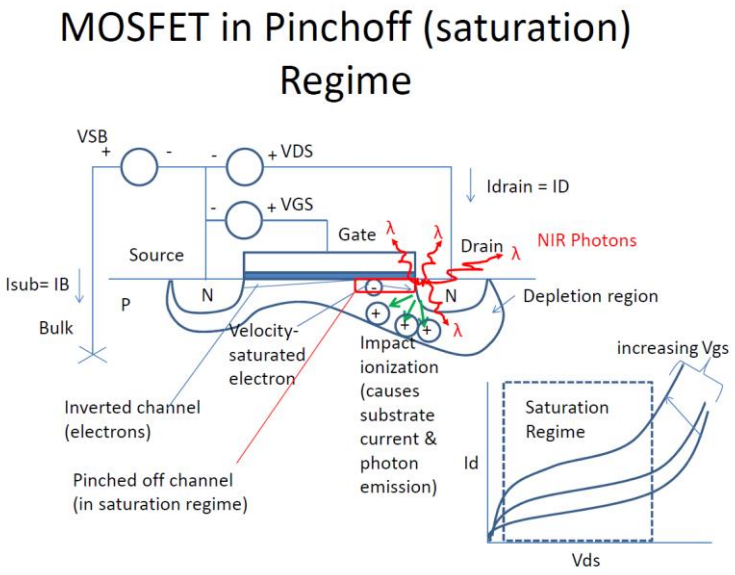
Amplifier Luminescence

Amplifier Luminescence





Generic Amplifier Luminescence Considerations



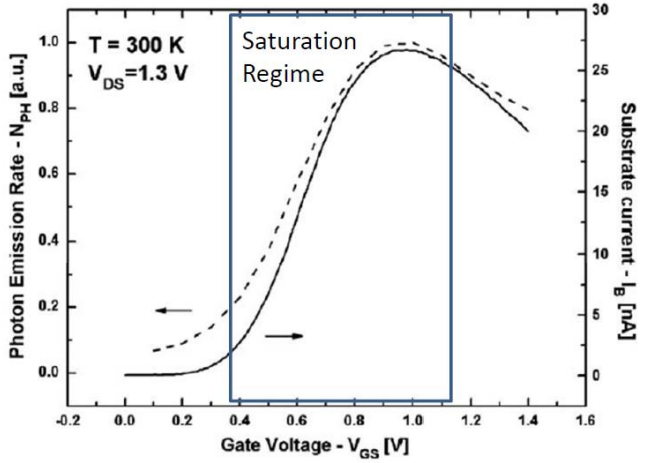


Fig. 1. Photon emission rate (dashed curve) and substrate current (solid curve) as a function of gate bias at $V_{DS} = 1.3$ V.

Saturation regime: VDS > (VGS – VT)

Pinchoff Regime (in dashed box)

Significant emission at wavelengths detectable by a silicon CCD

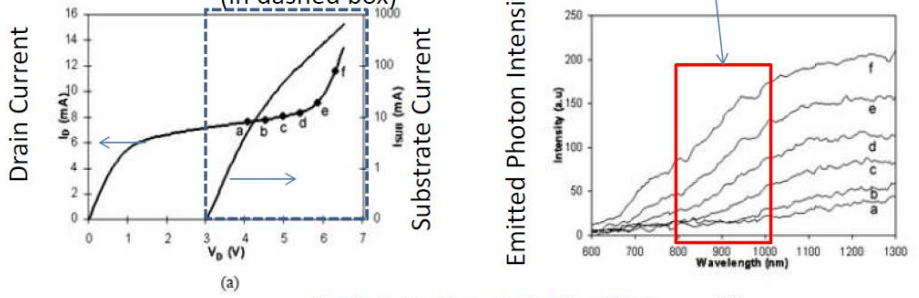


Fig. 11: (a) I_D and I_{sub} versus V_D at $V_{GS} = 3V$ and (b) emission spectra at operating points a – f for 1.0μm gate length nMOSFET (nMOS1) [16]

NIR Light Transmittance Through Silicon

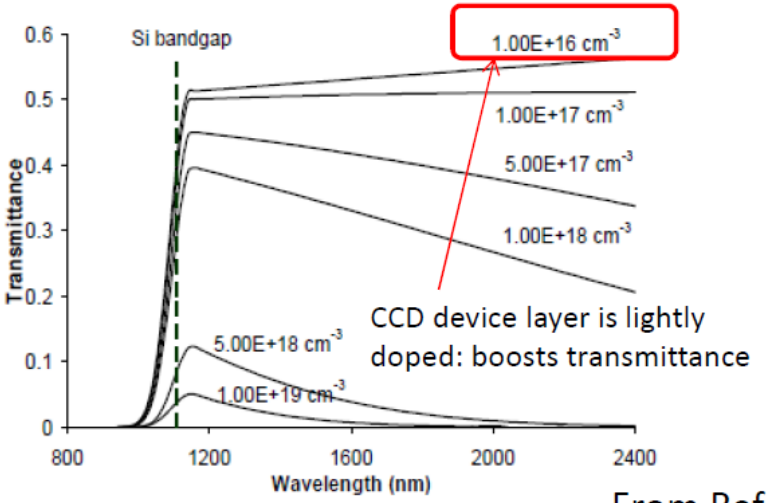


Fig. 2a: Photon transmittance of 500 µm p-Si for different doping concentrations

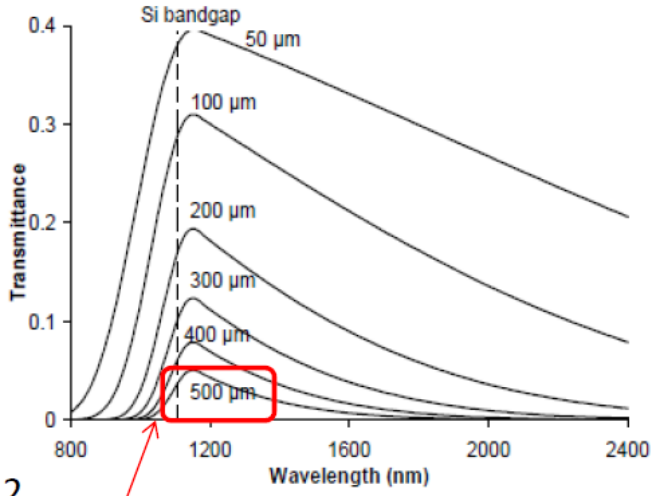
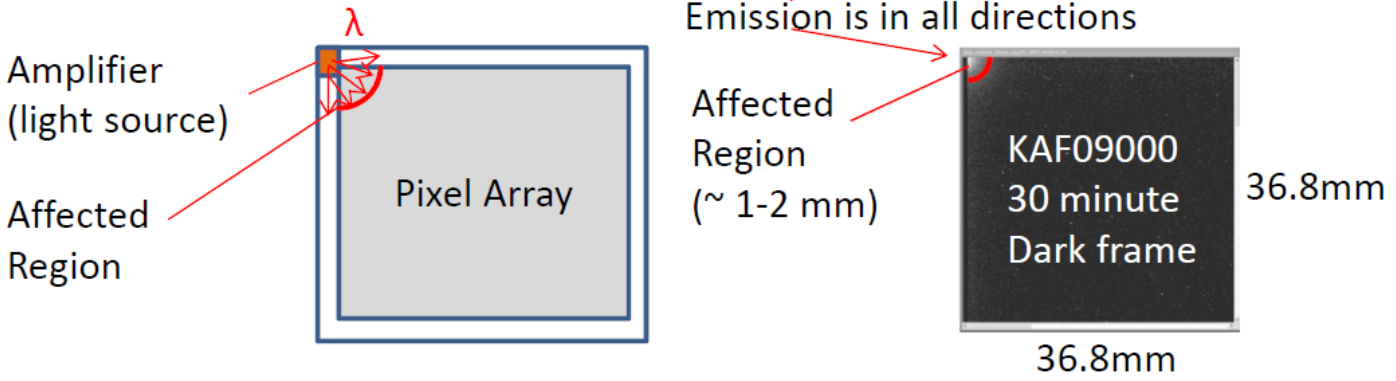


Fig. 2b: Photon transmittance of p-Si doped at 10^{19} cm^{-3} for different backside thicknesses

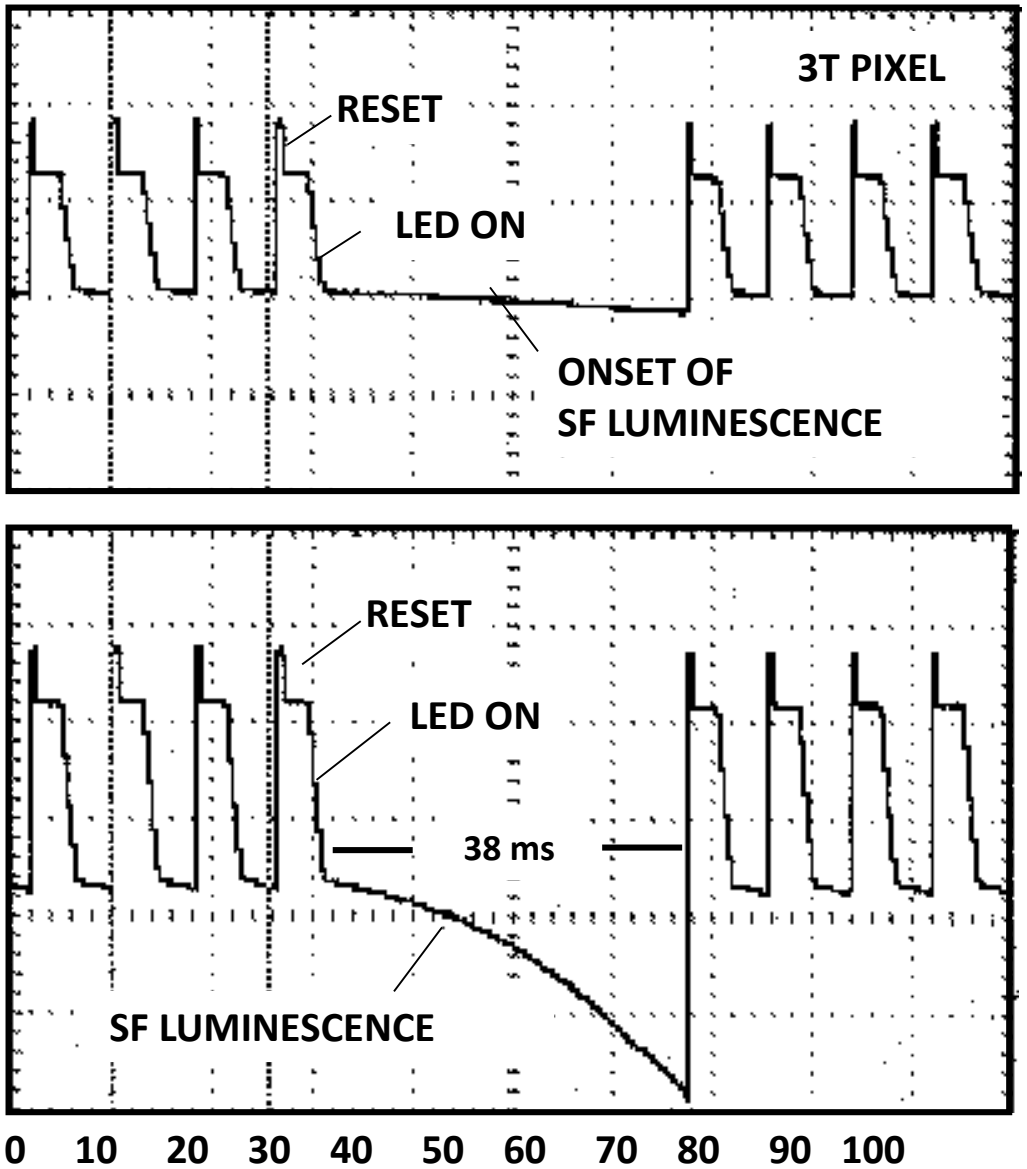
From Ref 2

CCD Example

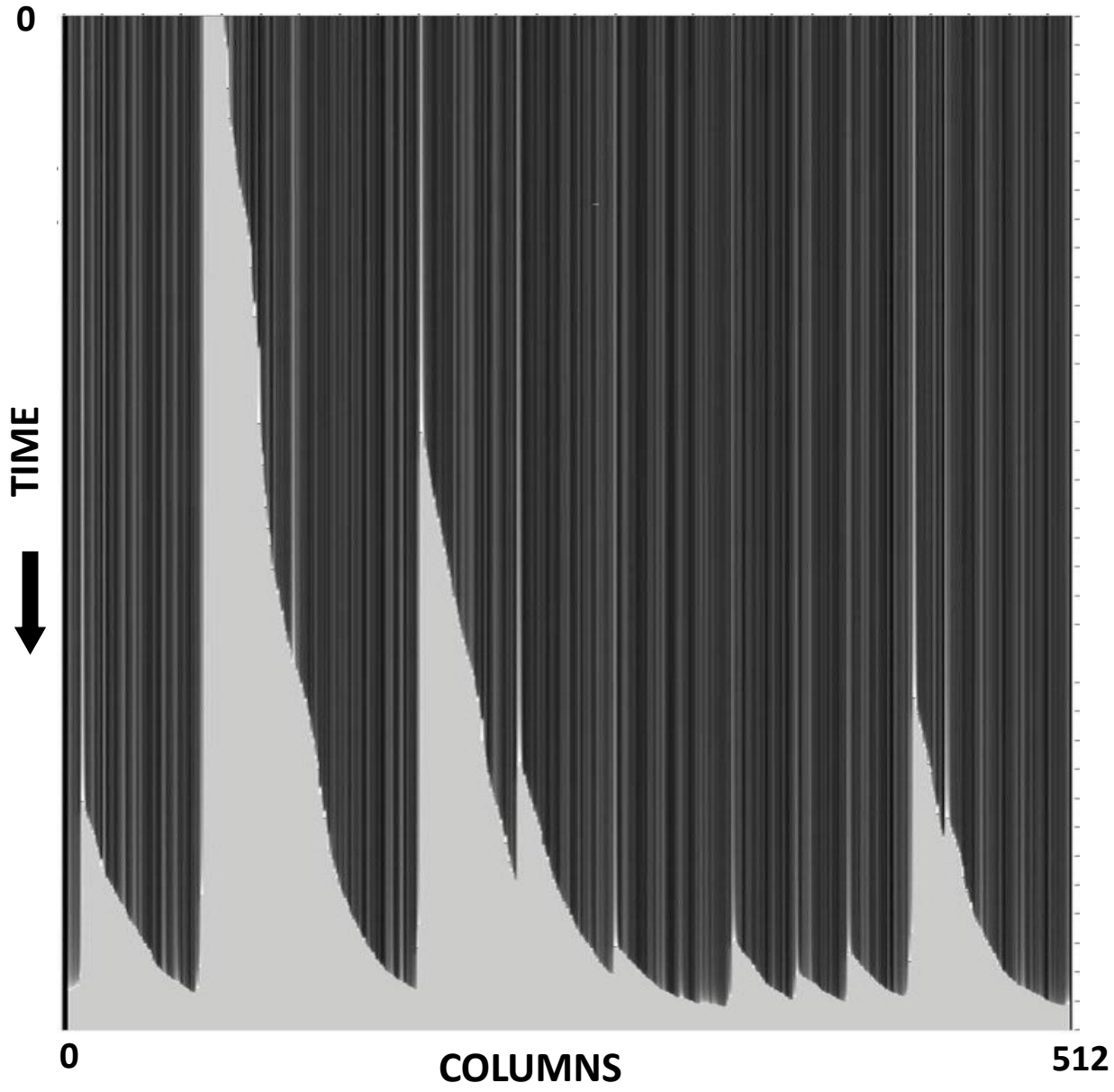


The luminescence may be transient but with RBI will remain in subsequent images via trap decay like RBI

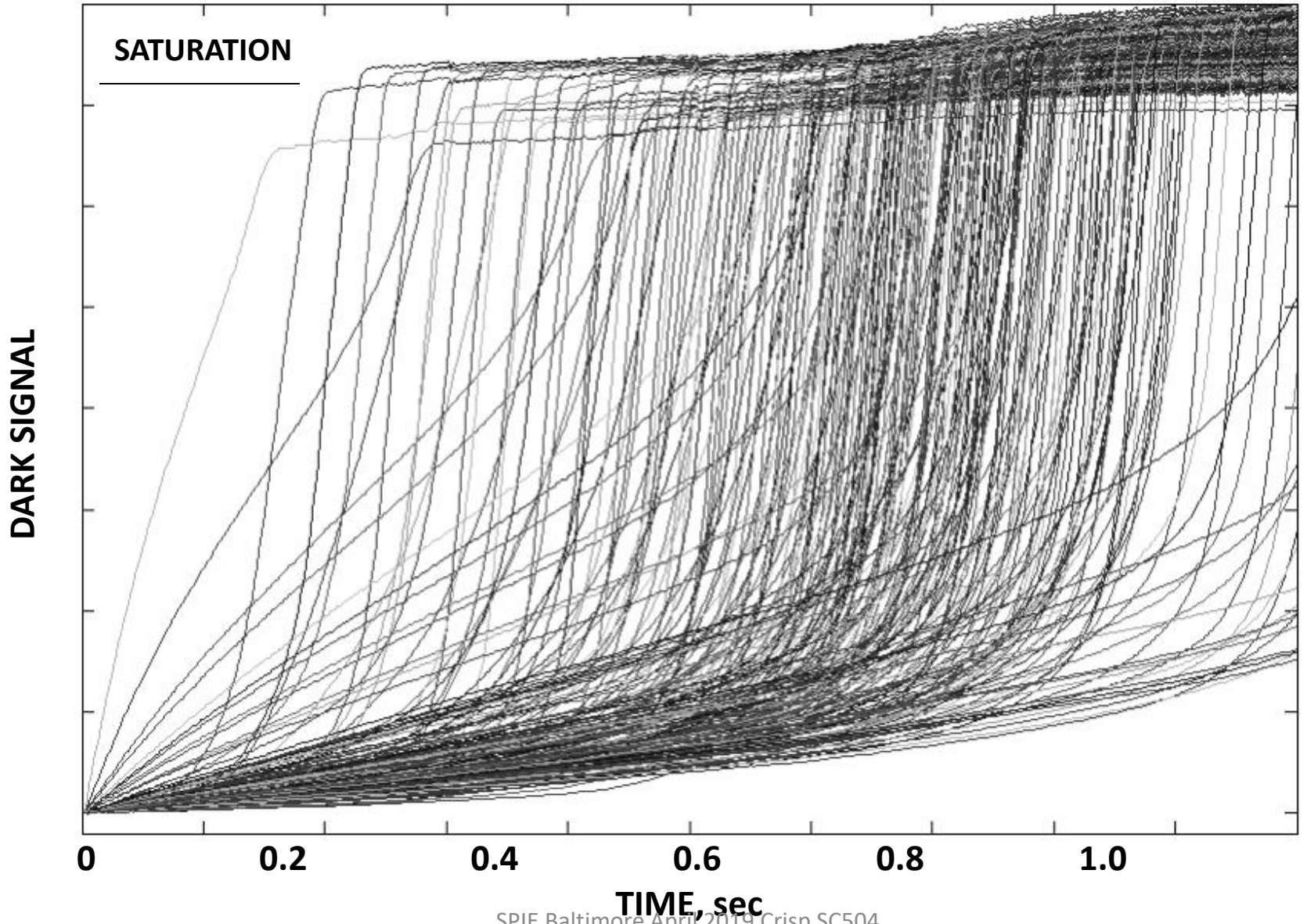
CMOS LUMINESCENCE



CMOS LUMINESCENCE



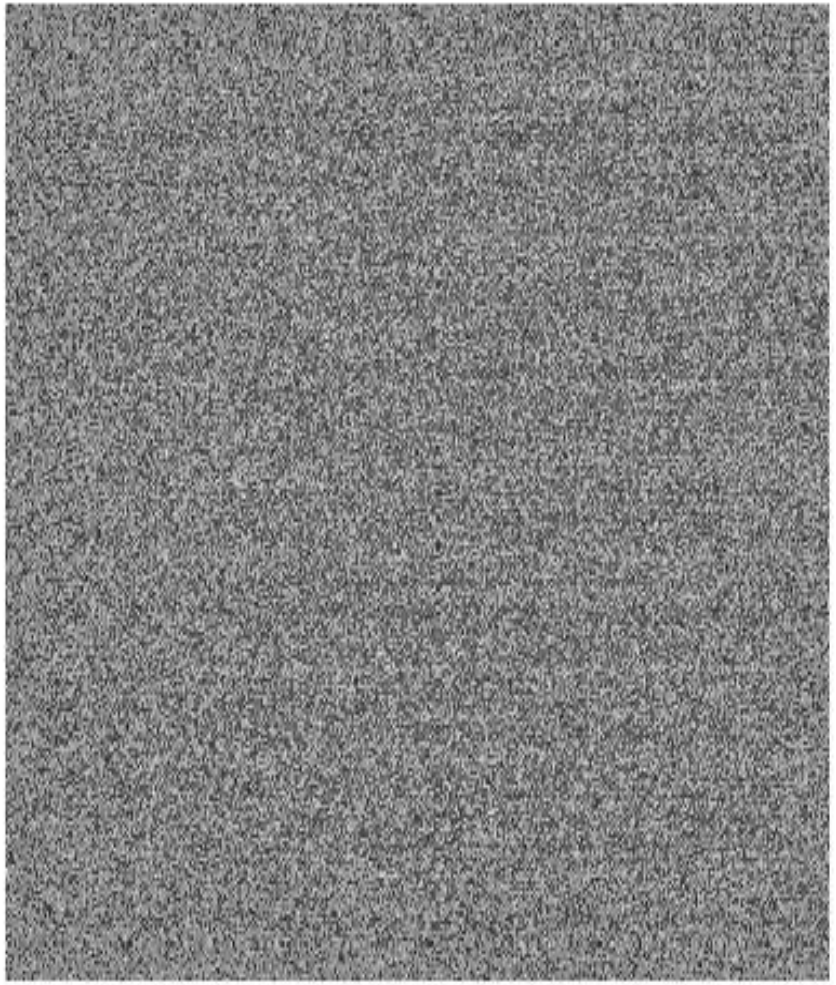
CMOS LUMINESCENCE



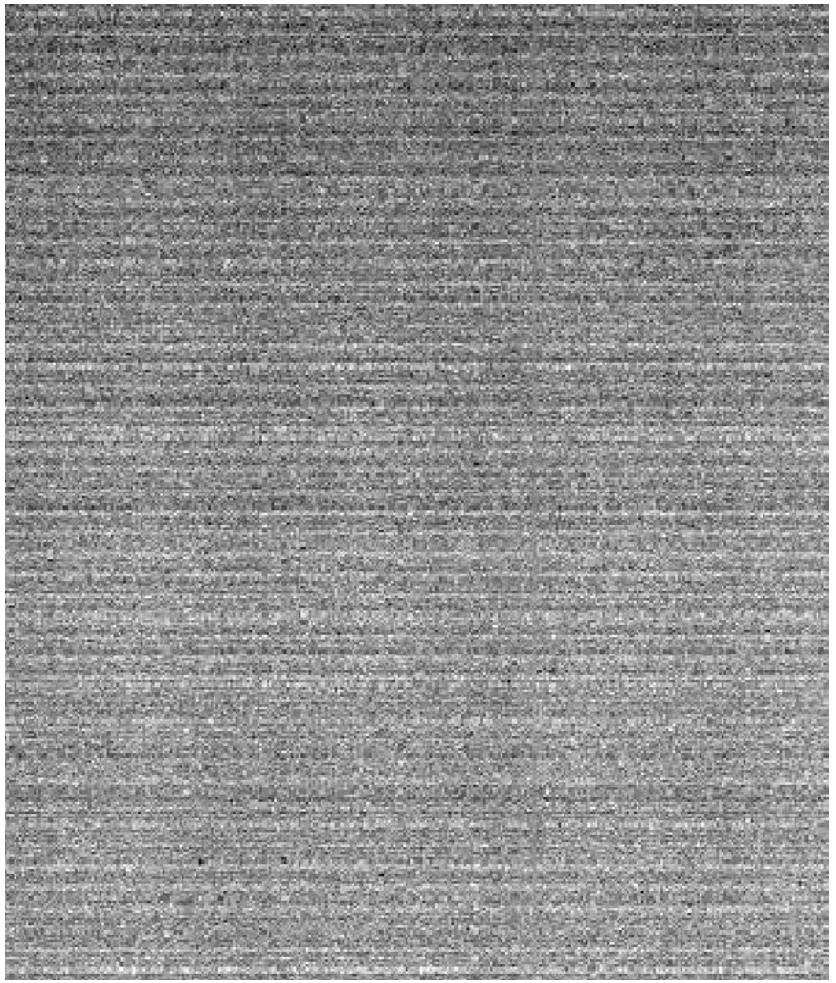
System Noise

SYSTEM NOISE

Low noise at low speed readout



2.5 Mpixels /sec



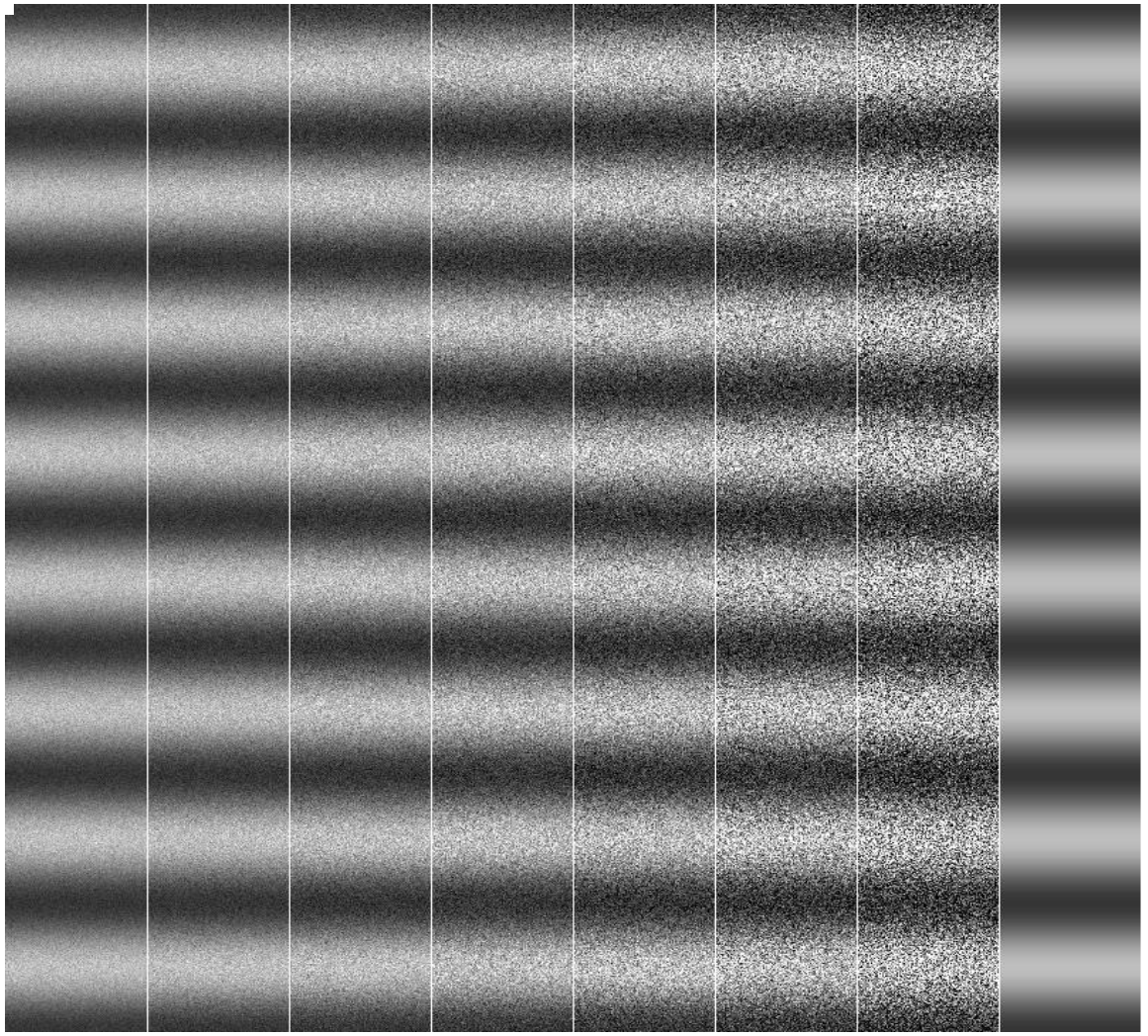
5.0 Mpixels /sec

Higher noise at high speed readout

Part 7
Performance Measurement

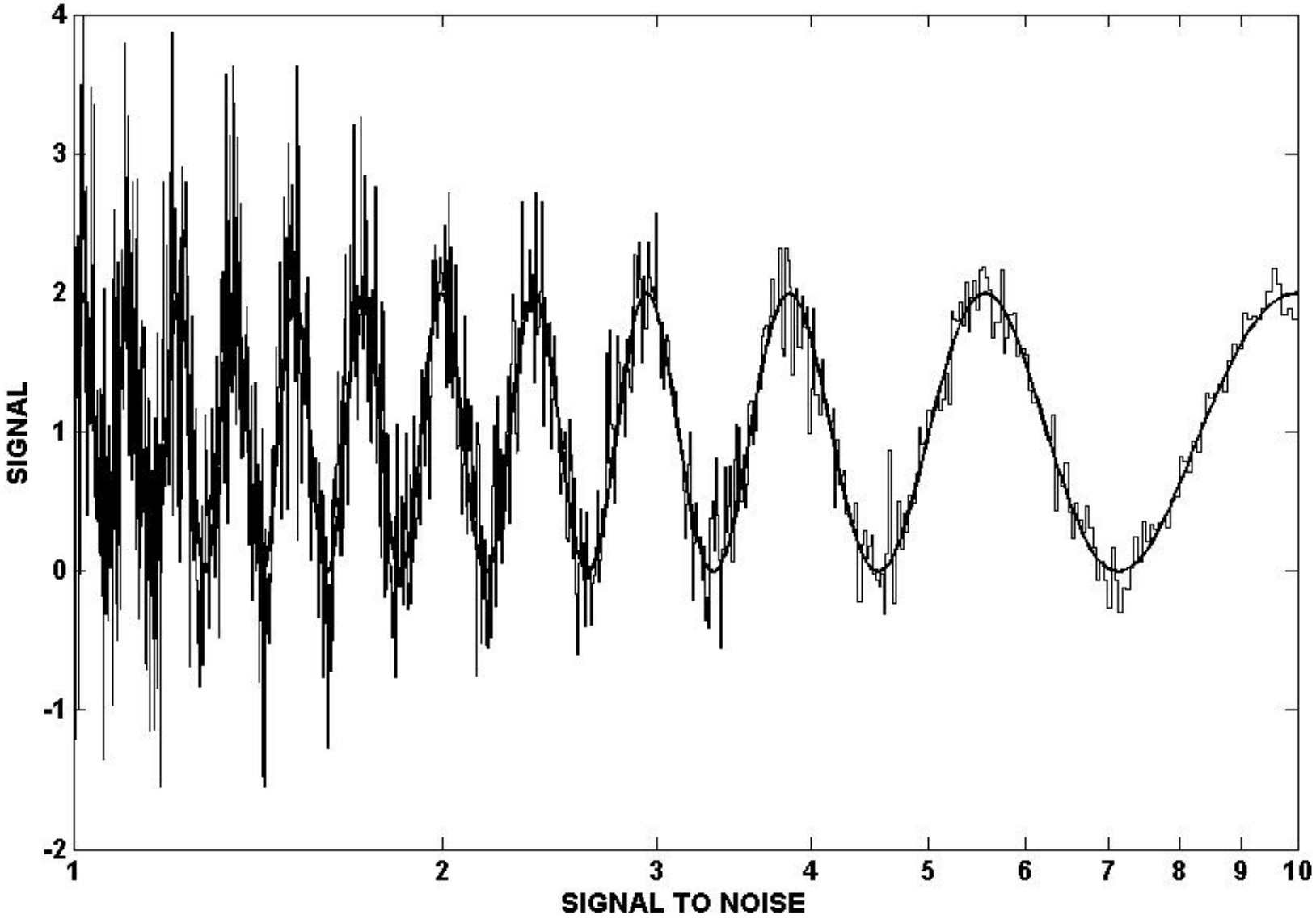
Signal to Noise Ratio (SNR)

SIGNAL-TO-NOISE



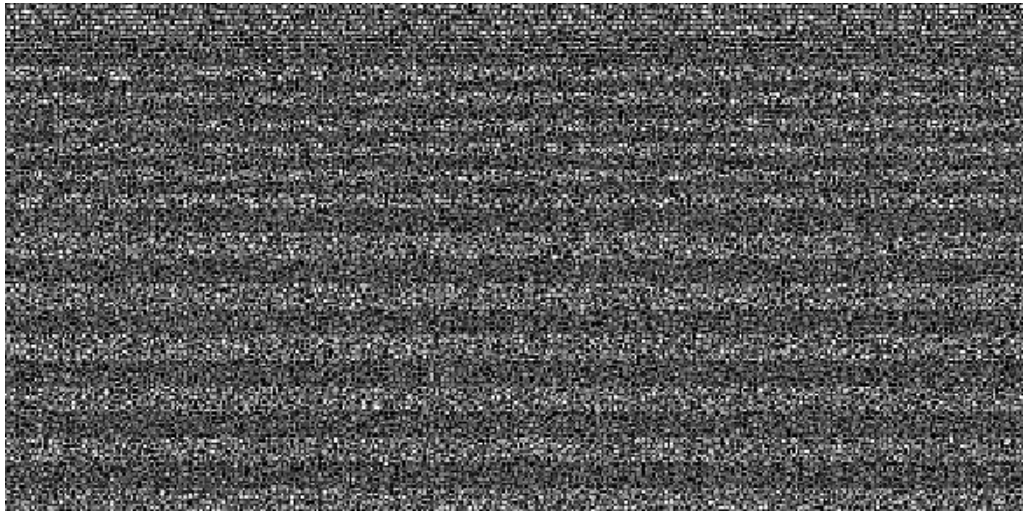
S/N =7.0 5.0 4.0 3.0 2.0 1.4 1.0 ∞

SIGNAL-TO-NOISE



1 e- IMAGERY

1 e- SIGNAL
1 e- SHOT NOISE
0 e- READ NOISE



1 e- SIGNAL
1 e- SHOT NOISE
1 e- READ NOISE

How do we measure performance?

- **Need objective method to assess sensor performance**
- **Quantify sensor performance using theory and graphical methods**
- **Plot noise versus signal for basic measurements**

FLAT FIELD S/N TRANSFER CURVES

- **PHOTON TRANSFER**

  NOISE VERSUS SIGNAL

- **LUX TRANSFER**

  S/N VERSUS ABSOLUTE LIGHT LEVEL

PHOTON TRANSFER NOISE REGIMES

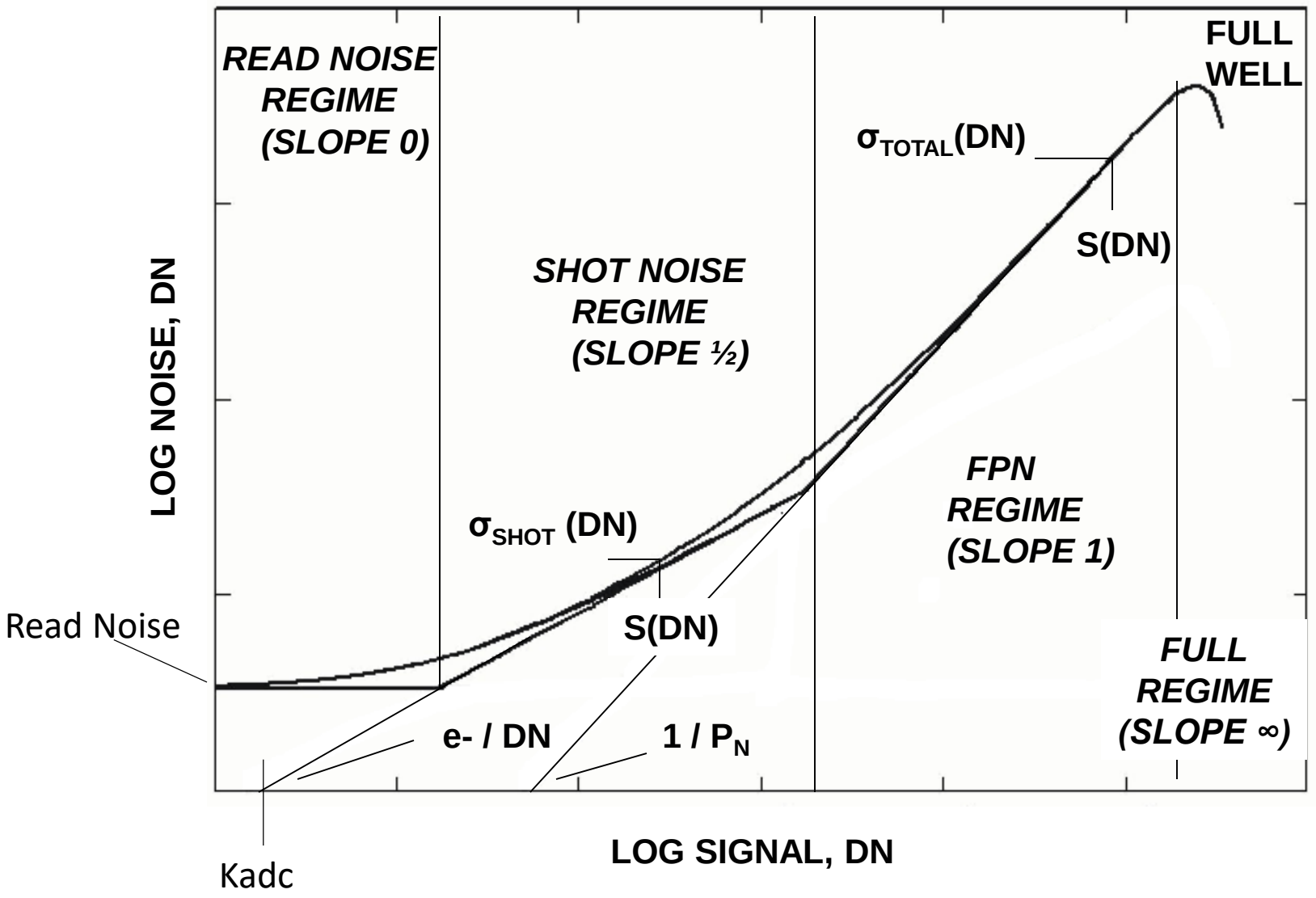
$$\text{Total Noise } (e^-) = (RN^2 + SN^2 + FPN^2)^{1/2}$$

RN = Read Noise (rms e^-)

SN = Shot Noise (rms e^-)
= (Signal (e^-))$^{1/2}$

FPN = Fixed Pattern Noise (rms e^-)
= P_N x Signal (e-)
P_N = Pixel Nonuniformity Factor

PHOTON TRANSFER CURVE (TOTAL NOISE)



SIGNAL-TO-NOISE REGIMES

READ NOISE REGIME

S/N= SIGNAL / READ NOISE

SHOT NOISE REGIME

S/N = SIGNAL / SHOT NOISE = SIGNAL / SIGNAL$^{1/2}$ = SIGNAL$^{1/2}$

FIXED PATTERN NOISE (FPN) REGIME

S/N = SIGNAL / FPN = 1 / P_N ⟵ CONSTANT !

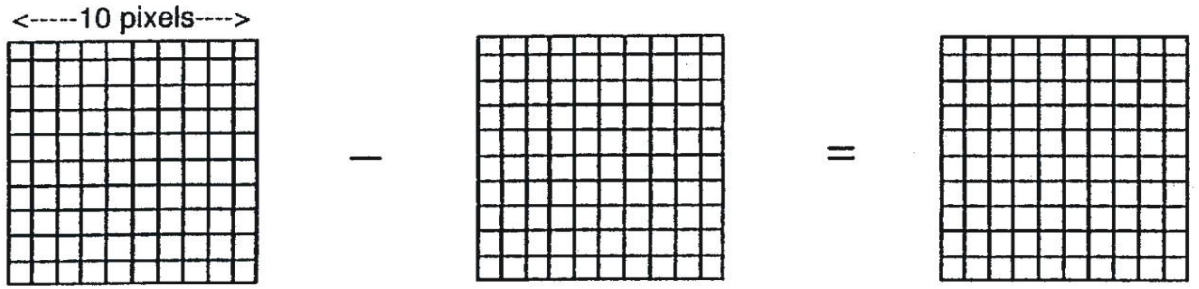
WHERE P_N = FPN / SIGNAL (SLOPE 1. . . APPROXIMATELY 1%)

FPN (e^-) = P_N x S(e^-)

ONSET OF FPN (e^-) = 1 / P_N^2

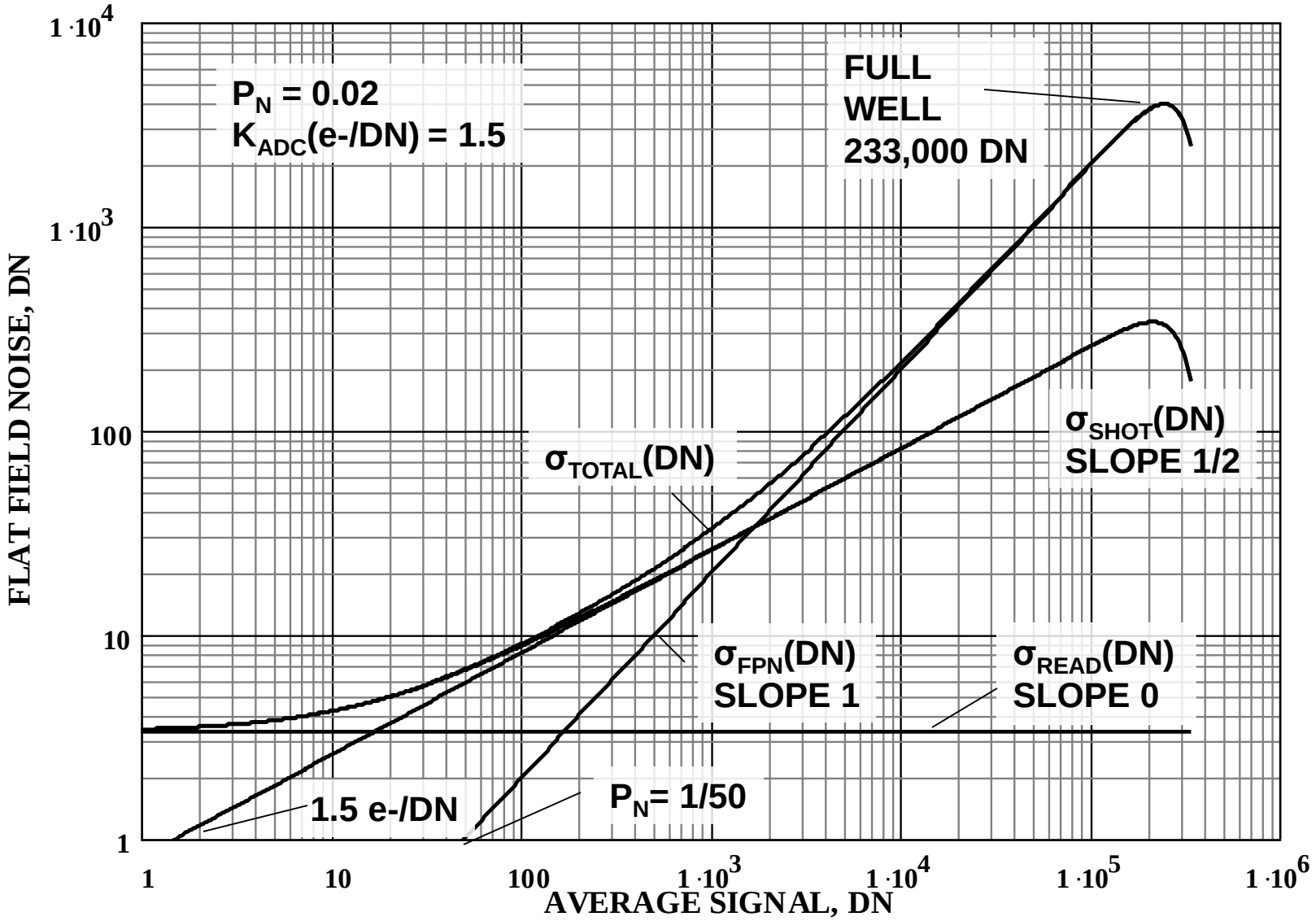
(APPROXIMATELY 10,000 e-)

PHOTON TRANSFER DATA COLLECTION
(FOR SHOT NOISE LIMITED RESPONSE)

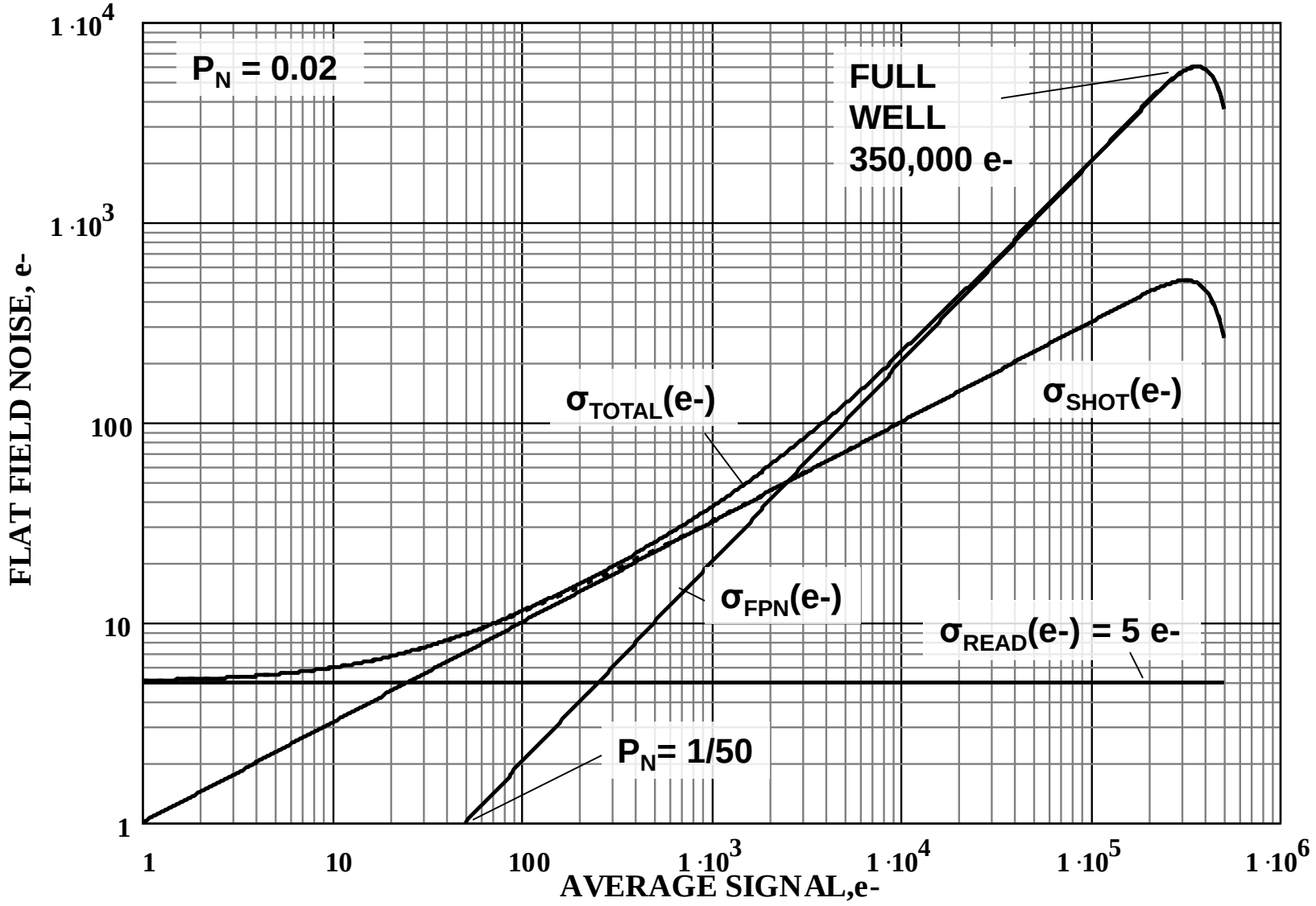


- **Signal(DN) = Average Signal Level of a Sub-array of Pixels**
- **Noise = Standard Deviation of Differenced Frames / $2^{1/2}$**

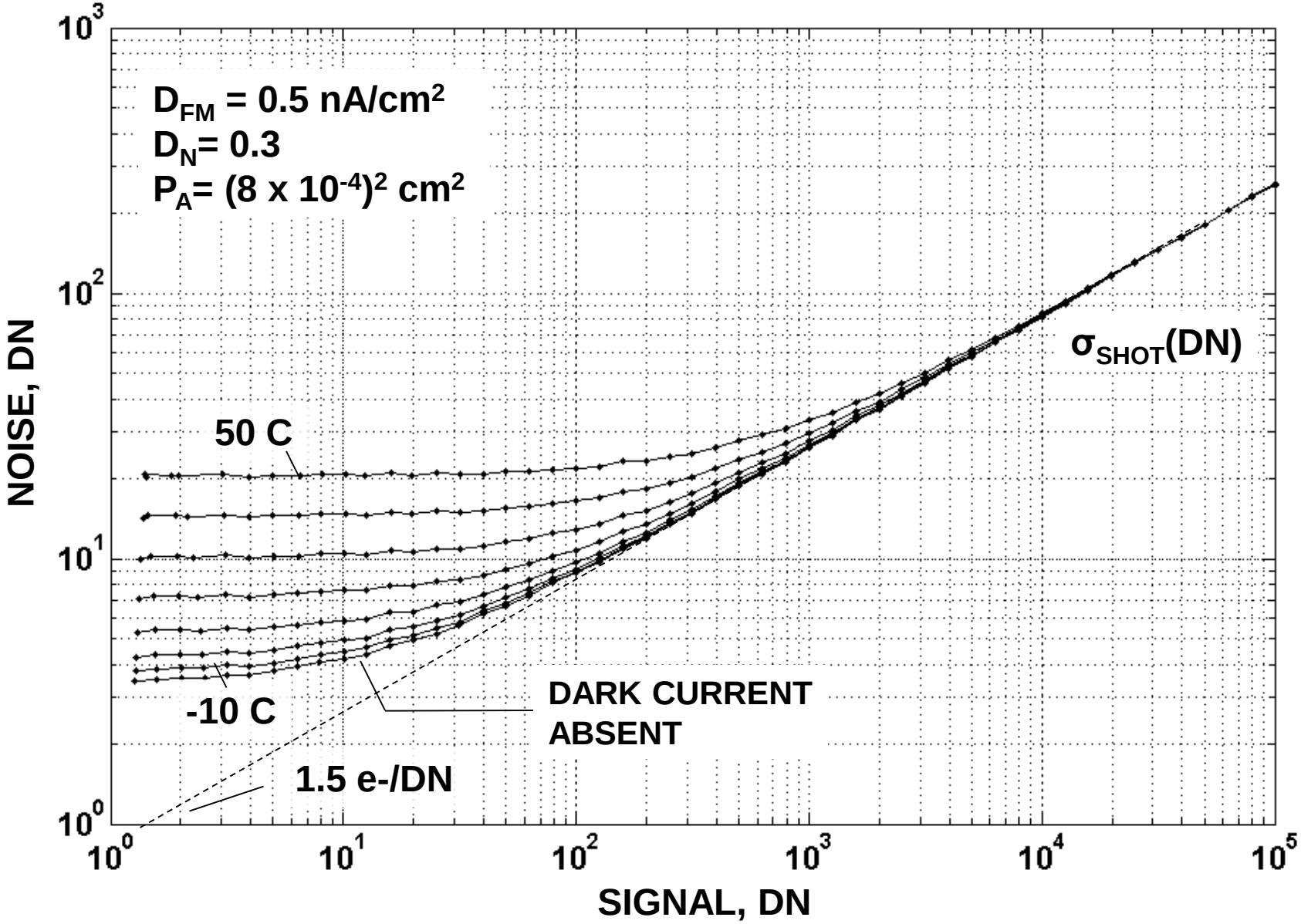
PHOTON TRANSFER CURVE
DN units



PHOTON TRANSFER CURVE
Electron units



PHOTON TRANSFER WITH DARK CURRENT SHOT NOISE



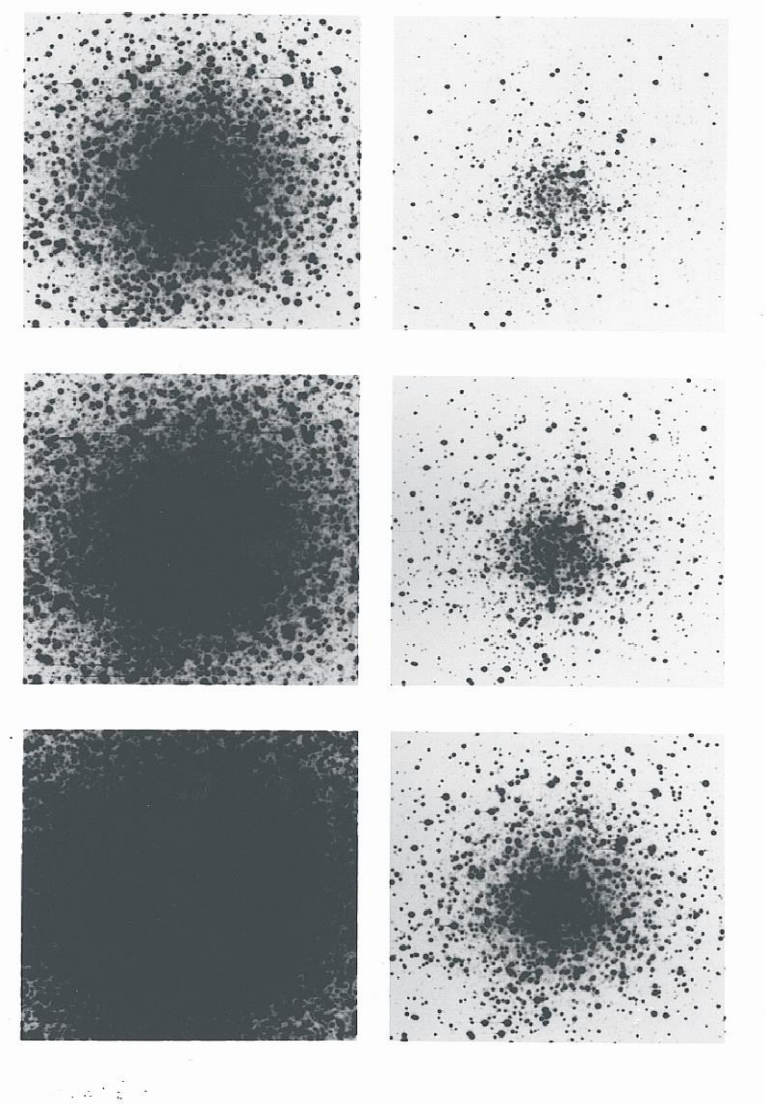
Normally you cool sensor or limit exposure to avoid any significant dark signal

DYNAMIC RANGE

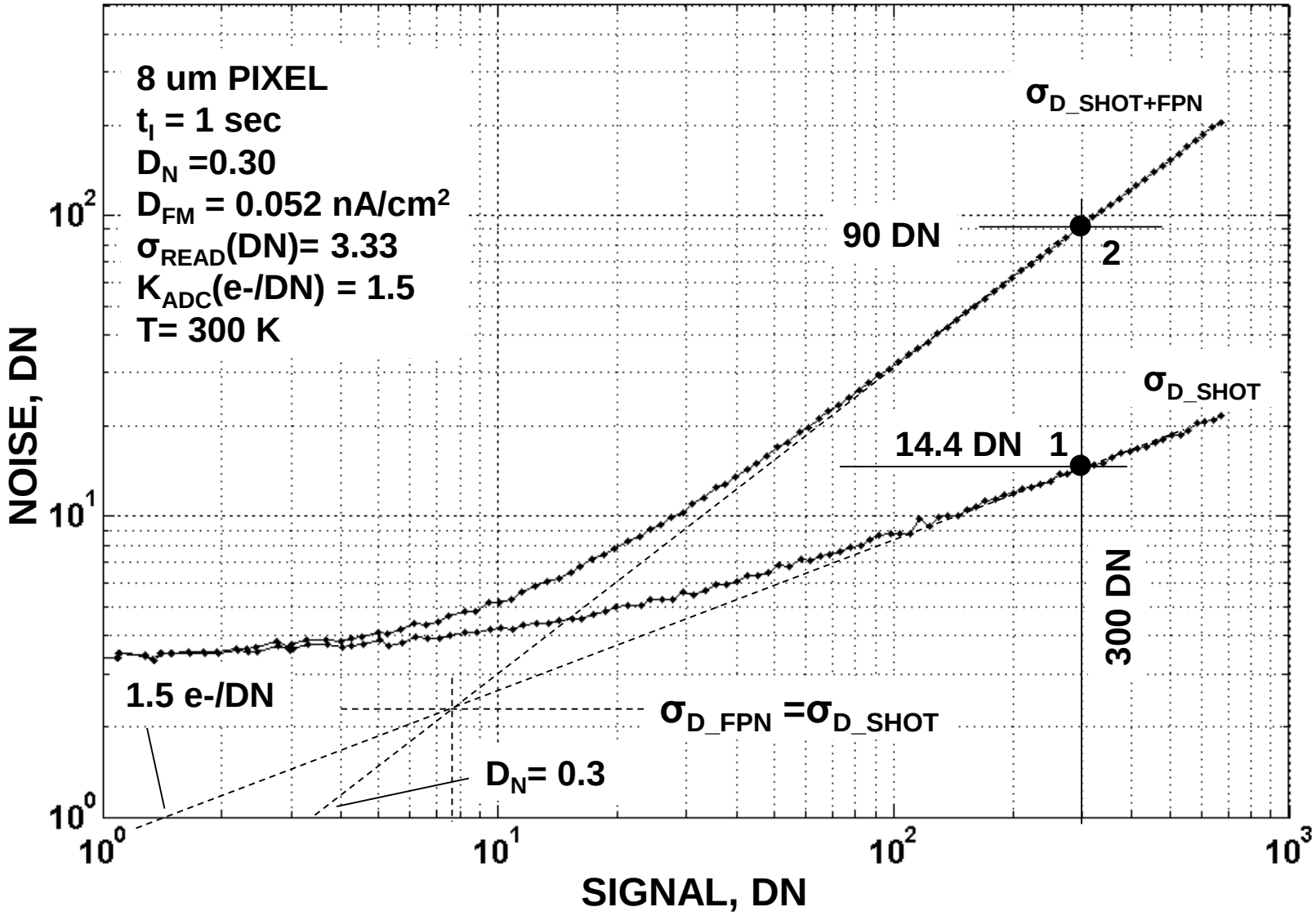
DYNAMIC RANGE:

FULL WELL / READ NOISE

Measured from PTC

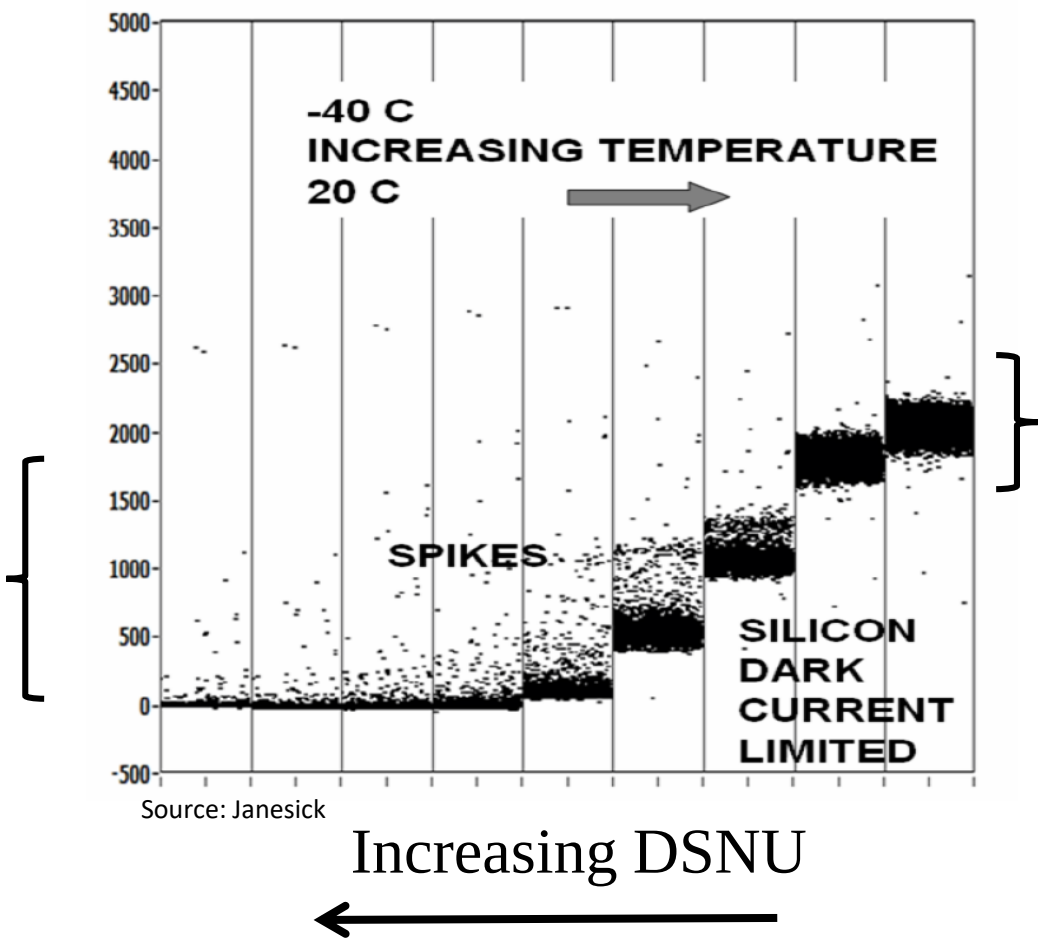


DARK PHOTON TRANSFER



Dark Spikes vs Temperature

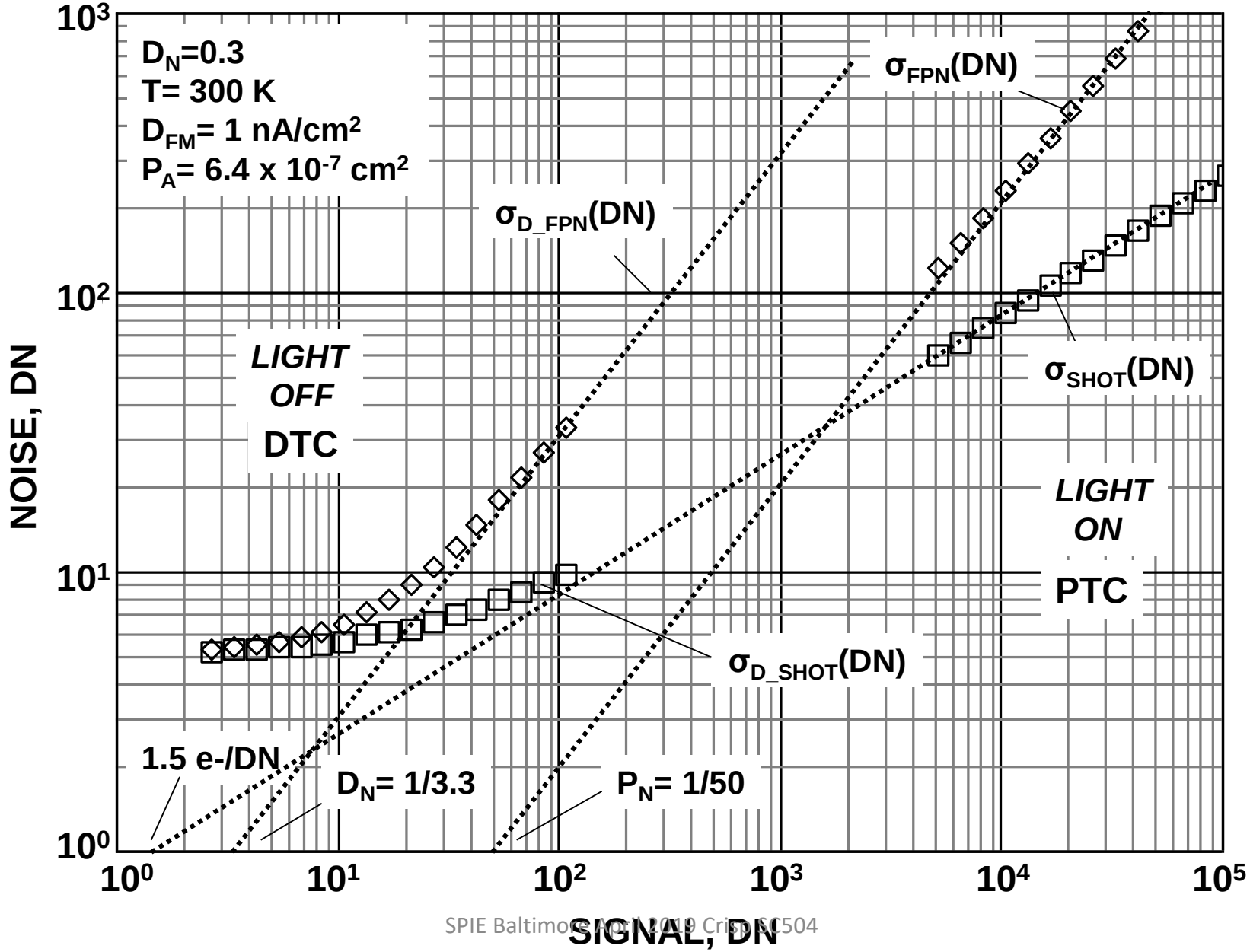
Reduced temperature: less thermal current, more variance of dark spikes: increases DSNU



Dark Current Limited: Reduces DSNU

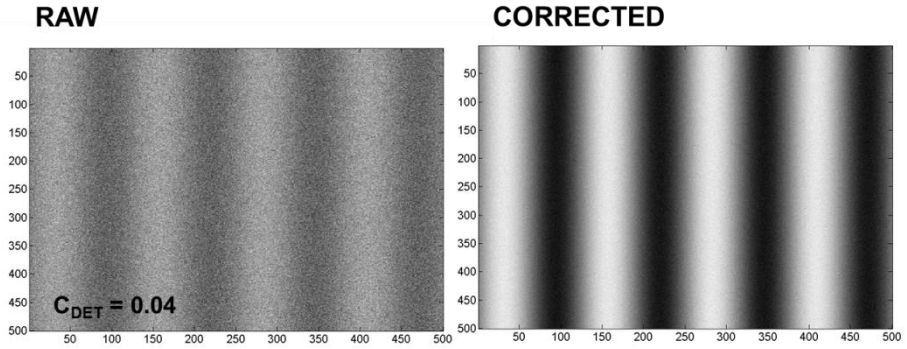
KAF series DSNU is specified at room temperature (25C)

DARK AND LIGHT PHOTON TRANSFER



Flat Fielding

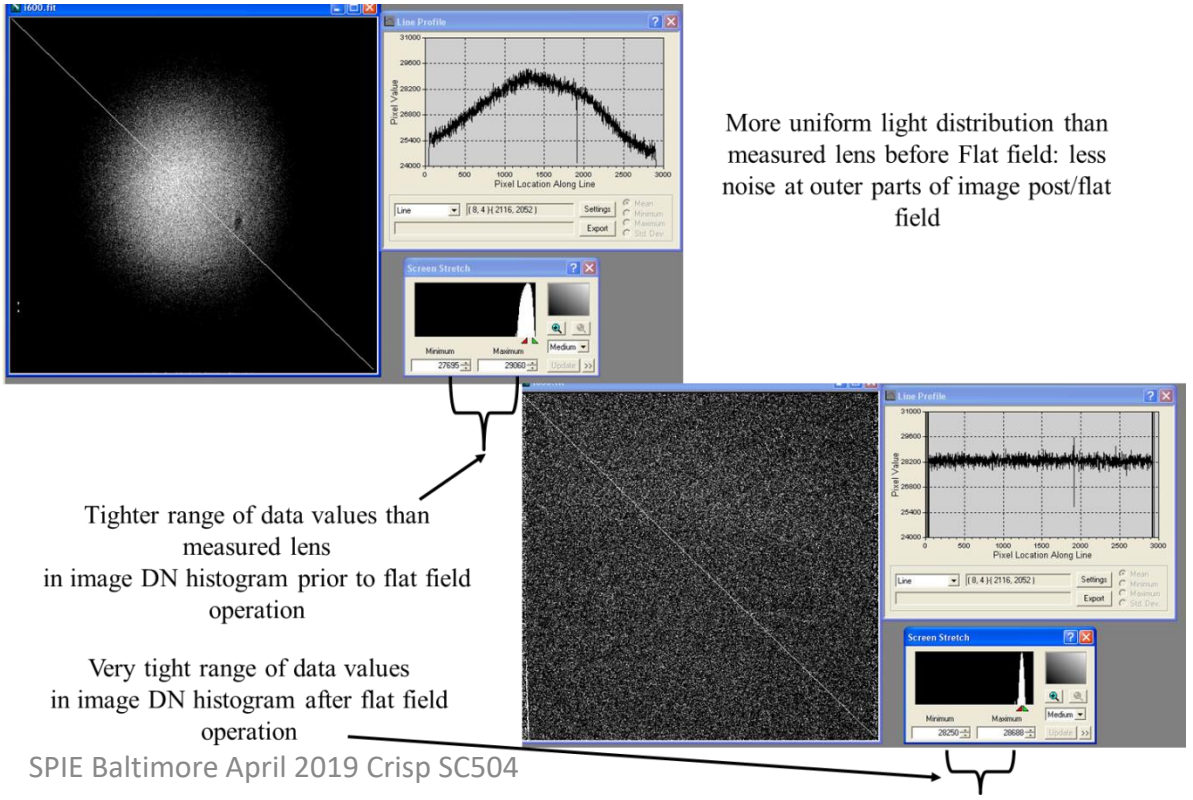
Flat Fielding for FPN Removal



Source: Janesick

Sensor FPN removal

Optical FPN removal



More uniform light distribution than measured lens before Flat field: less noise at outer parts of image post/flat field

Tighter range of data values than measured lens in image DN histogram prior to flat field operation

Very tight range of data values in image DN histogram after flat field operation

The flat fielding operation

The flat fielding operation consists of dividing, pixel by pixel, the raw image by a flat field image. The corrected ith pixel of an image that has been flat-fielded is expressed as:

$$S_{CORi} = \mu_{FF} \frac{S_{RAWi}}{S_{FFi}} \quad (1)$$

S_{COR_i} = corrected signal

S_{FF_i} = signal in flat field

S_{RAW_i} = signal in raw image

μ_{FF} = average signal level in flat field

Noise in a flat-fielded image

In order to test the efficacy of the flat-fielding operation, we need to know the noise of this corrected image. We now seek the equation for the noise of the corrected image in terms of the signal level in the flat field and the raw images.

Since the noise of the corrected image is simply the square root of the variance of the image we can calculate the variance.

The corrected image is a function of two variables, the raw signal and the flat field signal. To calculate the variance of a function of two variables where the variables are uncorrelated, we use the simplified propagation of errors formula:

$$\sigma_{\mathrm{Q}}^2 = \sigma_{\mathrm{x}}^2 \left(\frac{\partial \mathrm{Q}}{\partial \mathrm{x}} \right)^2 + \sigma_{\mathrm{y}}^2 \left(\frac{\partial \mathrm{Q}}{\partial \mathrm{y}} \right)^2 \qquad (2)$$

Noise in a flat-fielded image cont'd

Applying (2) to (1) and including a read noise term for a practical system we get

$$\sigma_{\mathrm{COR}}^2 = \sigma_{\mathrm{FF-shot}}^2 \left(\frac{\partial \mathrm{S}_{\mathrm{COR}}}{\partial \mathrm{S}_{\mathrm{FF}}} \right)^2 + \sigma_{\mathrm{RAW-shot}}^2 \left(\frac{\partial \mathrm{S}_{\mathrm{COR}}}{\partial \mathrm{S}_{\mathrm{RAW}}} \right)^2 + \sigma_{\mathrm{READ}}^2 \qquad (3)$$

Performing the differentiation and doing a lot of manipulation while substituting

$$\sigma^2{}_{\mathrm{FF\text{-}shot}} = \mathrm{S}_{\mathrm{FF}}$$

$$\sigma^2{}_{\mathrm{RAW\text{-}shot}} = \mathrm{S}_{\mathrm{RAW}}$$

equation (3) simplifies to

$$\sigma_{\mathrm{COR}}^2 = \mathrm{S}_{\mathrm{RAW}} \left(1 + \frac{\mathrm{S}_{\mathrm{RAW}}}{\mathrm{S}_{\mathrm{FF}}} \right) + \sigma_{\mathrm{READ}}^2 \qquad (4)$$

How it works

$$\sigma_{COR}^2 = S_{RAW}\left(1+\frac{S_{RAW}}{S_{FF}}\right)+\sigma_{READ}^2 \qquad (4)$$

so long as $S_{FF} >> S_{RAW}$ equation (4) reduces to

$$\sigma_{COR}^2 = S_{RAW}+\sigma_{READ}^2$$

which is shot noise limited when $S_{RAW} > \sigma_{READ}^2$

indicating the Fixed Pattern Noise is completely removed thereby meeting our goal

One remaining issue related to finite well depth

Unfortunately with a finite well depth the inequality $S_{FF} >> S_{RAW}$ cannot always be guaranteed when using a single flat field frame to calibrate a raw image containing a high signal level. A solution can be found by averaging N_{FF} frames of signal level S_{FF}

$$\sigma^2_{COR} = S_{RAW}\left(1+\frac{S_{RAW}}{N_{FF}S_{FF}}\right)+\sigma^2_{READ} \qquad (5)$$

Solving the finite well depth issue

Since any arbitrary number of flat field images can be combined together, it is a simple matter to guarantee $N_{FF}S_{FF} >> S_{RAW}$ by selecting an appropriate value of N_{FF} and S_{FF} such that (5) simplifies to

$$\sigma_{COR}^2 = S_{RAW} + \sigma_{READ}^2 \qquad (6)$$

Taking the square root of each side and substituting descriptive names for the variables (6) transforms into our desired noise equation, which is free of the SNR-limiting FPN term

$$\text{Noise}_{IMAGE} = \sqrt{\text{Signal} + \text{Read\_noise}^2}$$

Total Signal Level for “breakeven”

- When a flat is used to flat-field another flat of equal signal level, the shot noise in the resulting image is increased by SQRT(2)

- If the noise (electron units) of the flat-fielded image is set to be equal to the noise of the non-flat-fielded image the “breakeven” level of signal (electrons) in the flat field dataset is determined in terms of PRNU (see next page):
  - For the dataset used for the master flat, we can determine the minimum amount of signal needed to prevent increasing the noise after flat-fielding
  - If the signal is less than this minimum, flat-fielding will increase the noise in the image: this is counter to the purpose of flat-fielding

Breakeven signal level

$$\text{Noise}_{\text{IMAGE}} = \sqrt{\text{Signal} + (\text{Signal} * \text{PRNU})^2 + \text{Read\_Noise}^2} = \sqrt{\text{Signal}\left(1 + \frac{\text{Signal}}{Q_{FF}}\right) + \text{Read\_Noise}^2}$$

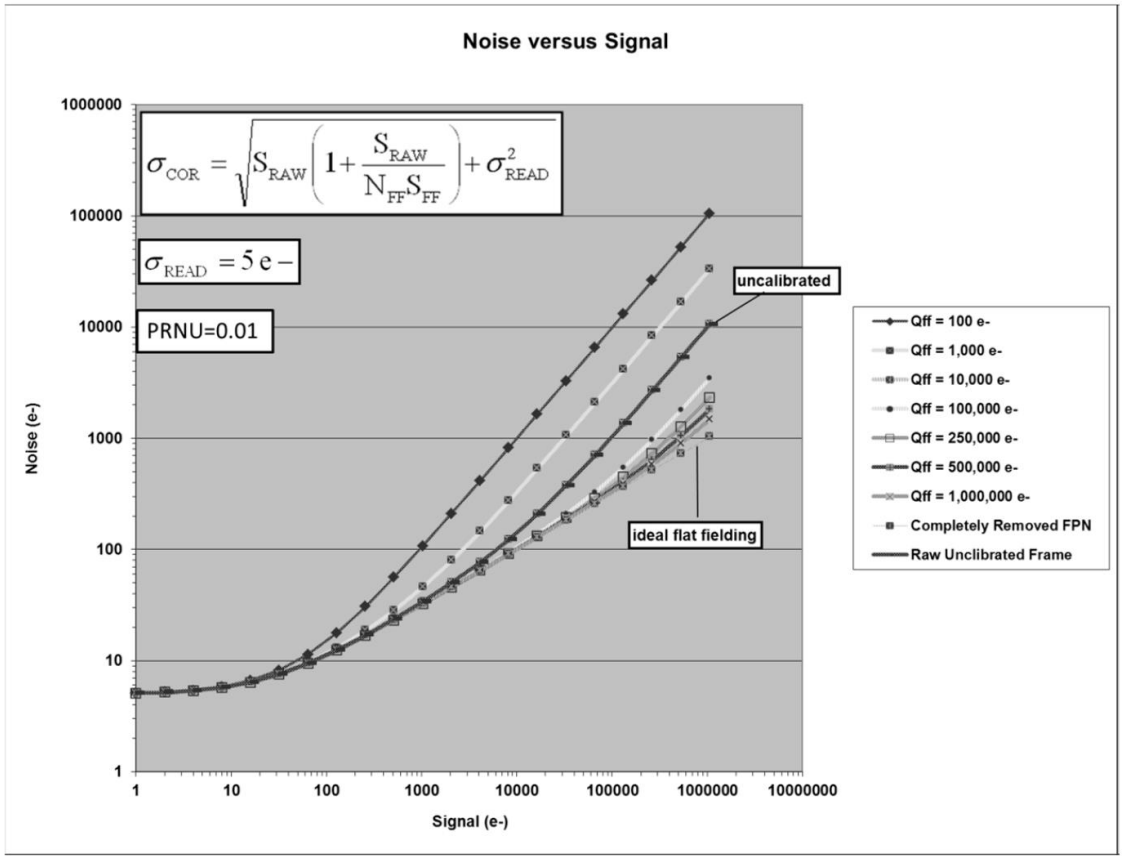
Solving for Q_{FF}

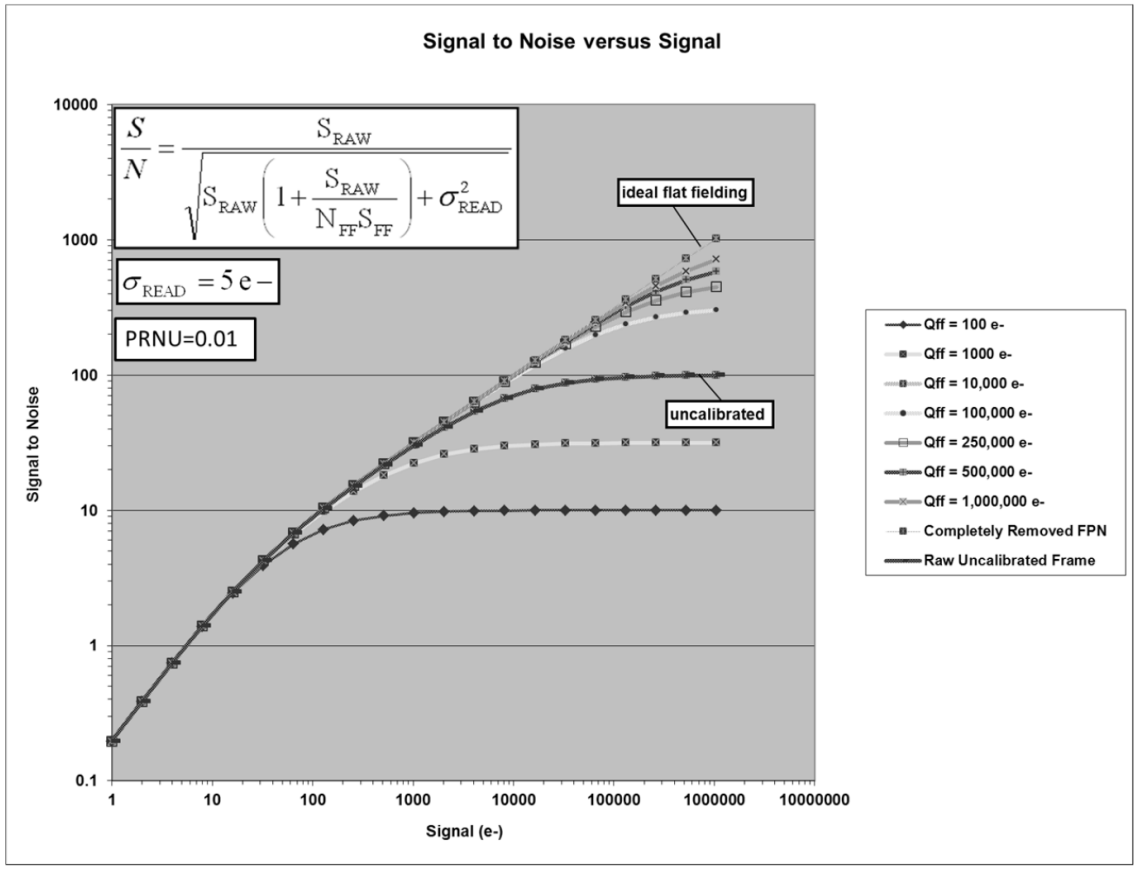
$$Q_{FF_{\text{Breakeven}}} = \frac{1}{\text{PRNU}^2}$$

This says that as PRNU increases, the minimum number of electrons needed in the flat field set to avoid increasing noise, drops.

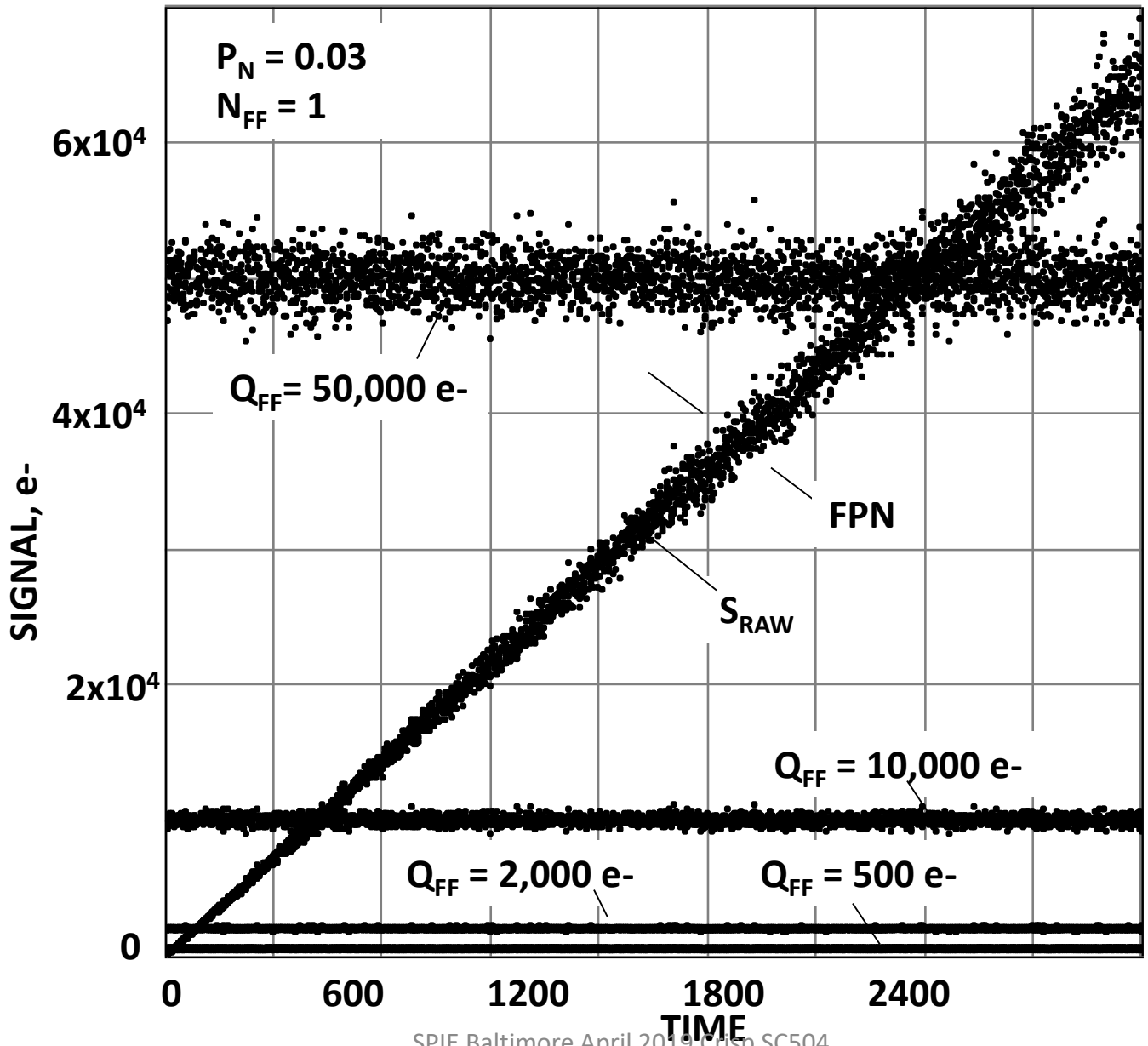
Ie: the noisier is the raw image, so the noisier can be the flat without increasing the noise in the calibrated image

Flat Field PTC, PRNU = 1%

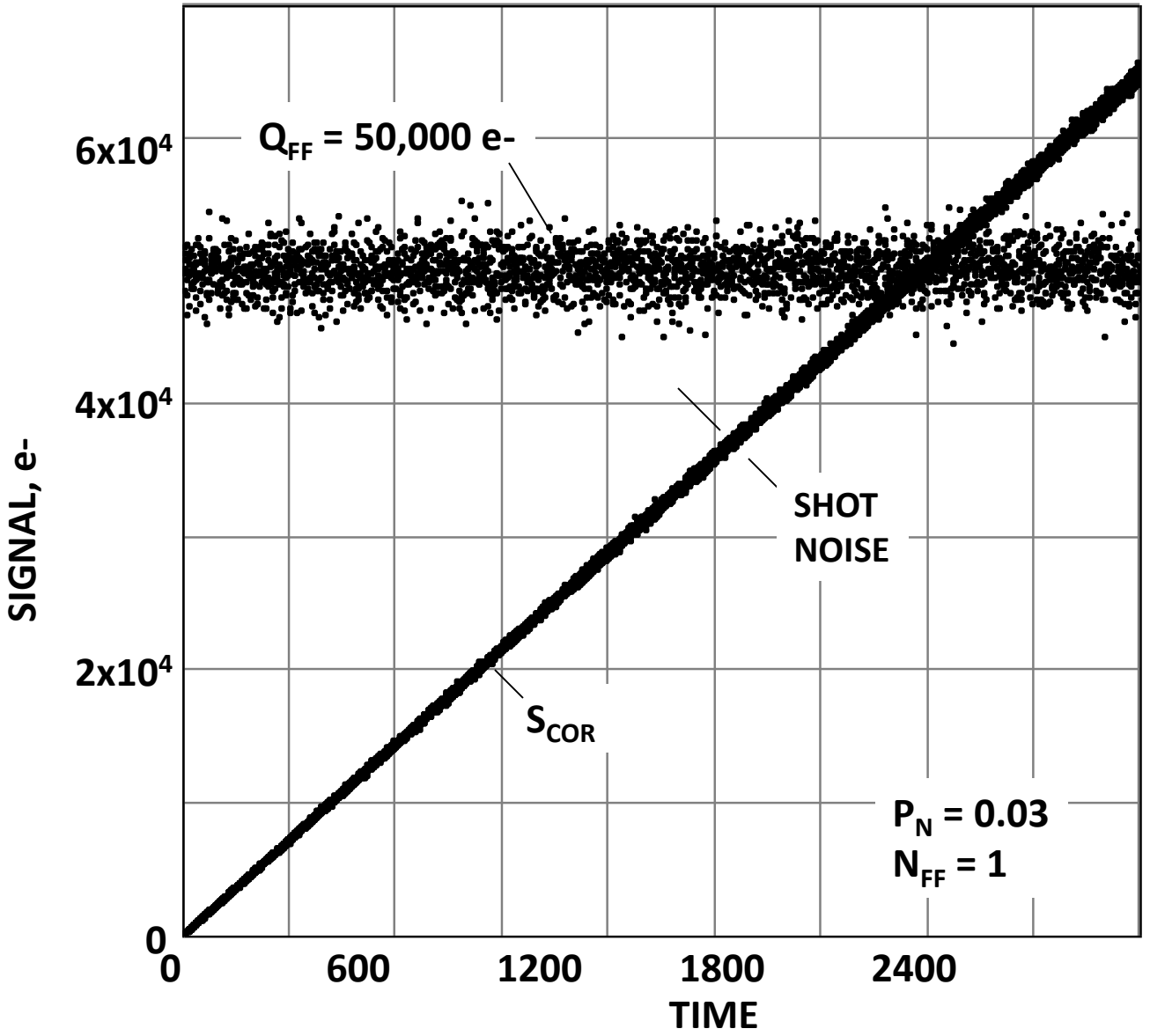




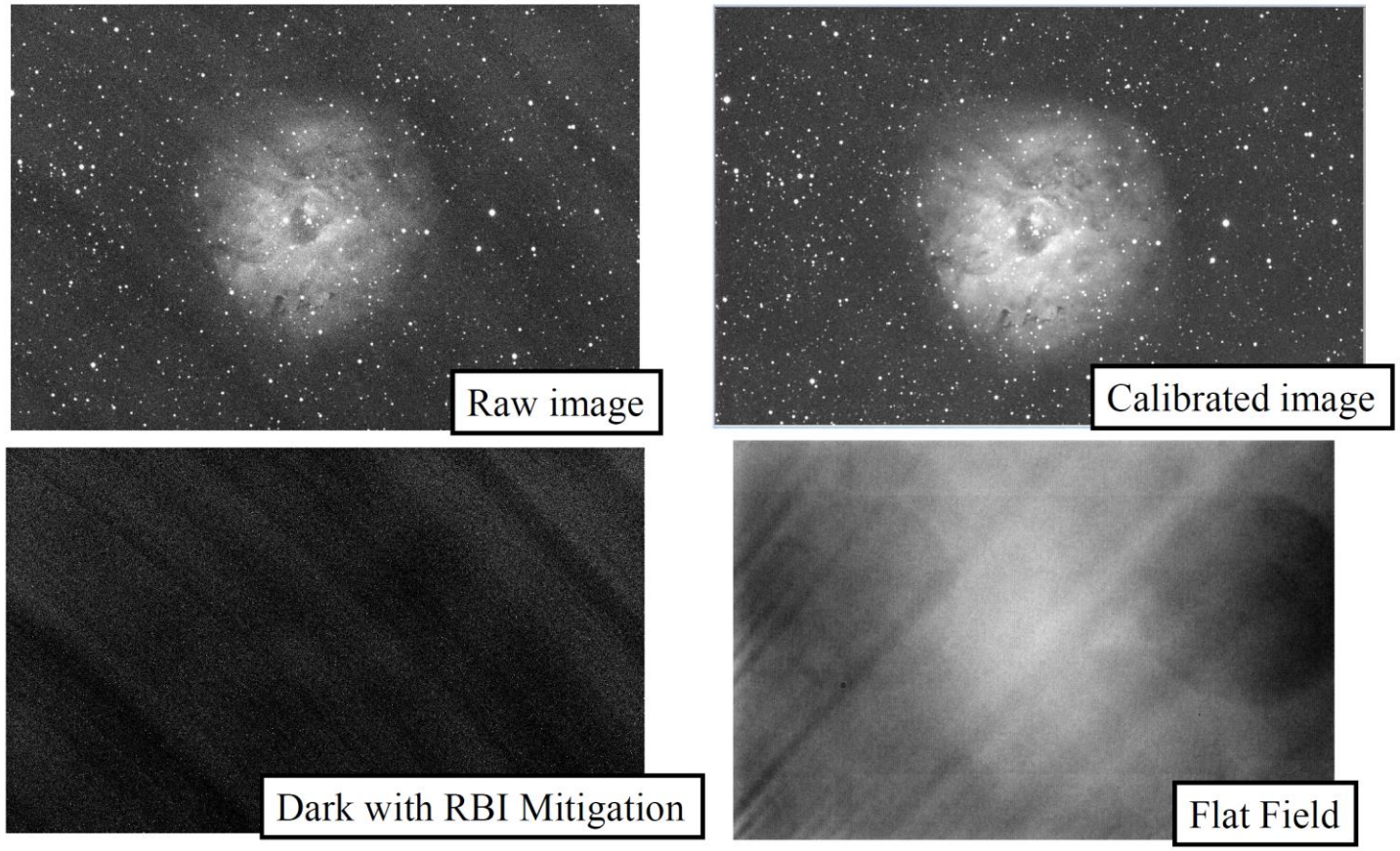
FLAT FIELDING



FLAT FIELDING

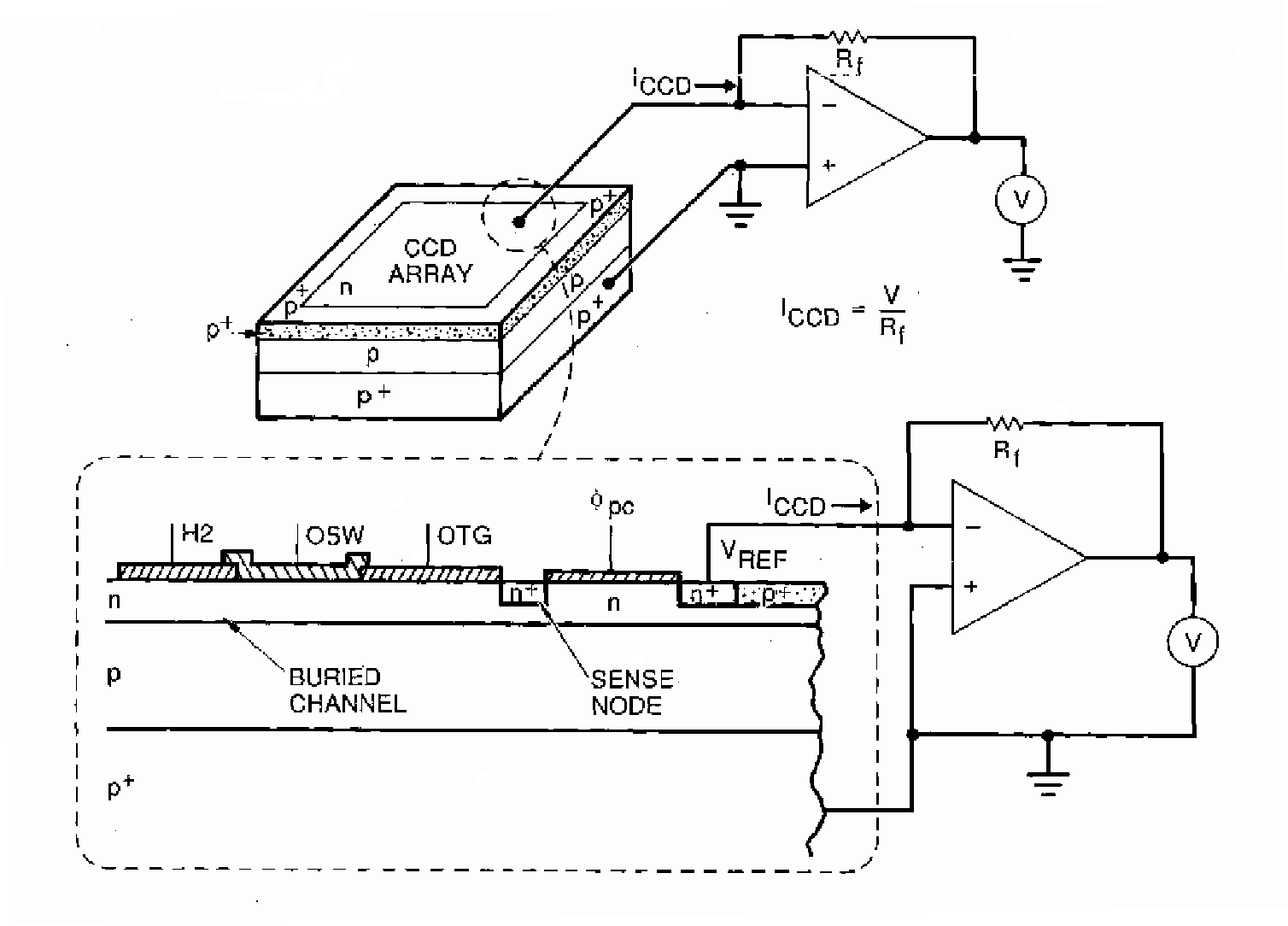


Before/after Despiking & Flat-fielding

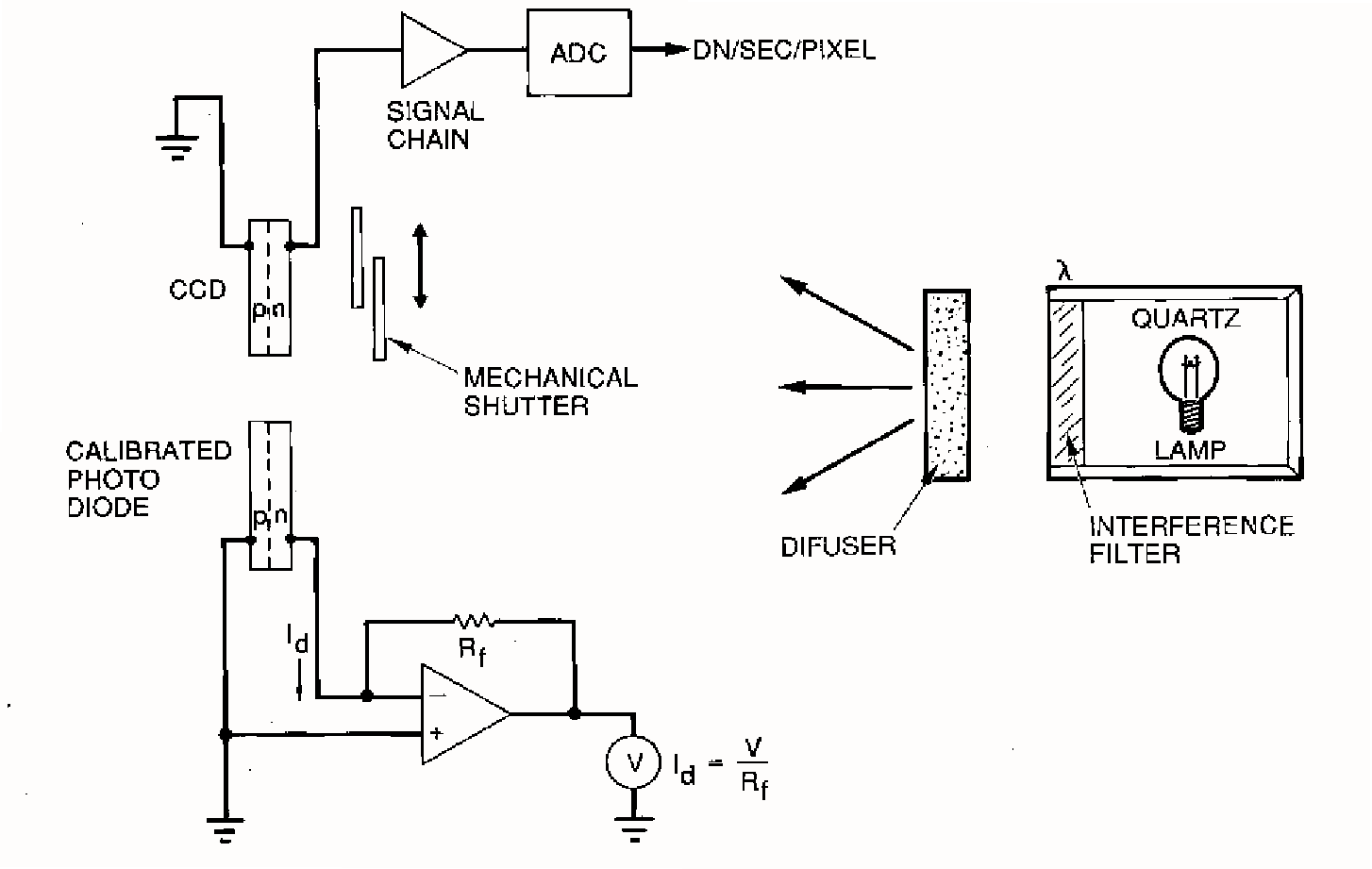


QE Transfer

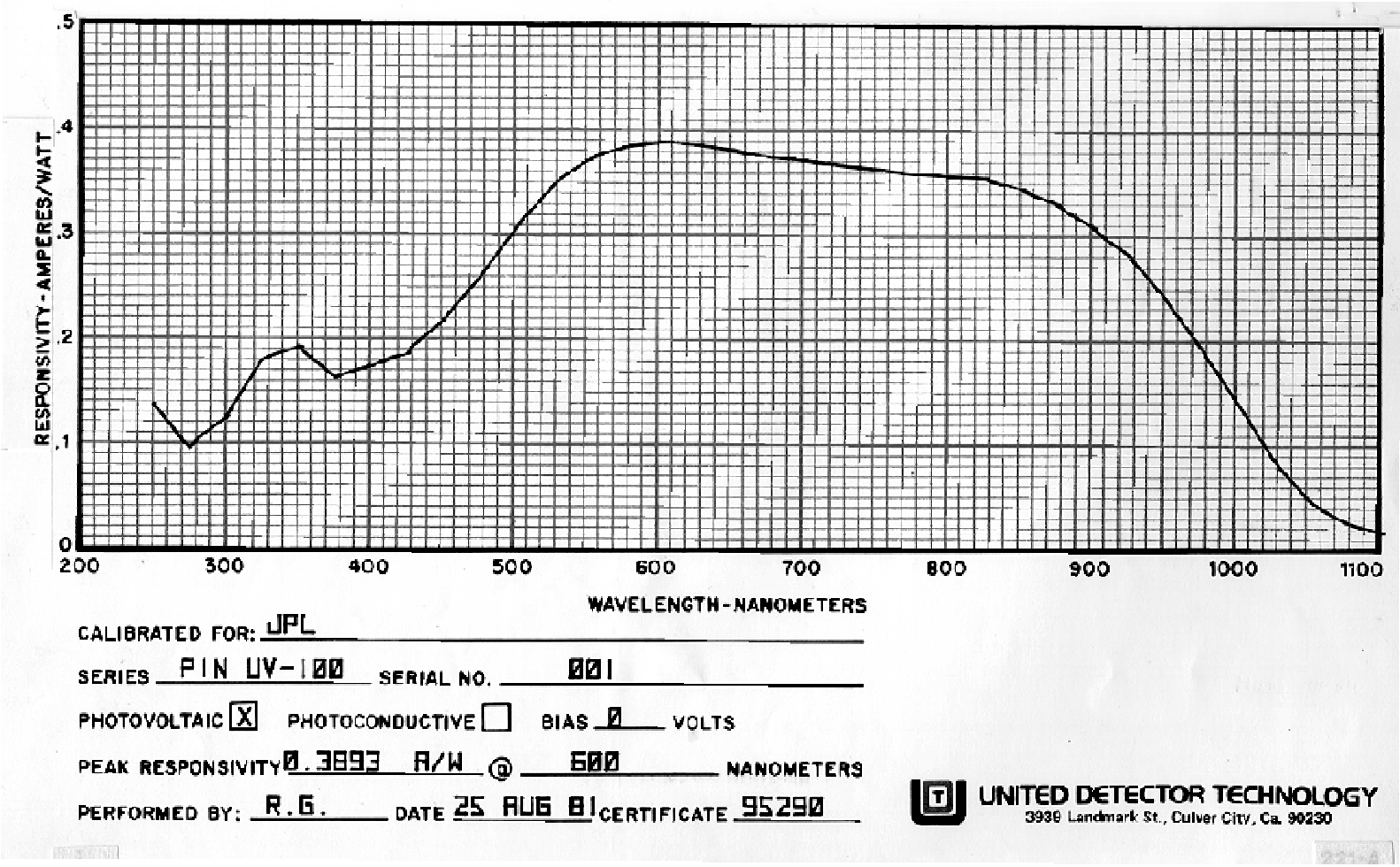
CCD AS PHOTO DIODE



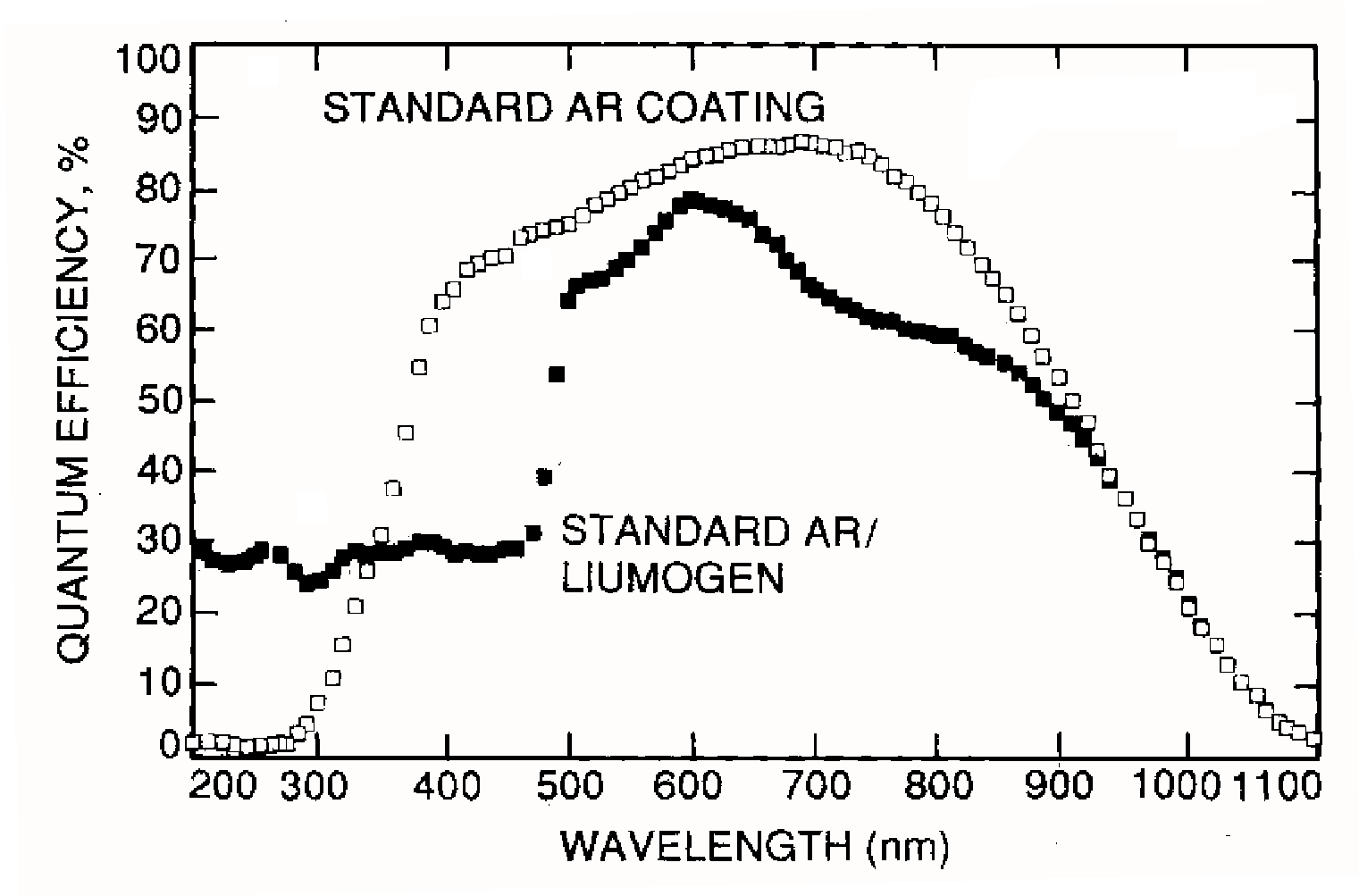
QUANTUM EFFICIENCY (QE) TRANSFER



PHOTON STANDARD (calibrated photodiode)

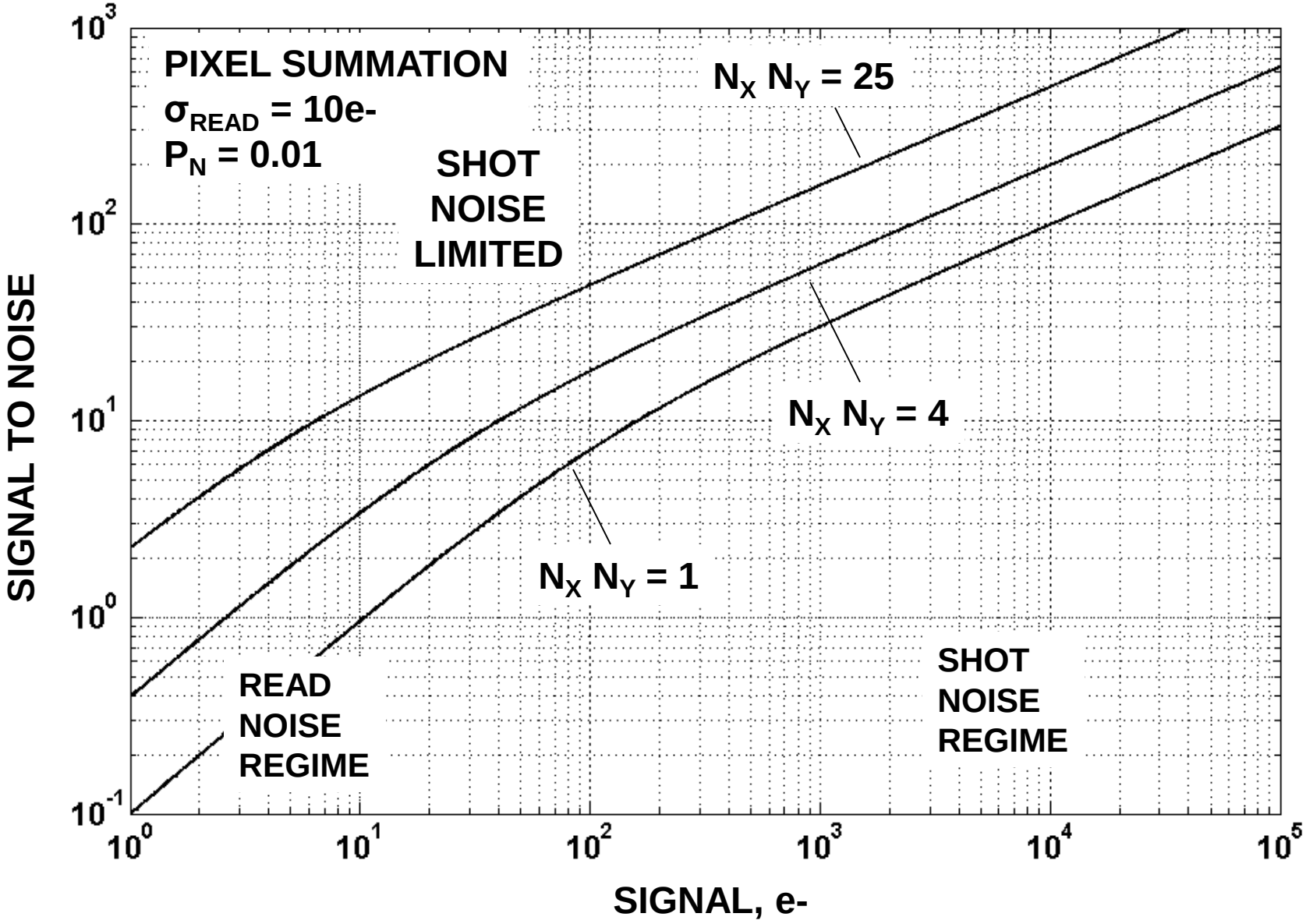


QE Curve


STANDARD AR COATING
STANDARD AR/
LIUMOGEN
QUANTUM EFFICIENCY, %
WAVELENGTH (nm)
100
90
80
70
60
50
40
30
20
10
0
200
300
400
500
600
700
800
900
1000
1100

Binning / on-chip summation

ON CHIP PIXEL SUMMATION



Analyzing / Optimizing Images with Modulation

Analysis of Images with Modulation

An image with modulation can be analyzed using the noise equation, by treating the RMS modulation as another noise term:

$$\delta_{total} = \mathrm{SQRT}(\delta_{modulation}{}^2 + Read\_noise^2 + Shot\_noise^2 + fixed\_pattern\_noise^2 + Dark\_fixed\_pattern\_noise^2 + Dark\_shot\_noise^2)$$

If the image to be analyzed has been flat-fielded and the operating temperature is low enough, then the dark and fixed pattern noise terms can be ignored simplifying the equation to:

$$\delta_{total} = \mathrm{SQRT}(\delta_{modulation}{}^2 + Read\_noise^2 + Shot\_noise^2)$$

Images with Modulation

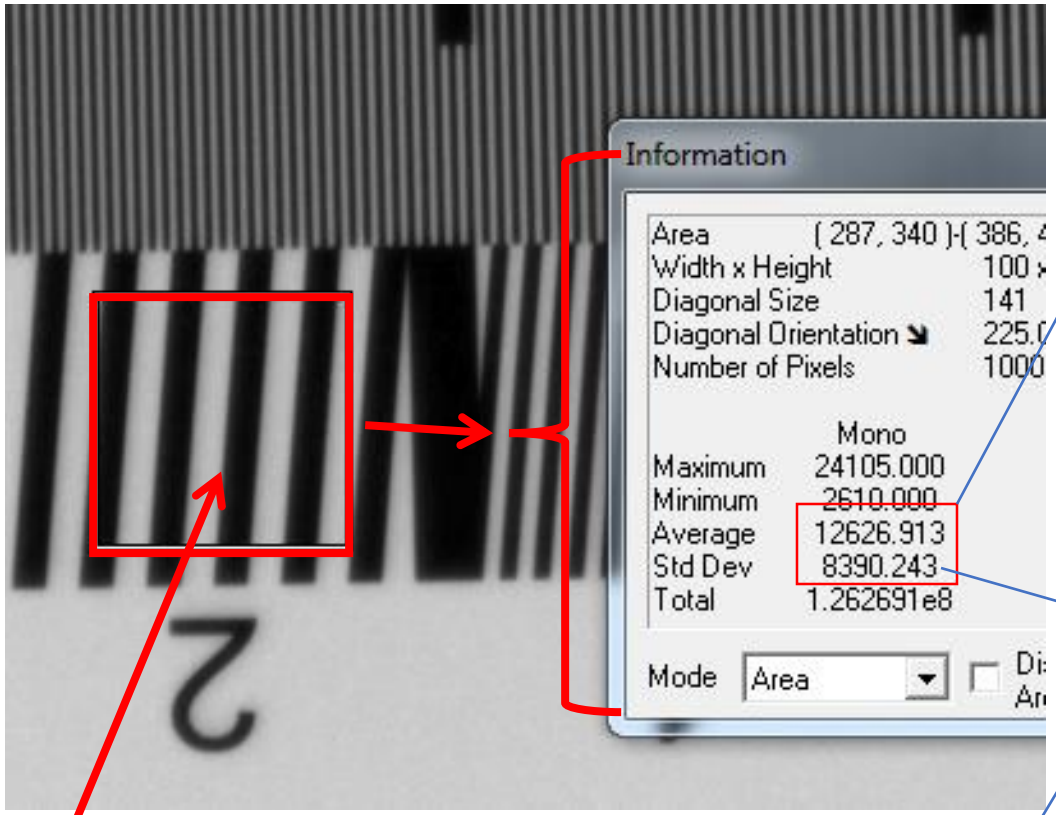
Mathematically the modulation, $\delta_{modulation}$, is modeled the same as fixed pattern noise, hence the value of the modulation is proportional to the average signal level. In this case instead of PRNU for FPN analysis a different constant, M_I is used.

For the analysis, the Modulation, $\delta_{modulation}$, is decomposed into a modulation constant, M_I, and an equivalent flat-field image with a signal level equal to the average value of the modulated image. The modulation constant, M_I , can be thought of like PRNU: the resulting modulation is proportional to signal level and this constant

$$\delta_{modulation} = M_I * \text{Equivalent\_flatfield\_average\_signal}$$

In general each feature in the image will have a different M_I and it is the variation of the M_I across the image that gives the image its appearance.

Making a Modulation PTC: Data Collection / Reduction



Equivalent Flat Field Signal Level

Offset from PTC

SNR of Flat= 103.32
SQRT(Avg-offset)
(assumed shot limited)

δ_{total}

Read_noise from PTC

Noise Equation

M_I

78.5%

SNR= 81.19

Calculating the SNR

The SNR of a modulated image is calculated by using the M_I factor multiplied by the SNR of a flat field image of the same average signal level:

$$SNR_{modulated\ image} = M_I * SNR_{Equivalent\ FF}$$

The total noise of the equivalent flat-field is equal to the shot noise of the flat field of that signal level: Noise = SQRT(Flat-Field Signal level)
SNR = (Flat-Field Signal level)/SQRT(Flat-Field Signal level)

SNR = SQRT(Flat-Field Signal level)

So in our example, the Signal Level for the Equivalent Flat-Field was 12,626.913DN – 1950DN of offset, making the SNR of the equivalent flat-field:

SQRT(12,626.913-1950) = 103.32

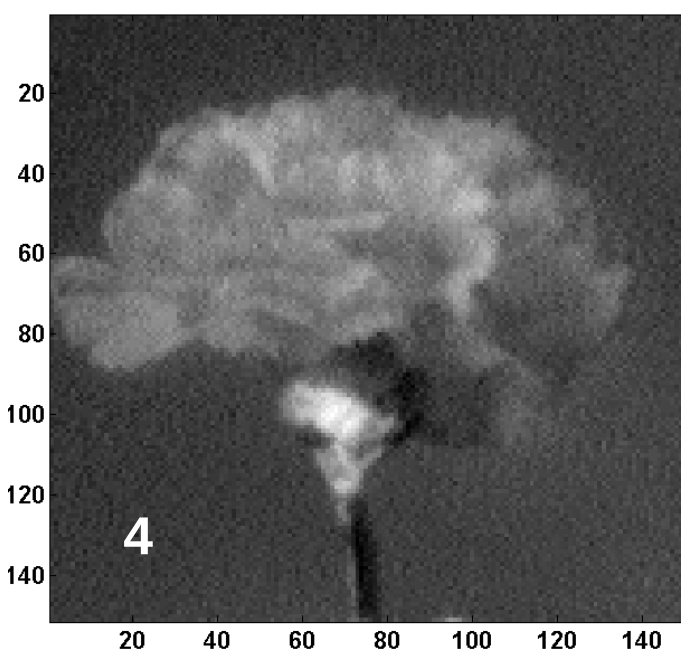
So with an M_I = 78.5% we get a final SNR for the modulated image region of:

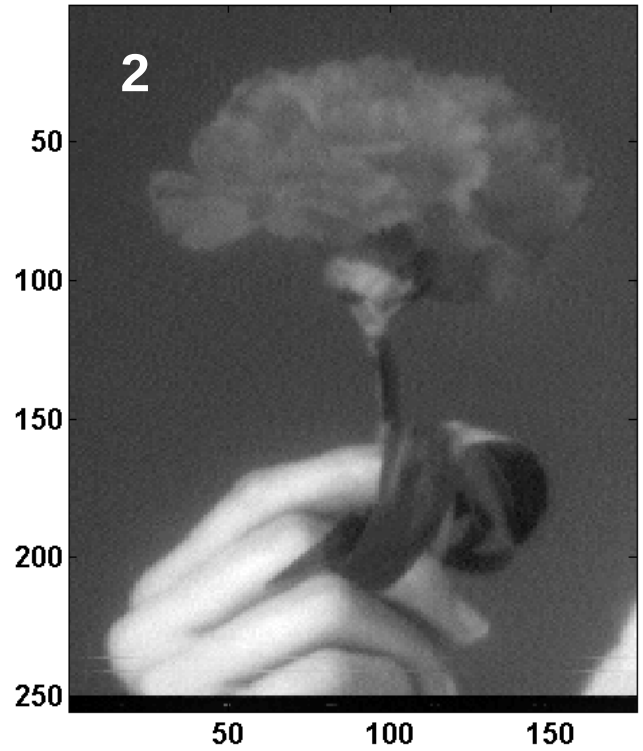
$SNR_{image-region} = 0.785 * 103.32 = 81.19$

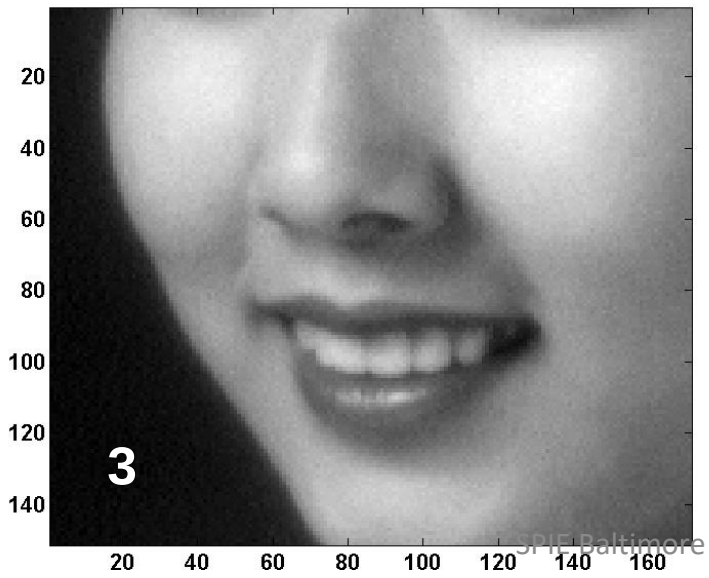
This is the calculation method that will be used for creating the curves that follow

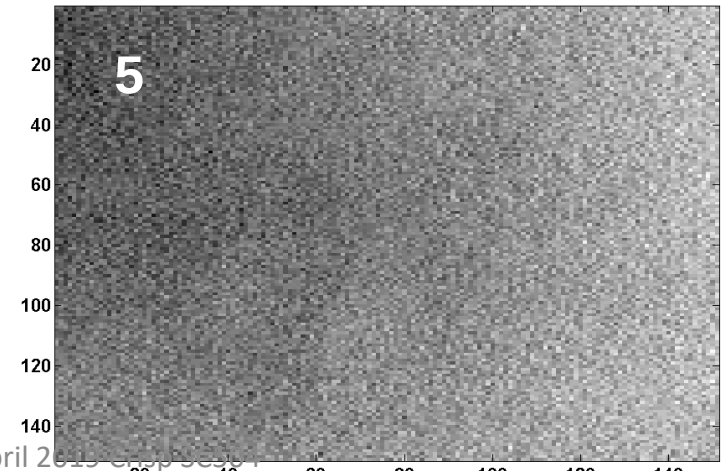
IMAGE SIGNAL TO NOISE

IMAGE SIGNAL TO NOISE

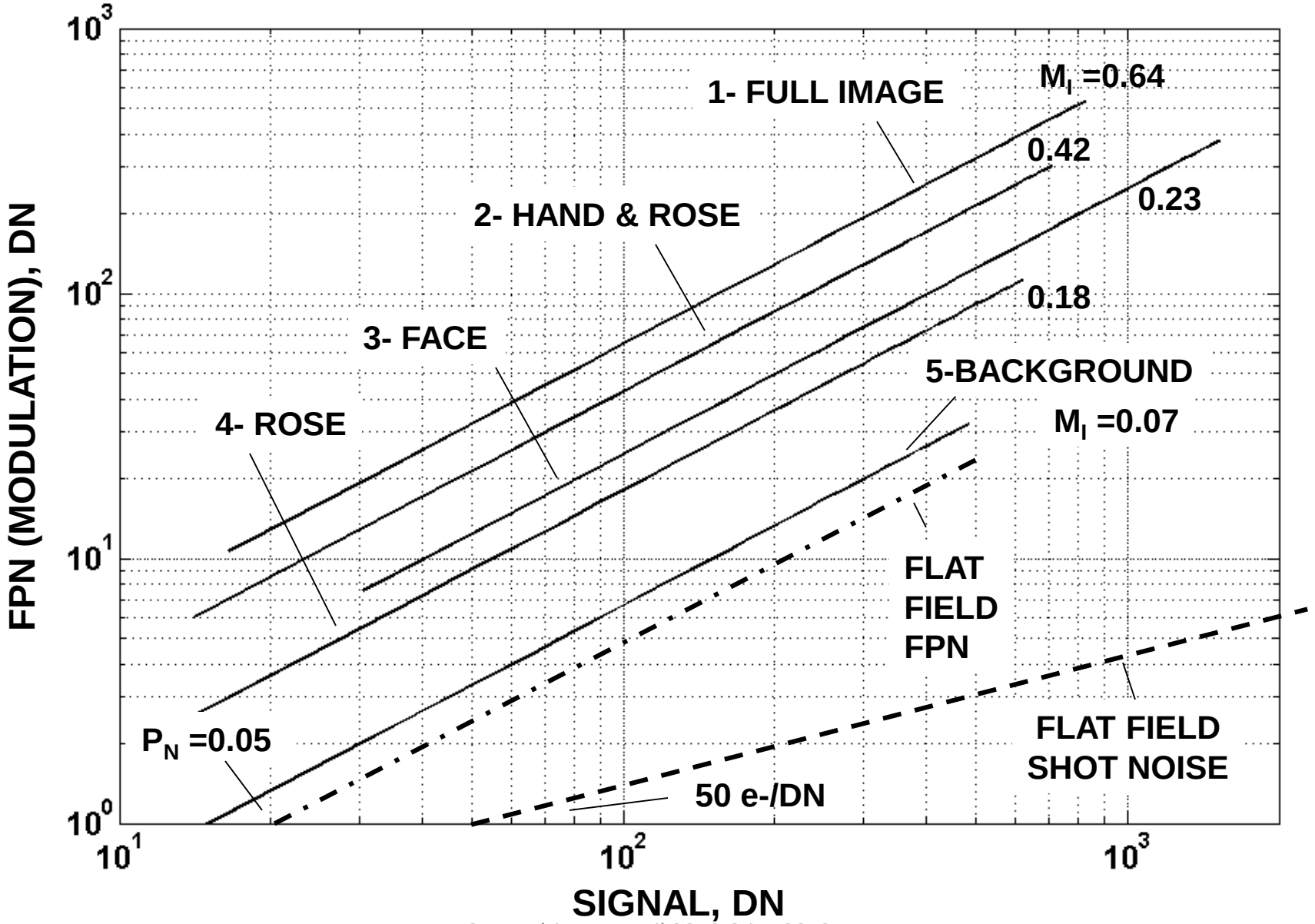




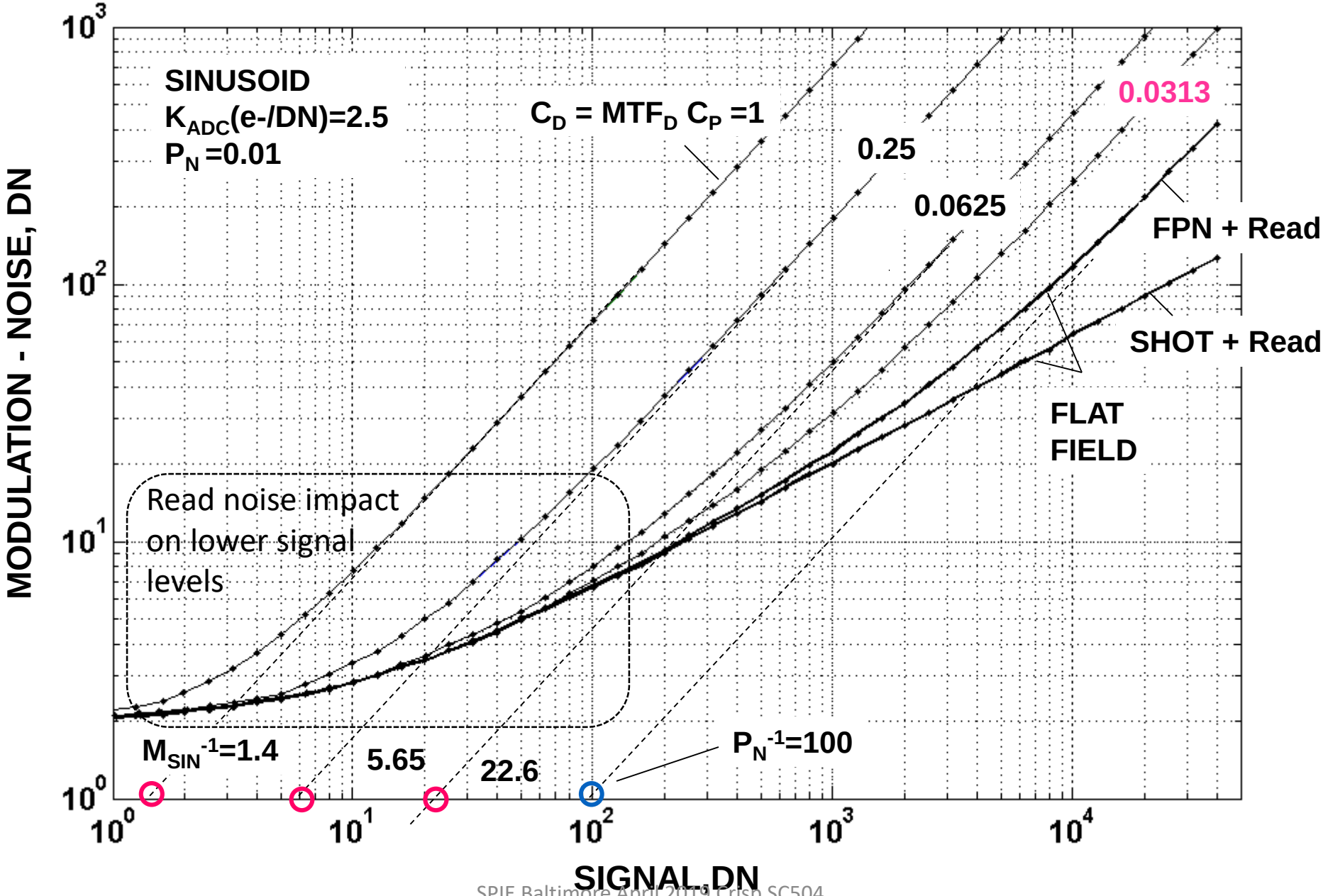




Modulation / Flat Field PTC

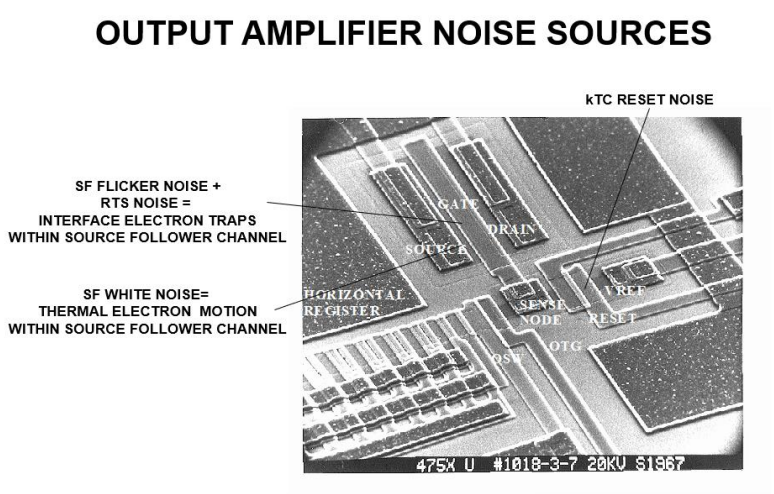


MODULATION AND FLAT FIELD PTC



PART 8
CMOS IMAGE SENSOR:
MAJOR PERFORMANCE DIFFERENCES VS CCD

CMOS: OFTEN LOWER READ NOISE THAN CCD

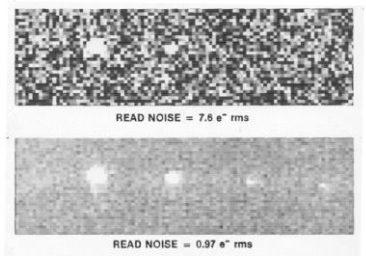


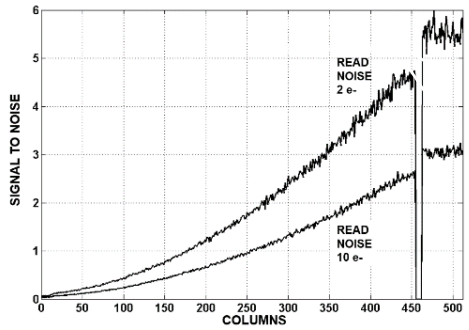
Source follower for CCD drives the off-chip load:
needs a big transistor

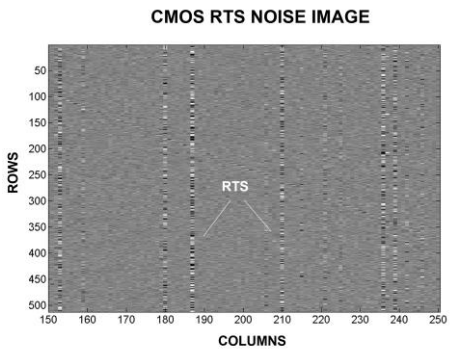
Trapping sites under large area gate electrode of source follower determine 1/F noise for CCD S-F. Large geometry transistor has many sites: behave as continuum of trapping-detrapping

Source follower for CMOS is in each pixel and drives small on-chip load: **uses tiny transistor**

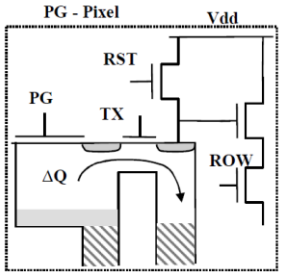
For CMOS, tiny S-F transistor has only small # trapping sites: lower noise & looks like discrete events
(called RTS: Random Telegraph Signal)



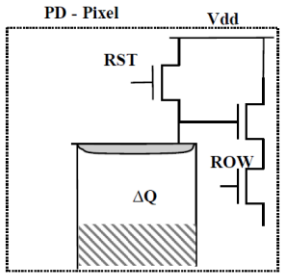




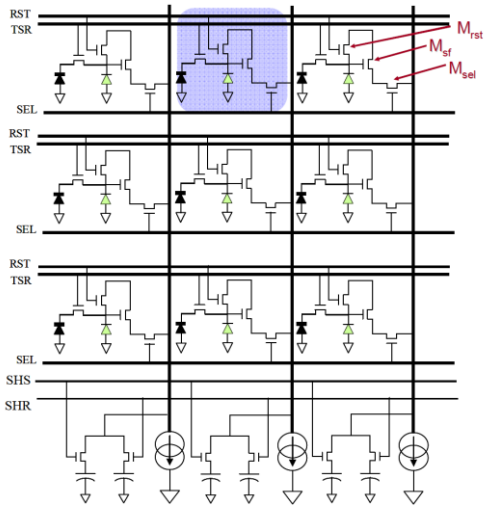
COMMON CMOS PIXEL ARCHITECTURES



4 Transistor
DCDS possible
(noise compensation)
Image Lag
Lower fill factor



3 Transistor
No DCDS
No Image Lag
Higher fill factor



On Chip Binning not feasible with this array design

Amplifier / ADC per column is possible
Can get very fast frame readout rates vs CCD, ie > 1000 frames/sec
Can you store that much data?
(**16Mpix * 1000 f/s** = 16Gigapixels/sec * 16bits/pix = **32Gbytes/sec**)

How many pins do you want and how much power is OK?

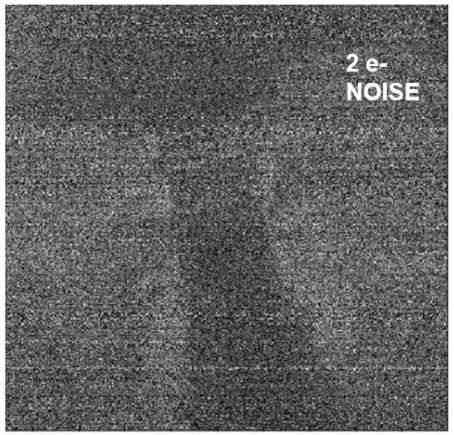
Many other architectures / features possible
Depending on pixel/array design
(global snap shutter, A/D per pixel for HDR etc)

CMOS IMAGE LAG

PPD IMAGE LAG

IMAGE

IMAGE LAG



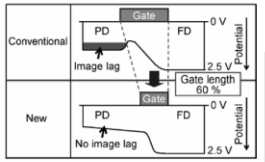
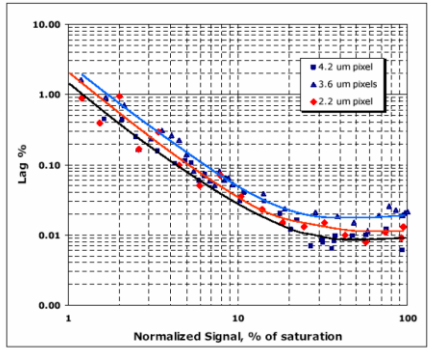


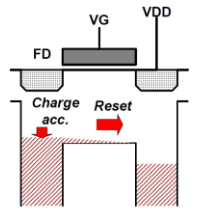
Image lag is a concern especially in small pixels operating at low voltages

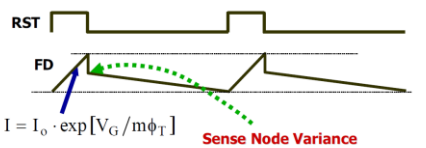
Difference in image lag shows up as pattern noise



RESET NOISE WITH "SOFT-RESET"

In steady state:
charge added during exposure = charge removed by reset





$I = I_o \cdot \exp[V_G / m\phi_T]$

Sense Node Variance

$$\sigma^2 = \begin{cases} \Delta n\ ; & \text{for } \beta \cdot \Delta n << 1 \\ \frac{kTC}{2}\ ; & \text{for } \beta \cdot \Delta n >> 1 \end{cases}$$

Source modulation: m ~ 1

$$\beta = \frac{q}{m \cdot C \cdot \phi_T} \qquad m = 1$$

- Soft-reset produces image lag
- May provide ultra-low noise in video mode w/o fast motion

Looks like CCD Residual Image but caused by different mechanism

IMAGE LAG

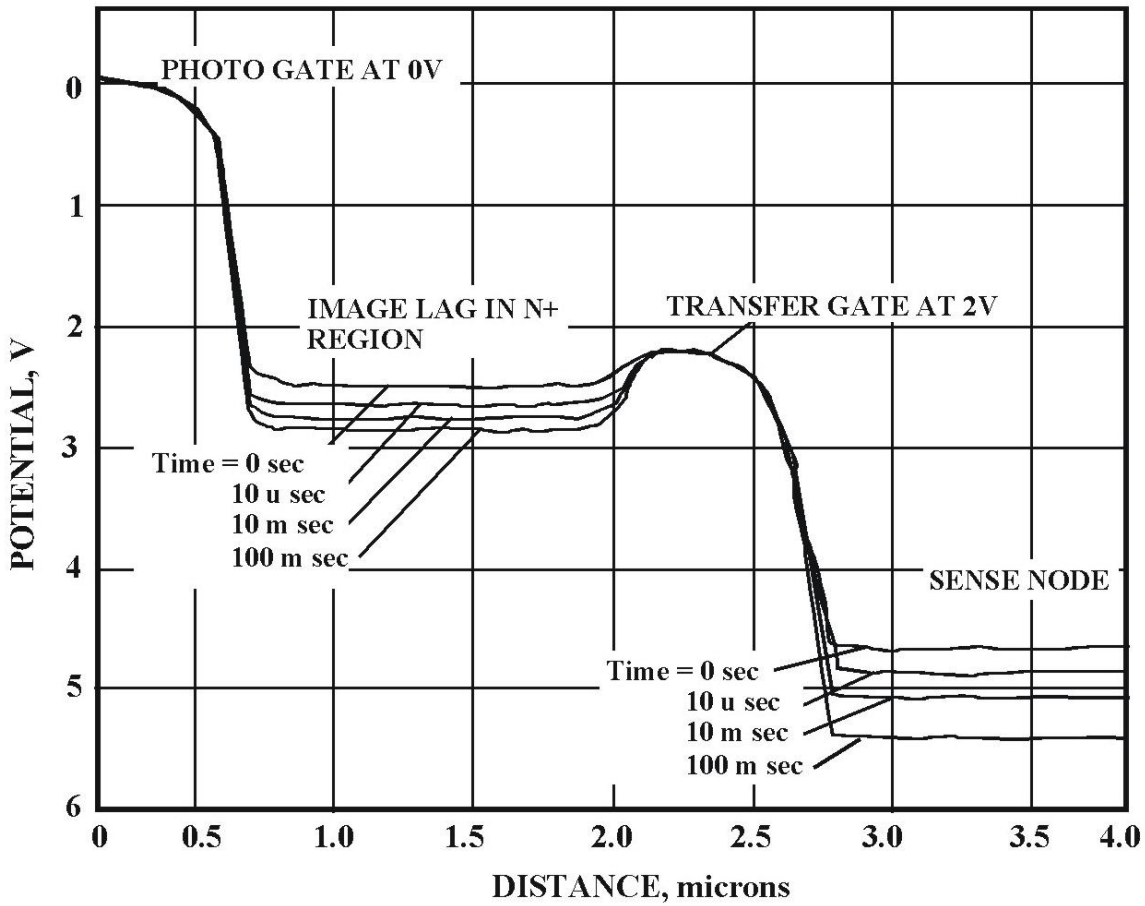
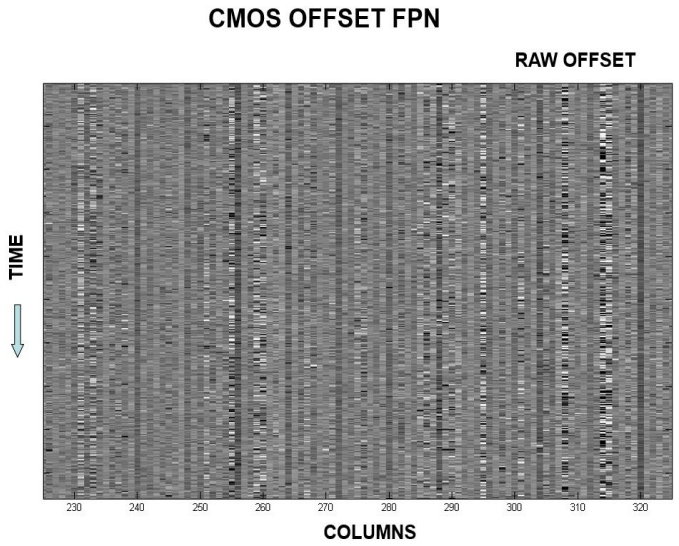
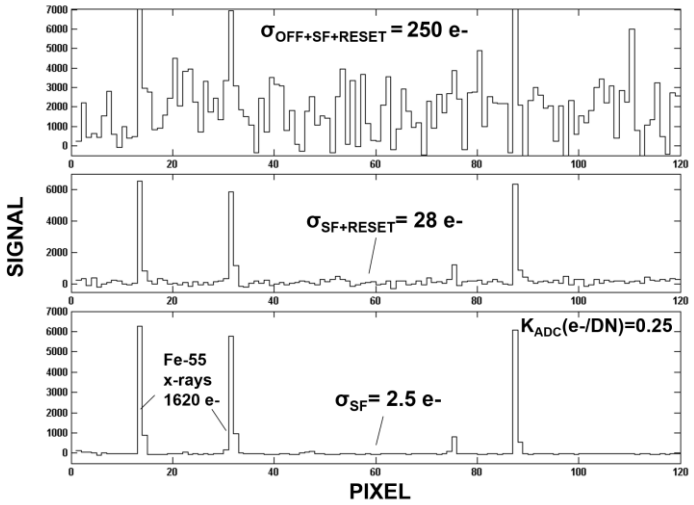


PHOTO GATE AT 0V
IMAGE LAG IN N+ REGION
TRANSFER GATE AT 2V
Time = 0 sec
10 u sec
10 m sec
100 m sec
SENSE NODE
Time = 0 sec
10 u sec
10 m sec
100 m sec
POTENTIAL, V
0
1
2
3
4
5
6
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
DISTANCE, microns

CMOS OFFSET & RESET FPN



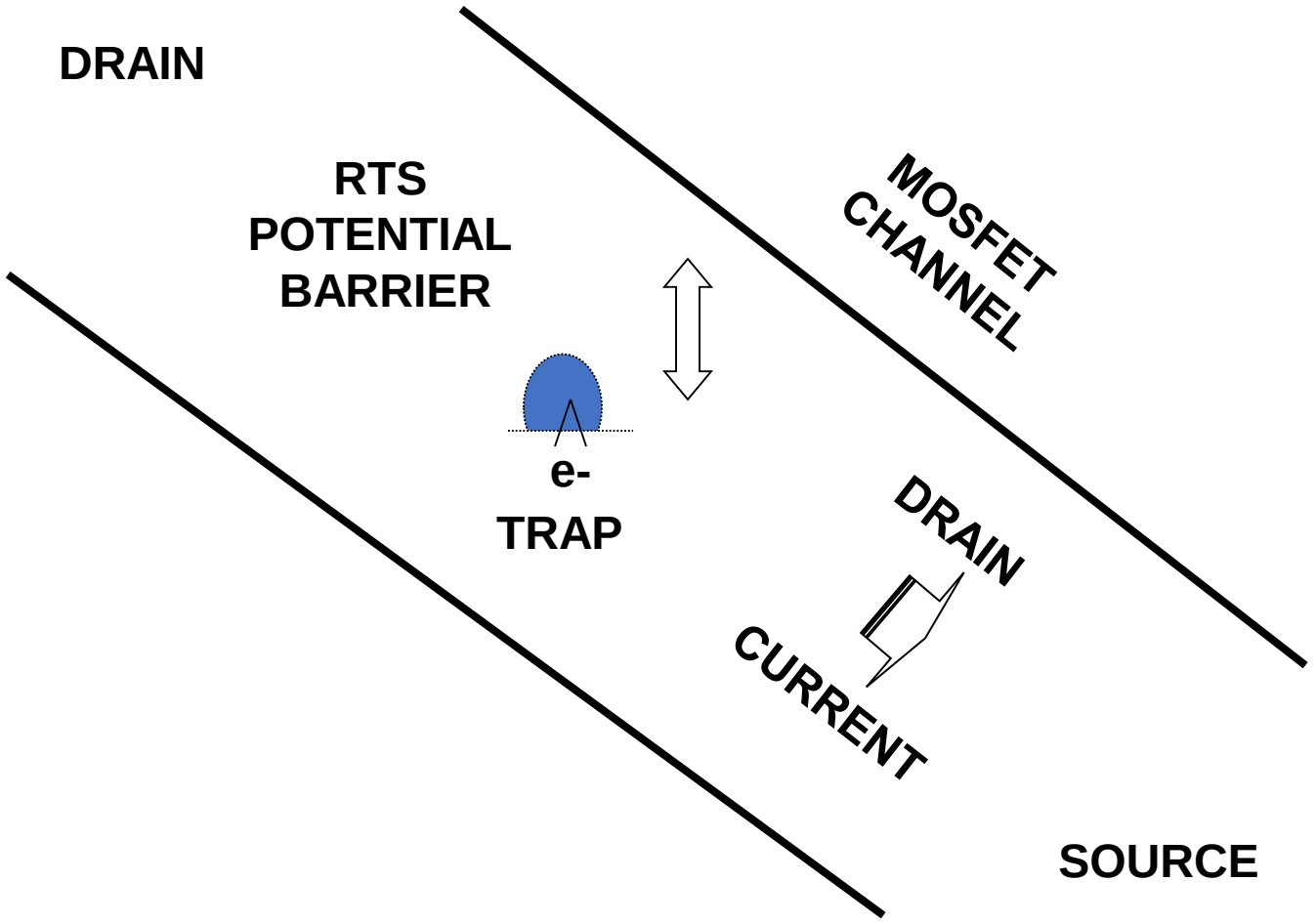


For most CMOS sensors, each pixel in a has its own amplifier
The offset value of each pixel amplifier is a little different resulting in pixel to pixel offset FPN.

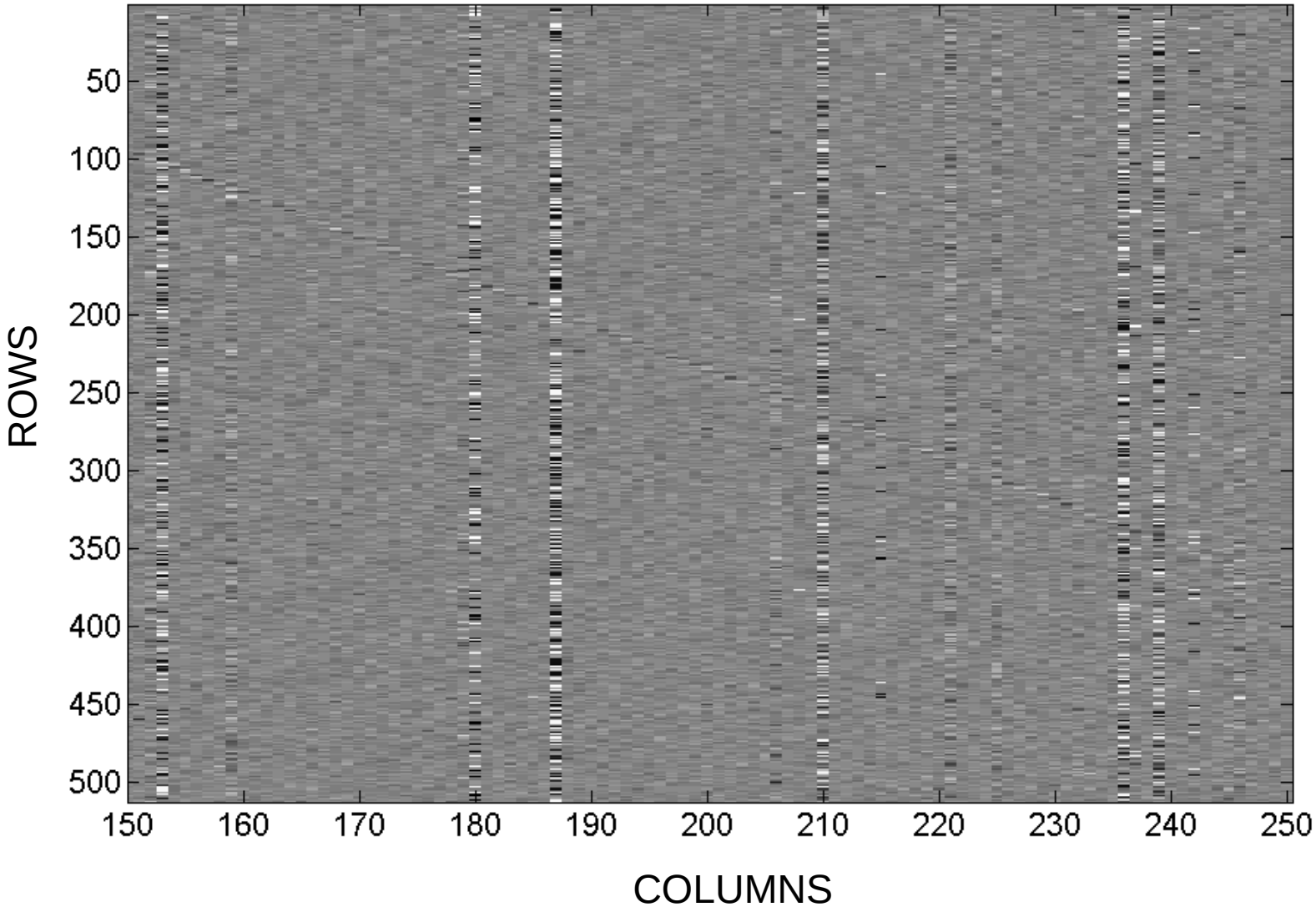
This can be removed on-chip depending on IC architecture
(DCDS, digital correlated double sampling)

CCD usually has 1 to 4 amplifiers only and off-chip CDS circuits are used

RANDOM TELEGRAPH SIGNAL AND FLICKER NOISE

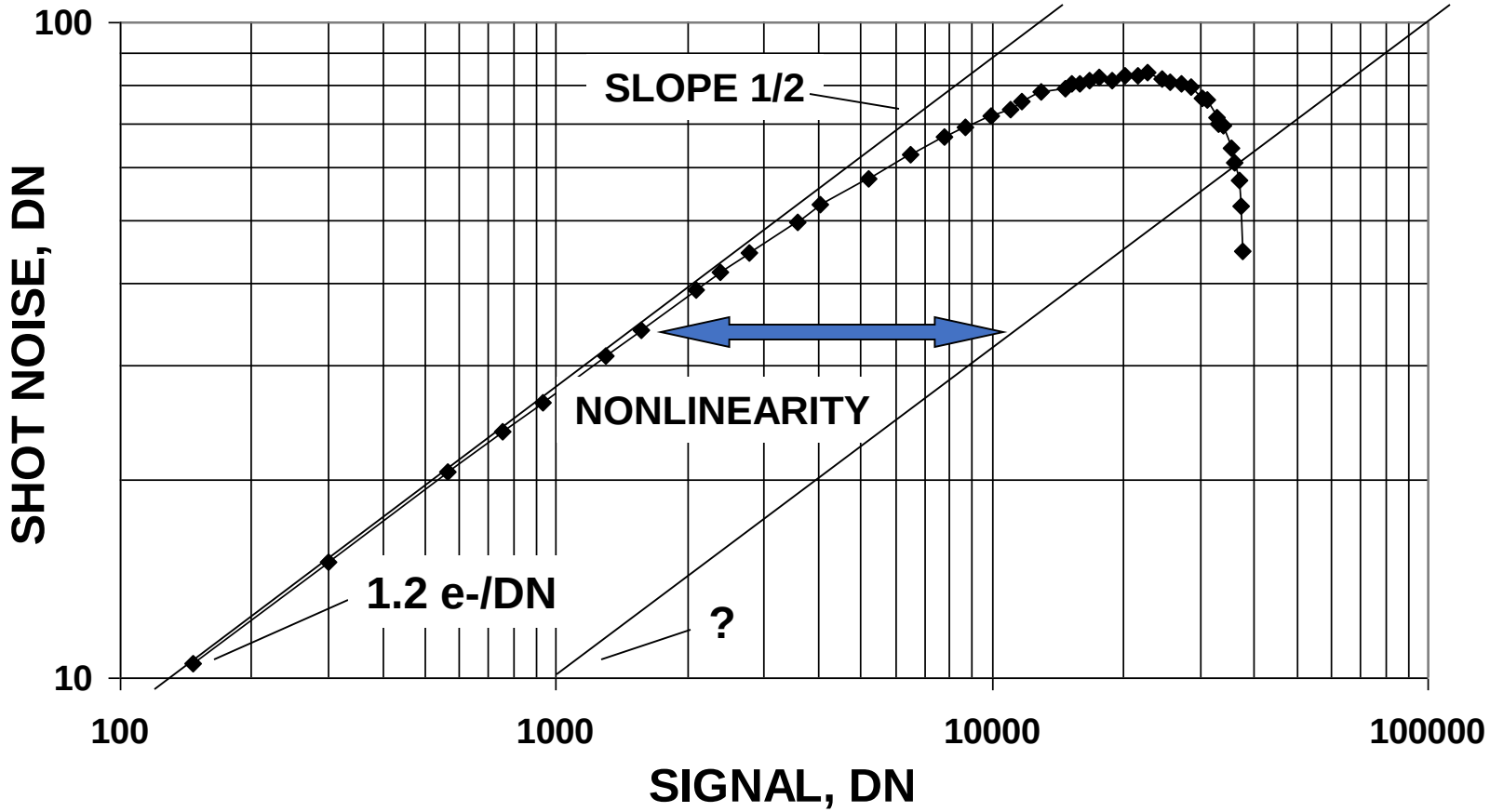


RTS NOISE IMAGE

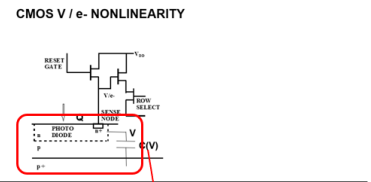


Ultimately RTS noise sets the noise floor for CMOS

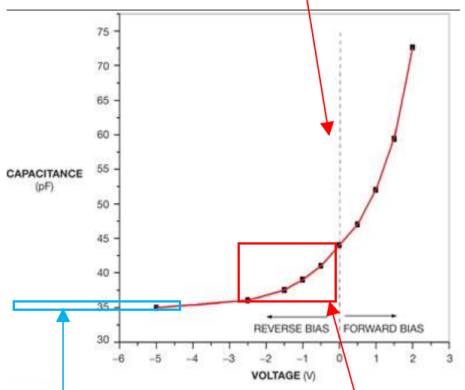
V/e- NONLINEARITY



CMOS: V/E NON-LINEARITY & FLAT FIELDING

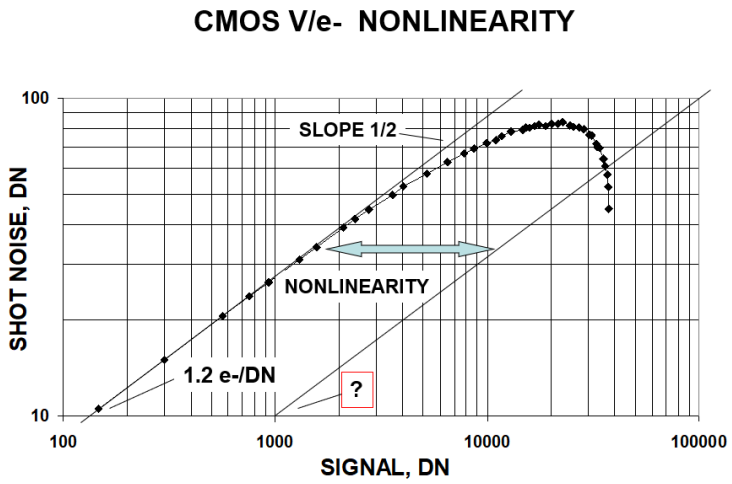


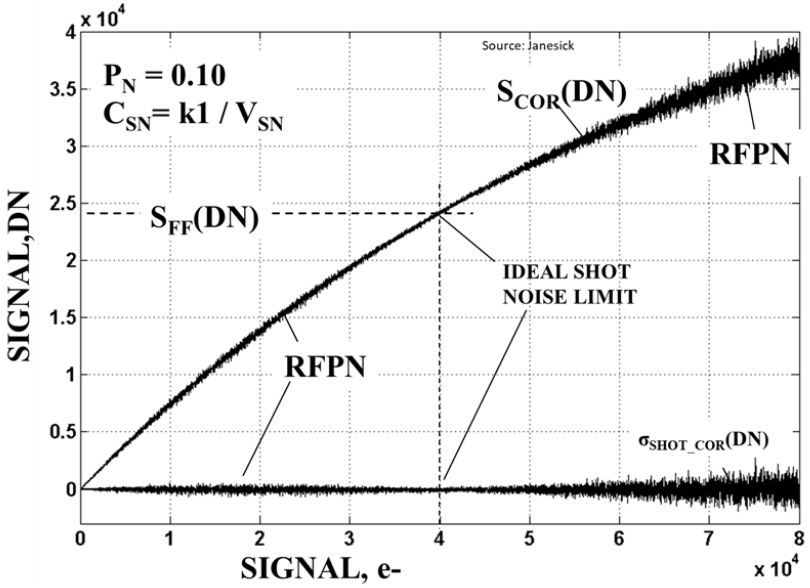
Reverse biased diode Capacitance vs Voltage (like sense node floating diffusion)



Typical CCD sense node voltage swings

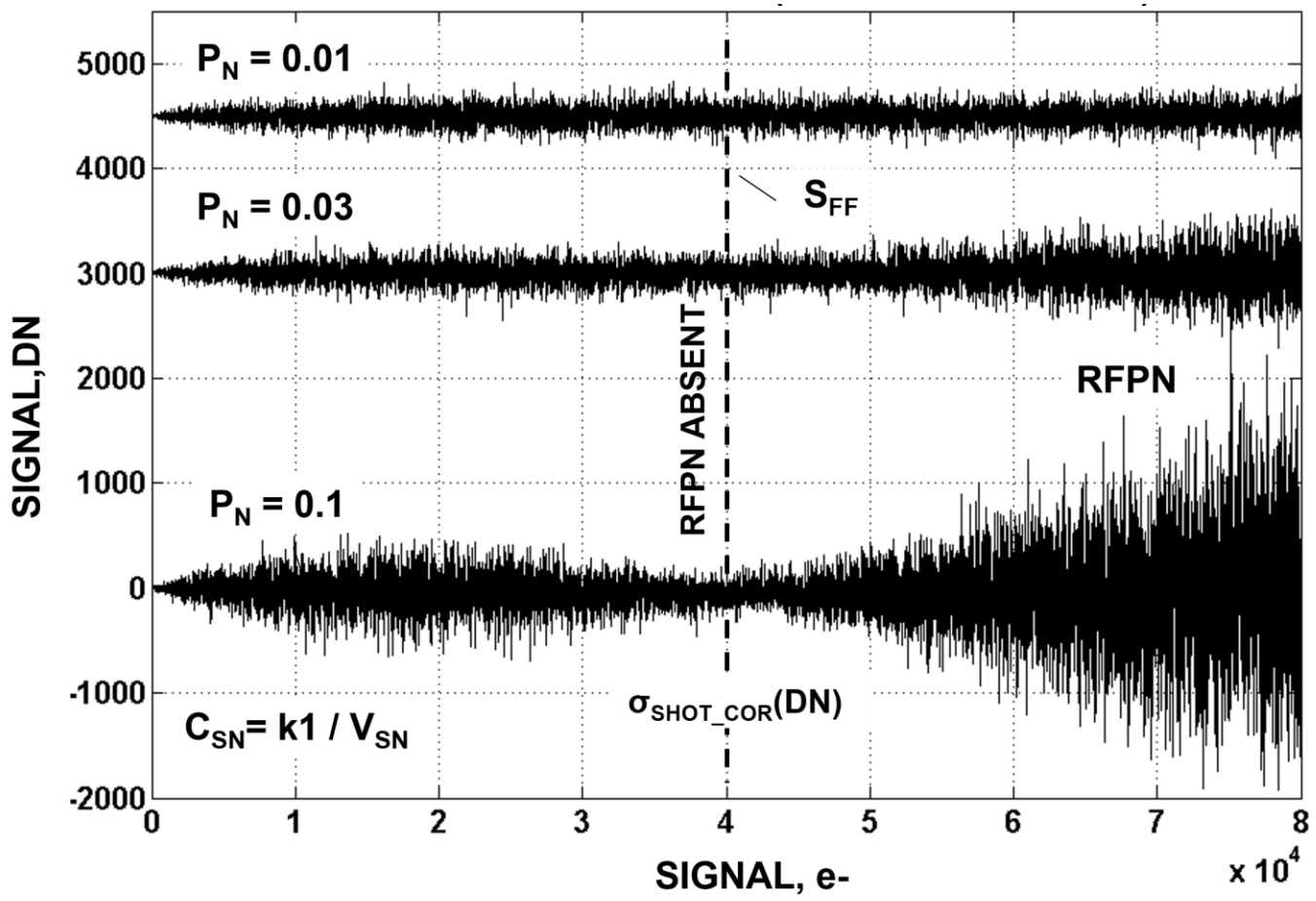
Typical CMOS sense node voltage swings





Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: REMNANT FPN



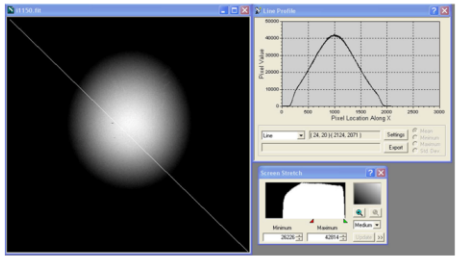
1%

IF PRNU is 1% or less flat fielding is effective in presence of V/e- nonlinearity

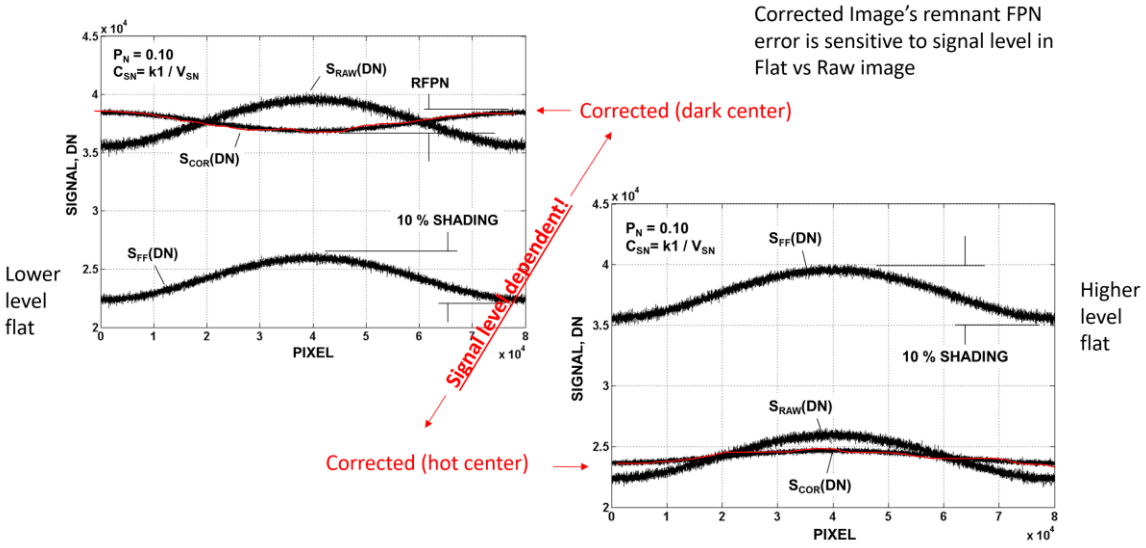
3%

For larger values of PRNU (ie lens cos^4 rolloff), flat fielding may not be 100% effective

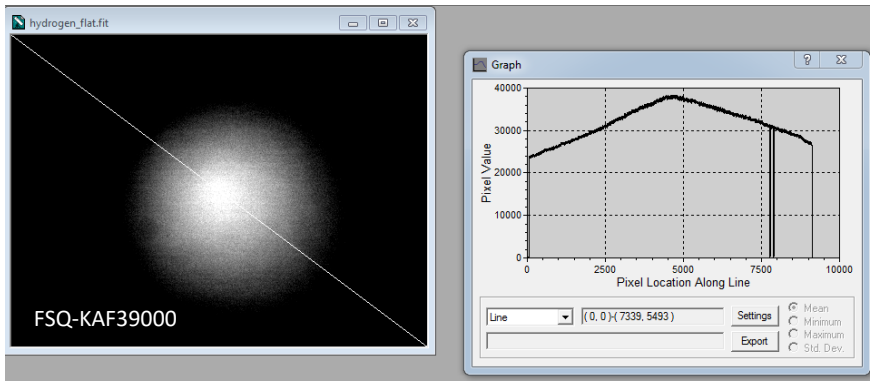
10%



CMOS: V/E NON-LINEARITY: FLAT/SIGNAL DEPENDENT REMNANT FPN



Imperfect flat fielding is the net result



>10% Lens shading/rolloff is not unusual for wide FOV – big sensor combo

SUMMARY

CMOS often has lower read noise than CCD

- Source follower noise is lower because transistor geometry is smaller
- Lower noise with equal QE results in less time to given SNR target

CMOS Sensors can be read at very high speed

- One or two Amplifiers & A/D per column is feasible for ultra fast frame rates (> 1000 frames/sec)
- Very difficult to store the high bandwidth data (32GByte/sec = 1000 frames sec of a 16 megapixel sensor with 16 bits/pixel)

Some CMOS pixel architectures suffer from image lag

- Reminds you of RBI but is a different mechanism
- Can be especially bad in high frame rate video applications

Some CMOS noise sources behave differently than CCD

- Each pixel has its own amplifier with its own offset and noise characteristics
    - Reset Noise
    - Offset FPN
        - Reset and Offset FPN can be corrected on-chip, depending on architecture
- RTS noise (ultimate noise floor)

CMOS nonlinearities can be more severe than CCD

- V/e- more severe vs CCD and that causes FPN to not be fully removed by flat fielding
- Can cause visible artifacts with as little as 10% lens intensity rolloff & high signal levels

Part 9
Manufacturing

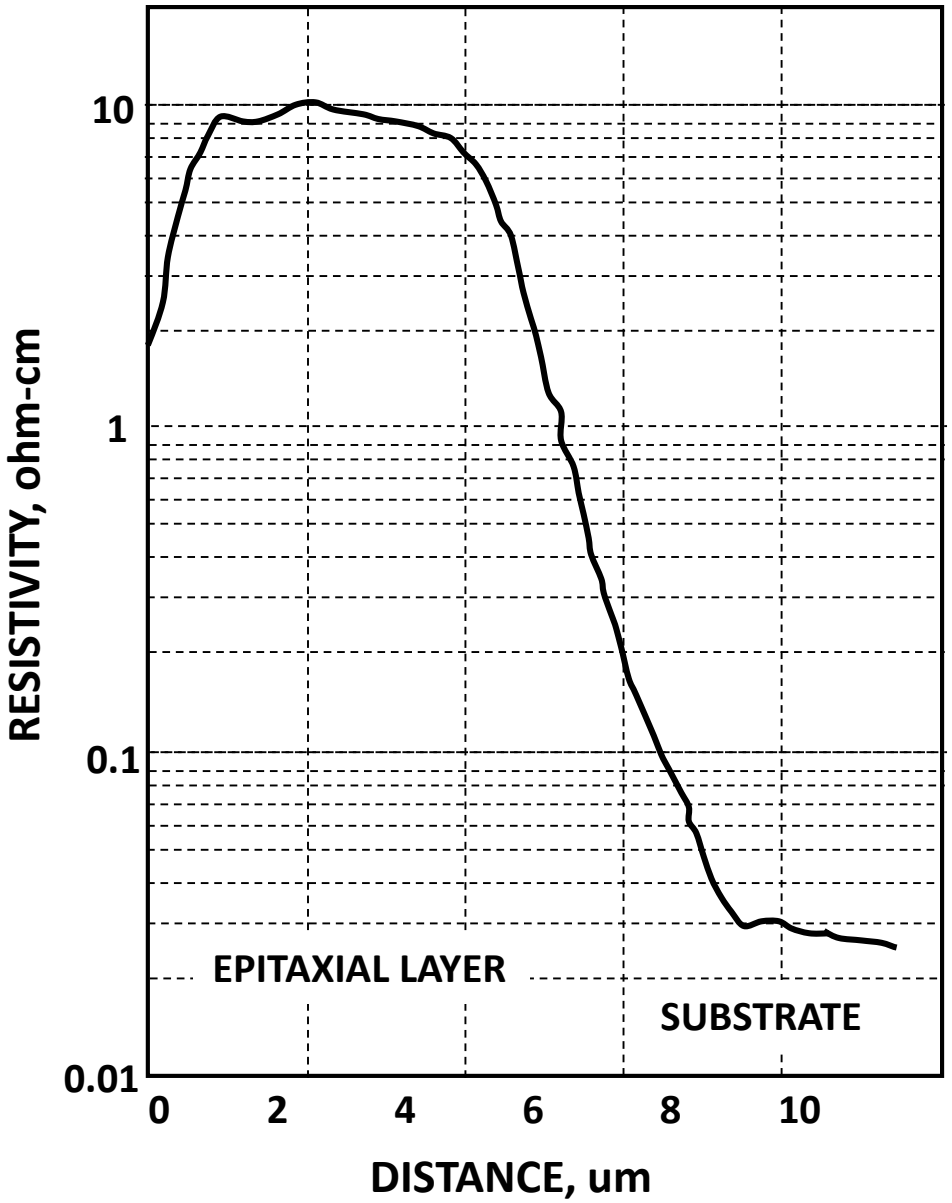
Manufacturing Issues

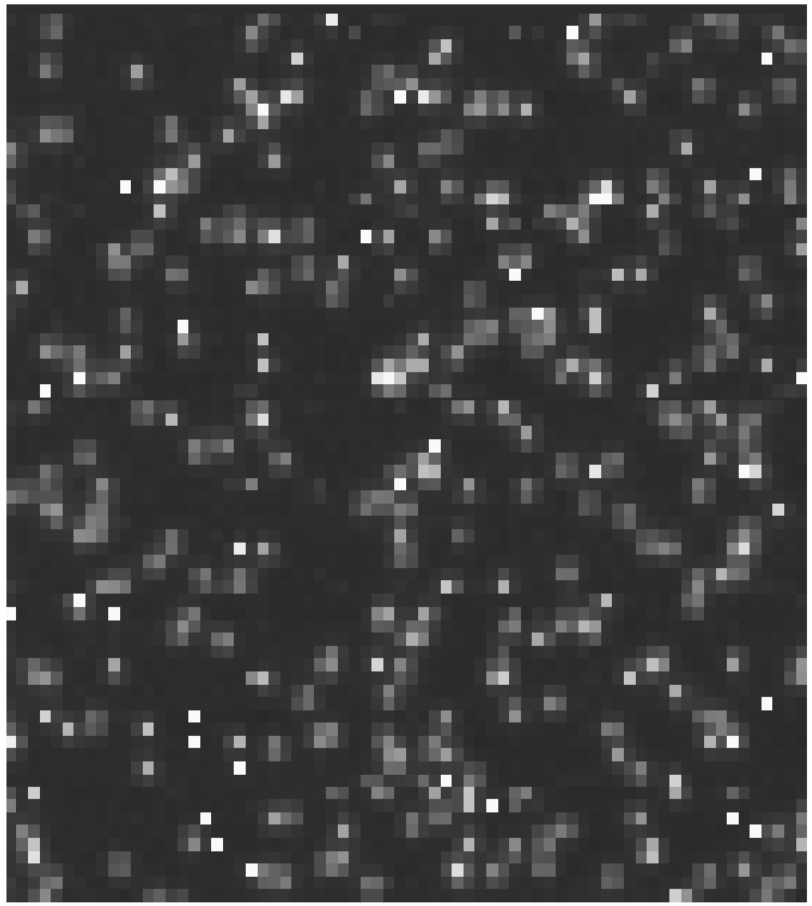
- Wafer Fab processes
  - Starting material: high resistivity epi or high resistivity wafers
  - Photolithography: maximum die size vs litho tool's FOV, stitched reticles & wafer size
  - Doping profiles versus logic (high resistivity device layer vs low)
    - Want deep depletion regions for good QE and MTF
  - No need for ultra small transistors (light doesn't scale)
  - Nice to have copper metallization vs Al to minimize interconnect/dielectric stack height (~65nm node)
- Backside Illumination
  - Thinning
  - Accumulation layer
- Die Stacking
  - Separate photosensing layer vs readout IC
    - Potential for compound semiconductor sensing layer (SWIR sensing)
    - Logic process vs photodiode process
    - Smallest possible footprint: set by photodiode array
    - Bumped surfaces vs TSV?
  - Include memory (DRAM) in stack?
    - Three die stack, with buffer DRAM
      - High speed Rolling Shutter: minimize tearing
      - Very high speed for slow motion
      - Fill DRAM fast then readout at link speed

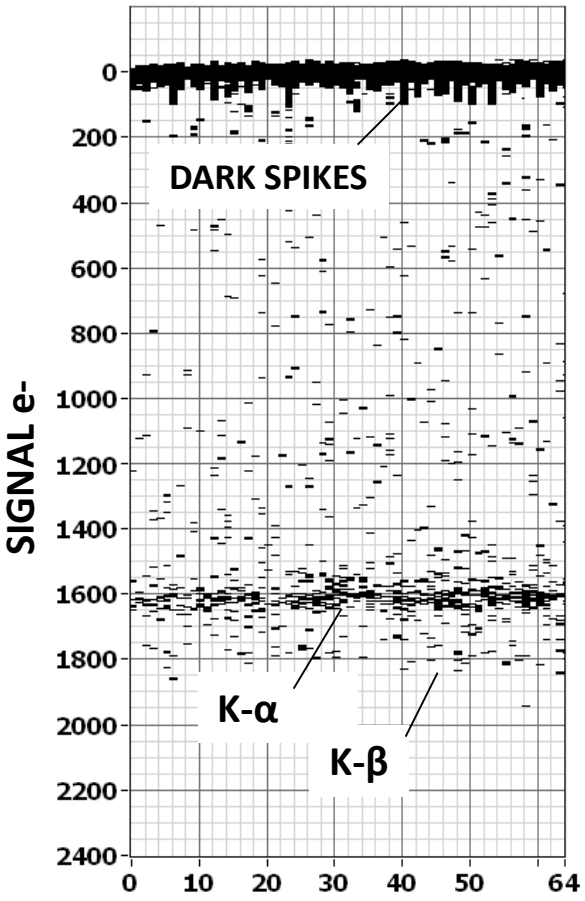
Starting Material

COMMERCIAL CMOS SILICON

(Fe-55 X-RAY)





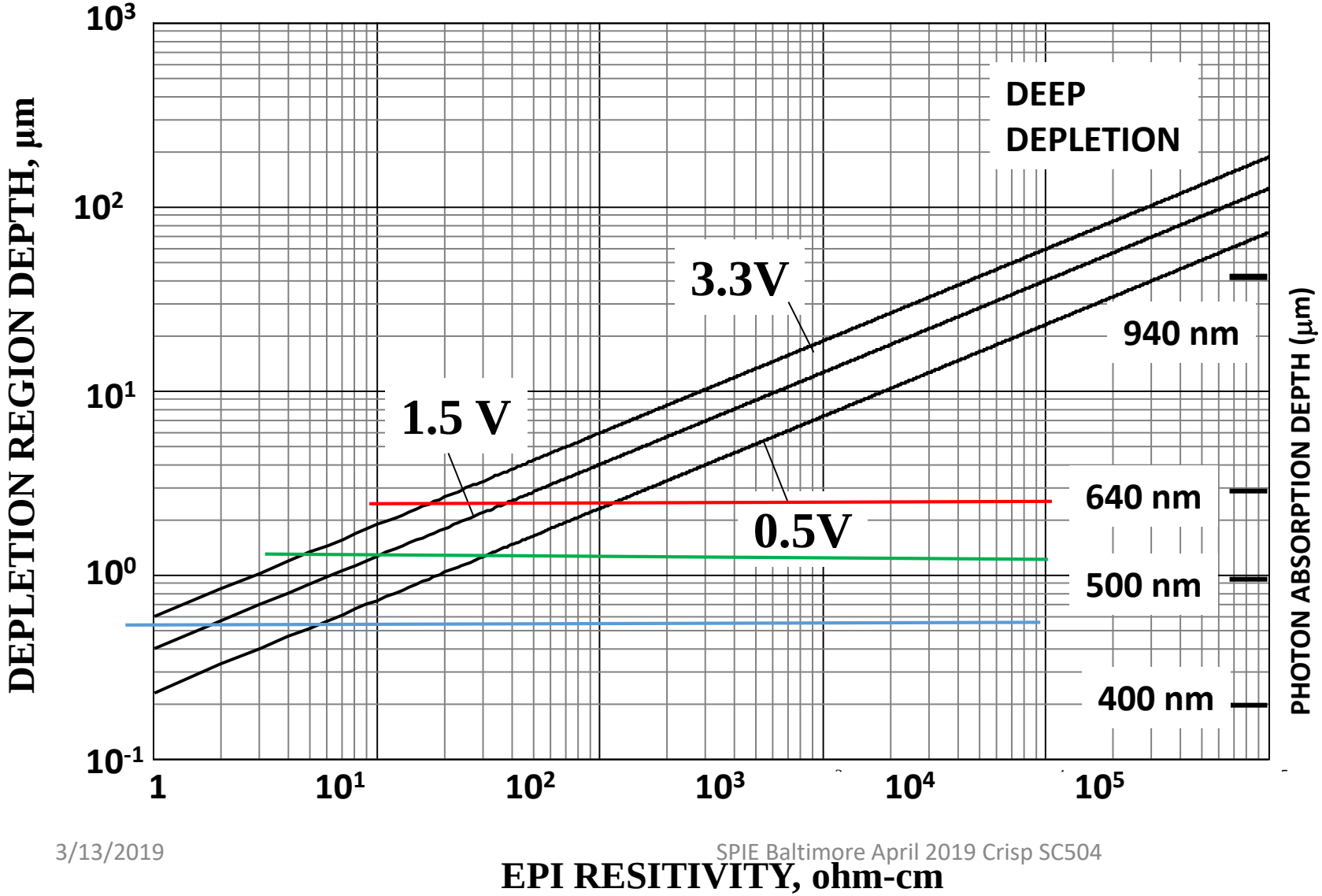


10 ohm-cm

Many split events: many h-e pairs generated in field free region

Starting material / epi resistivity

At what wavelength is it OK to sacrifice MTF?



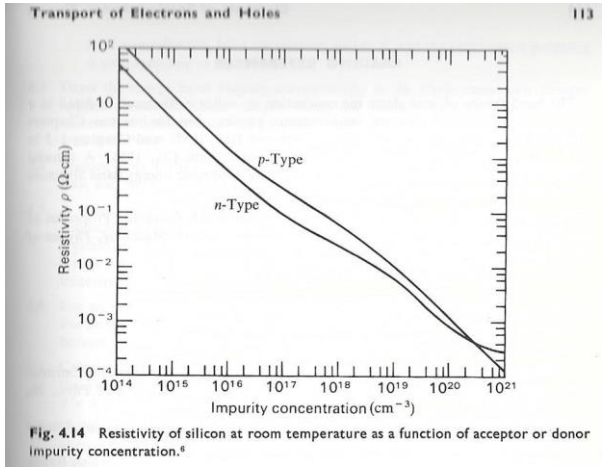


Fig. 4.14 Resistivity of silicon at room temperature as a function of acceptor or donor impurity concentration.[6]

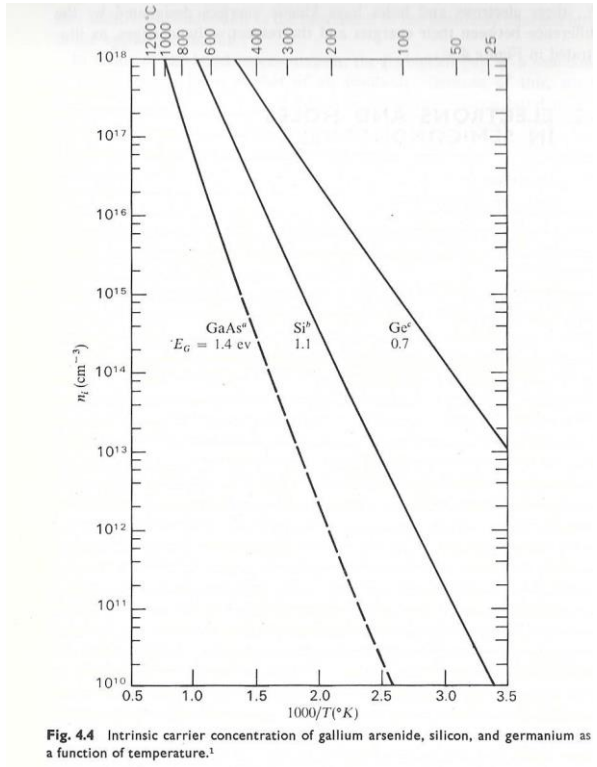
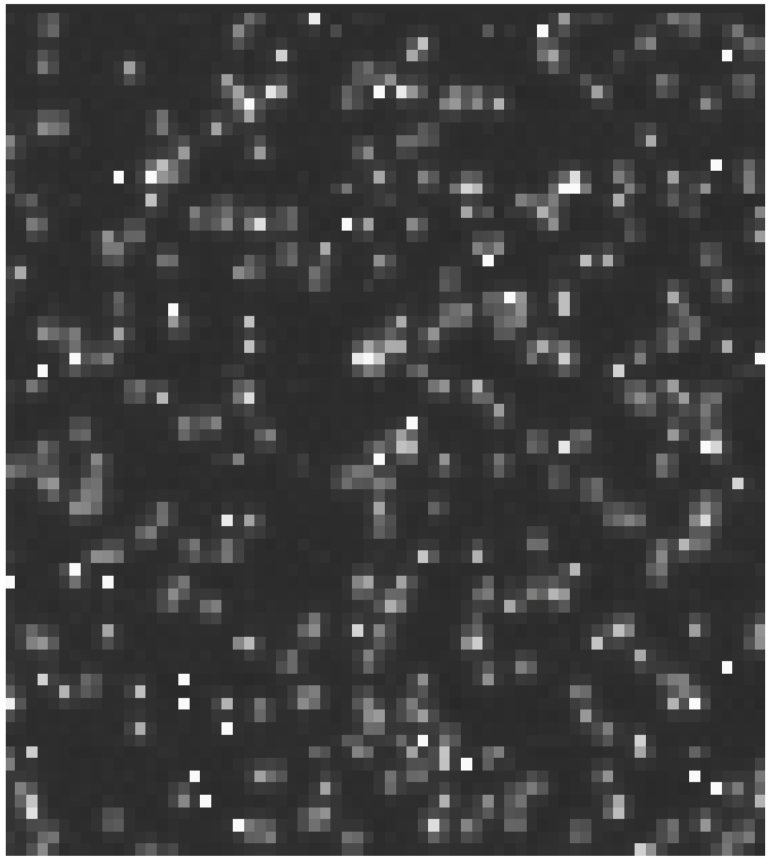


Fig. 4.4 Intrinsic carrier concentration of gallium arsenide, silicon, and germanium as a function of temperature.[1]

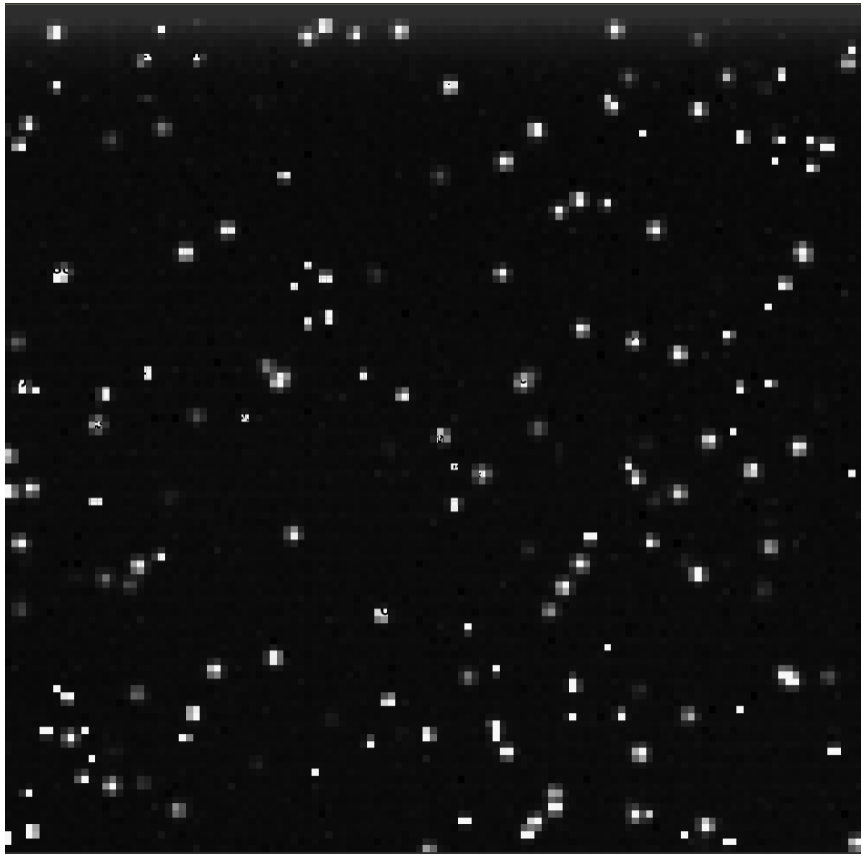
Fe- 55 X-RAY EVENTS

8 um PIXELS



10 ohm-cm

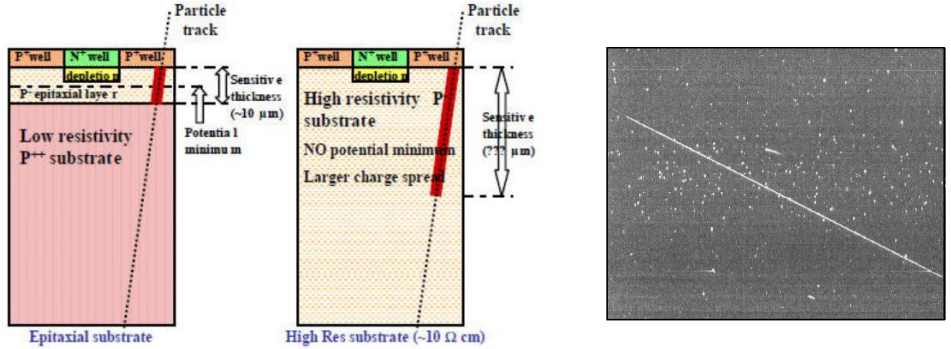
Note large number of split events



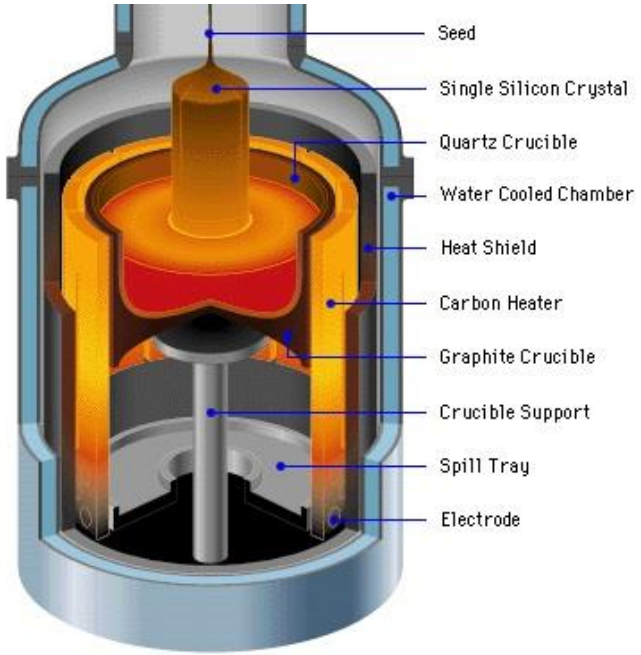
MINIMAL ARRAY
Fe- 55
15 µm EPI (30,000 ohm-cm)

Wafer Starting Material: Czochralski, Float Zone, EPI?

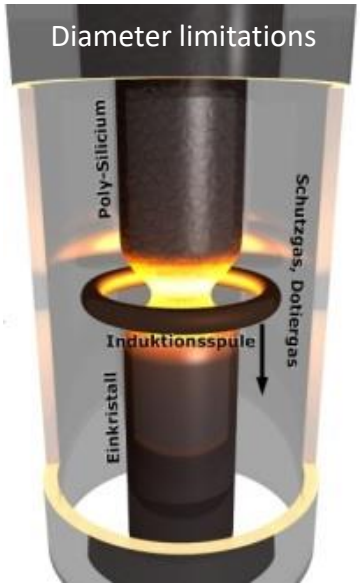
High resistivity silicon is defined as monocrystalline silicon having a bulk resistivity larger than 1 kΩcm. Although Czochralski grown monocrystalline silicon is often specified up to 1.5 kΩcm, Float Zone grown monocrystalline silicon is the only growth technology that is able to have bulk resistivitites above 1 kΩcm with good tolerance control of the resistivity along the ingot from where the silicon wafers is sliced. Topsil manufactures and sells Float Zone grown high resistivity silicon (HiRes™) with bulk resistivities approaching 70 kΩcm. Furthermore, the company's properiatary knowledge of keeping the radial resistivity variation low makes Topsil high resistivity ingots and wafers excellent candidates for future GHz & THz technologies based on silicon.



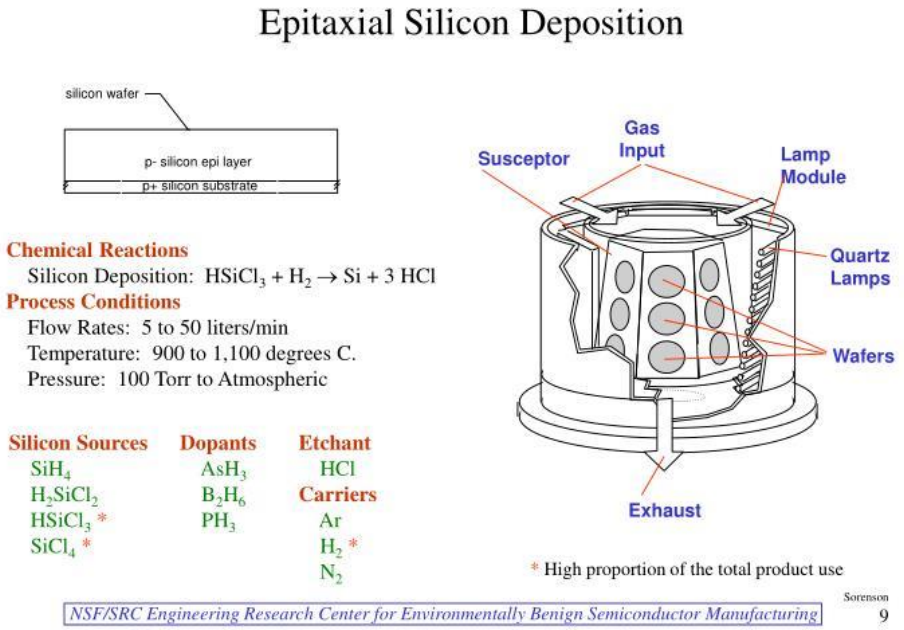
Epi more immune to radiation hits



Czochralski (cheapest)

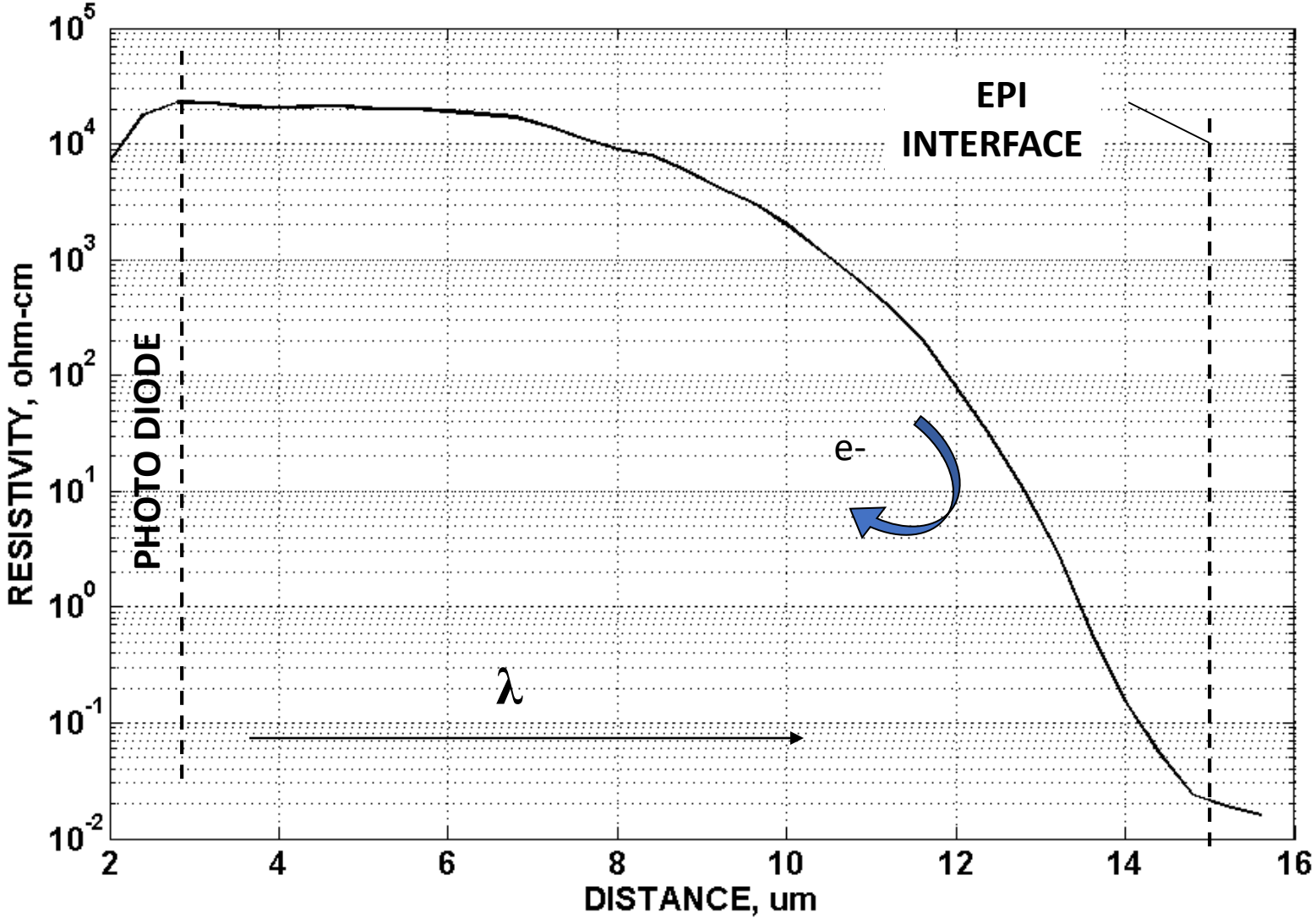


Float Zone (ultra pure)

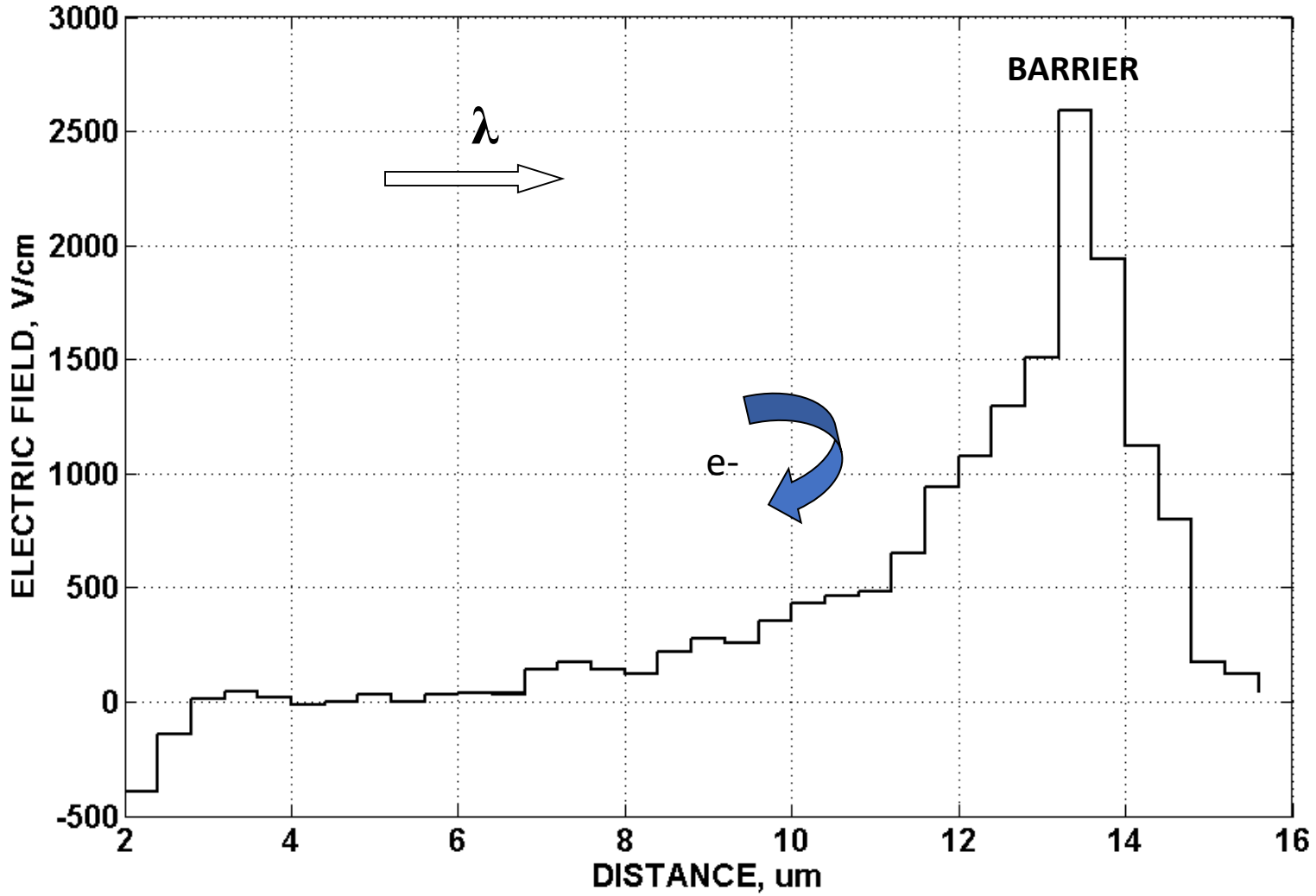


Epitaxy

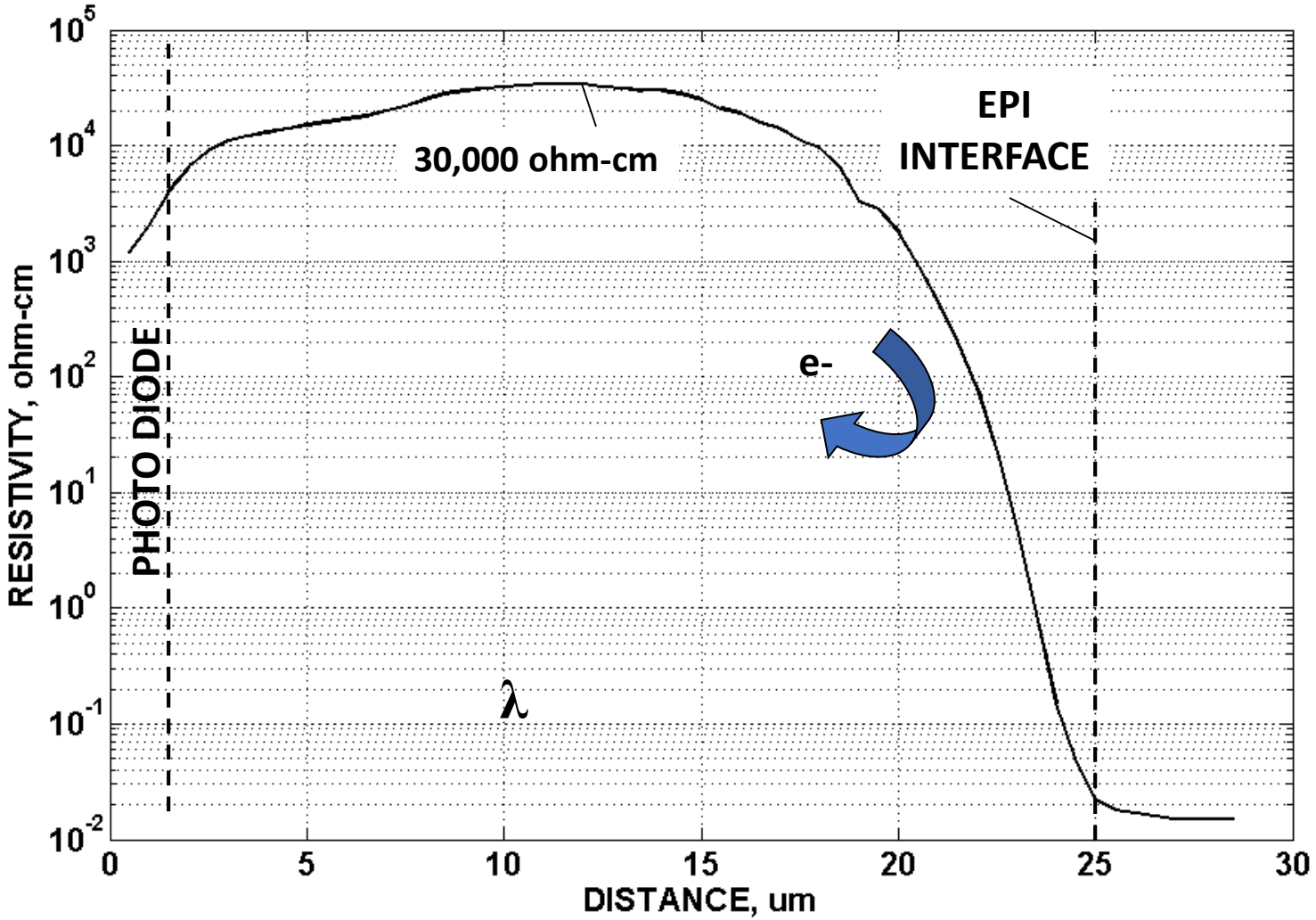
HIGH RESITIVITY EPI SILICON



HIGH RESITIVITY EPI SILICON



HIGH RESITIVITY EPI SILICON



Lithography

Lithography

- Possible to make a single big chip per wafer up to 150 mm wafer size
  - Industry used “Projection” printers: illuminates entire wafer with a single exposure flash
- When industry switched to 200 mm and later to 300 mm wafers, they switched lithography tools to “Steppers” and “Scanners”
  - These tools use multiple exposure flashes per masking layer
    - They Step and Scan/Repeat across the wafer exposing at each stop
    - The “reticle” printed at each step is of limited size (25 x 25 mm is common)
    - Only feasible way to make a big die is to use “stitched” reticle (ie 2x2 mosaic)
      - 4x the # of expensive photomasks needed
      - ¼ the wafer fab throughput
- Big CCDs are still built using 150 mm wafers and projection printers
- Most CMOS sensors are made on 200 mm or 300 mm wafers and therefore usually have a limit of about 25 x 25 mm maximum reticle (cluster of die) size

Lithography

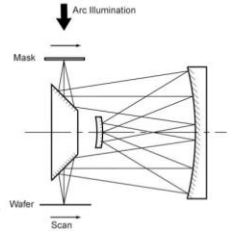


Figure 5. Canon MPA-500FA (1978)

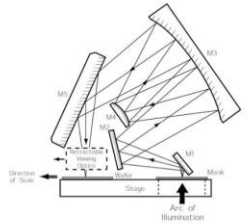


Figure 6. Cobilt CA 3000 (1978)

A larger, final evolution of the Micralign is shown in Figure 7. This system, commercialized in 1984, had no fold mirrors, but an annular field large enough to sweep out a 6" wafer.

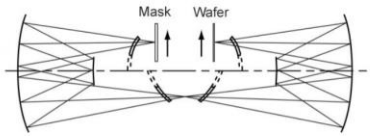


Figure 7. Perkin Elmer Micralign 500 (1984)

Several other approaches to 1:1 printing were attempted with varying degrees of success. The Micralign systems were ultimately limited by overlay, primarily because there were few practical methods to compensate overlay errors over a large wafer. In 1976, Bell Laboratories developed several prototypes of a 2-dimensional Scanning Projection Printer[6] (SPP) as shown in Figure 8.

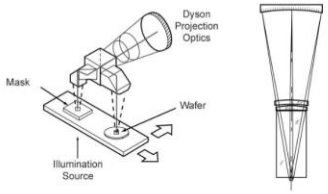


Figure 8. Bell Labs 1:1 Scanning projection printer (1976)

Various projection systems

3.2. High-NA step-and-scan reduction lithography: 1990 – 2004

Demand for still-higher resolution and throughput drove lithography tool makers to further enlarge the image field by stepping *and* scanning the image. Scanning afforded the opportunity to increase image field *coverage* without increasing the *natural* field size of the lens. In 1990, Perkin Elmer introduced the first step-and-scan system, the Micrascan I[10]. This system had an annular image field, but a complex optical system with many folds, as shown in Figure 11. This system was very difficult to manufacture. Three years later, the system was replaced by the SVGL Micrascan II, shown in Figure 12. The MS-II design was a more manufacturable folded catadioptric design that enabled scanning a narrow, rectangular strip image which reduced the throughput loss from over-scanning an annular image field. Multiple generations of the Micrascan are summarized in Table 2 and reference 11.

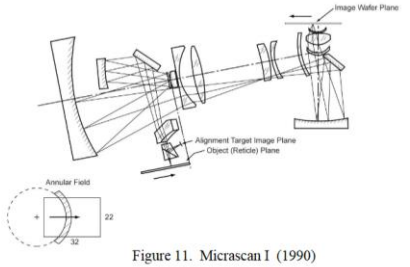


Figure 11. Micrascan I (1990)

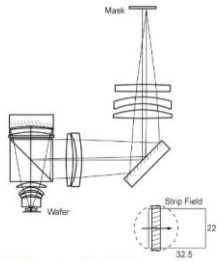


Figure 12. Micrascan II (1993)

Table 2. Evolution of PE/SVGL Micrascan step-and-scan systems (1990 – 2003)

Year	Model	Image Area (mm x mm)	λ (nm)	NA	CD_{min}(nm)	N
1990	MS-I	22mm x 32mm - Annular	250 lamp	0.35	350	5.6×10^9
1993	MS-II	26mm x 50mm - Strip	250 lamp	0.50	250	2.1×10^{10}
1997	MS-III	26mm x 50mm - Strip	248 KrF	0.60	200	3.2×10^{10}
2001	MS-V	26mm x 50mm - Strip	193 ArF	0.75	130	7.7×10^{10}
2003	MS-VII	26mm x 50mm - Strip	157 F_2	0.75	100	1.3×10^{11}

Various Stepper & Stepper/Scanner Systems

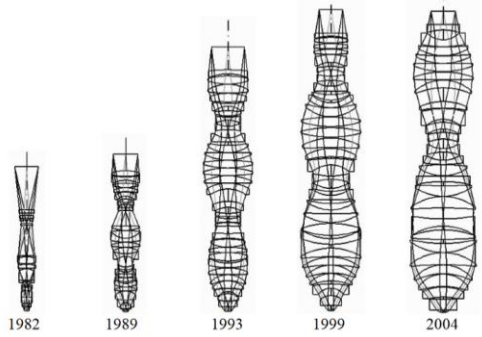


Figure 13. Nikon lithography lenses

Table 3.

Year	Image Area (mm x mm)	λ (nm)	NA	CD_{min}(nm)	N
1982	15mm x 15mm - Stepper	436 lamp	0.30	1200	1.6×10^8
1989	15mm x 15mm - Stepper	435 lamp	0.54	660	5.2×10^8
1993	22mm x 22mm - Stepper	365 lamp	0.57	450	2.4×10^9
1999	26mm x 32mm - Scanner	248 KrF	0.68	200	2.1×10^{10}
2004	26mm x 32mm - Scanner	193 ArF	0.85	82	1.2×10^{11}

3.3. Ultra-high NA and immersion imaging (2003 – Present)

In early 2000, lithography faced an even greater challenge keeping up with Moore's Law. Both 157nm and 193nm wavelengths were being developed along with other optical and non-optical approaches with no obvious long-term choice. By 2003, 157nm was written off as an impractical next step in optical lithography after 193nm. Optical lithography demonstrated tremendous staying power and accumulated an enormous investment in its supporting infrastructure and technologies. Besides advancements in wavelength and numerical aperture, further resolution improvements have come about as a result of improved mask, wafer and process integration that allow lithography systems to operate at smaller values of k_1. Figure 14 illustrates the progress in exploiting optical lithography at lower k_1 values over a period of nearly 15 years[15]. The cross-features with their overlayed aerial images to the right of the Figure show the impact on the aerial image when the cross feature is printed, at that particular k_1 value, without compensation or resolution extension techniques.

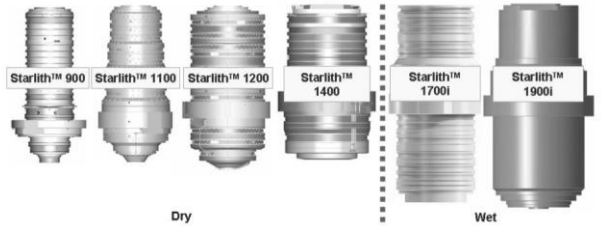


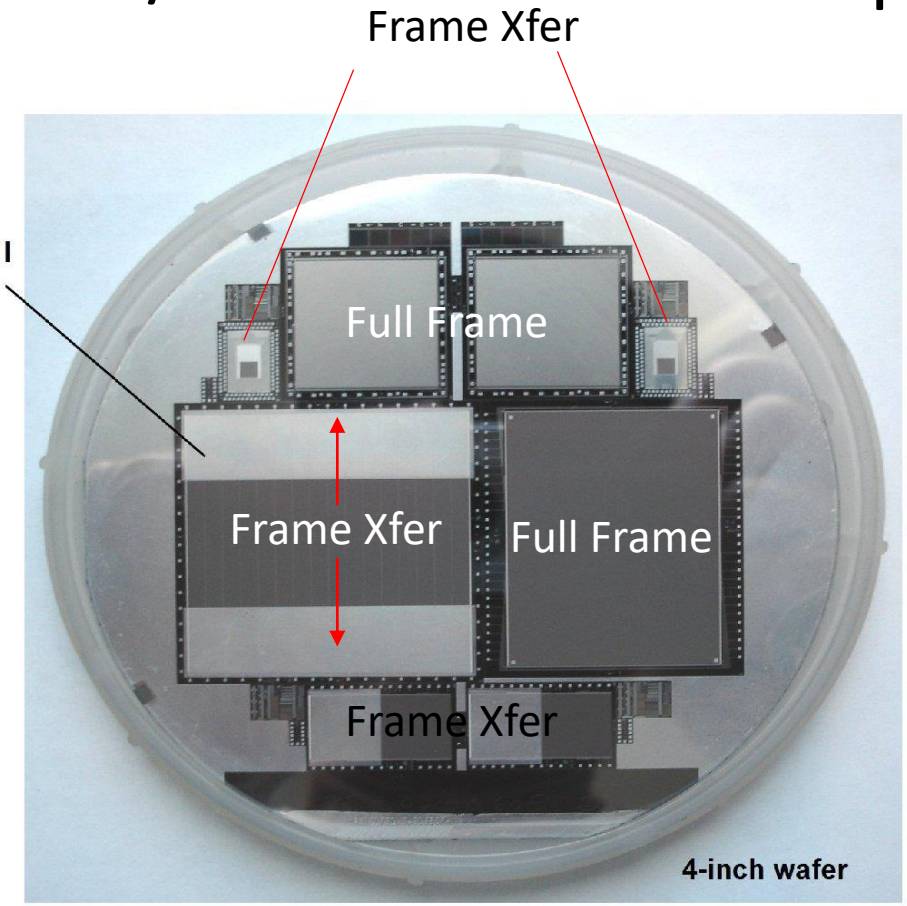
Figure 16. 193nm lens evolution at Carl Zeiss

Table 4. Parameters of Zeiss Lens

Model	900	1100	1200	1400	1700	1900
Node, CD_{min}	130	100	80	65	50	45
NA	.63	.75	.85	.93	1.20	1.35
k_1 Factor	.42	.39	.35	.31	.31	.31
N	4.9×10^{10}	8.3×10^{10}	1.3×10^{11}	2.0×10^{11}	3.3×10^{11}	4.1×10^{11}

Various Stepper & Stepper/Scanner Lenses

Projection/Scanner vs Stepper/Scanner



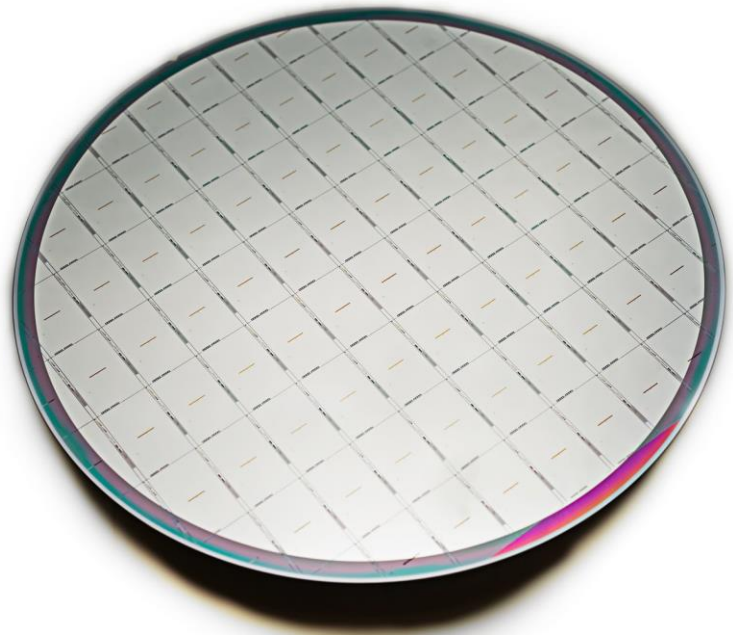
CINEMA CCD
4096(V) x 4096(H) x 9 um pixels
16 output amplifiers

First of its kind, the imager was intended to replace photographic film used in cinematic moving picture cameras. Future versions of the Cinema CCD were later fabricated and tested (Cinema II below).

RETICON fabricated

Projection/Scanner Printer, 100 mm wafer

Up to & including 150mm diameter wafers

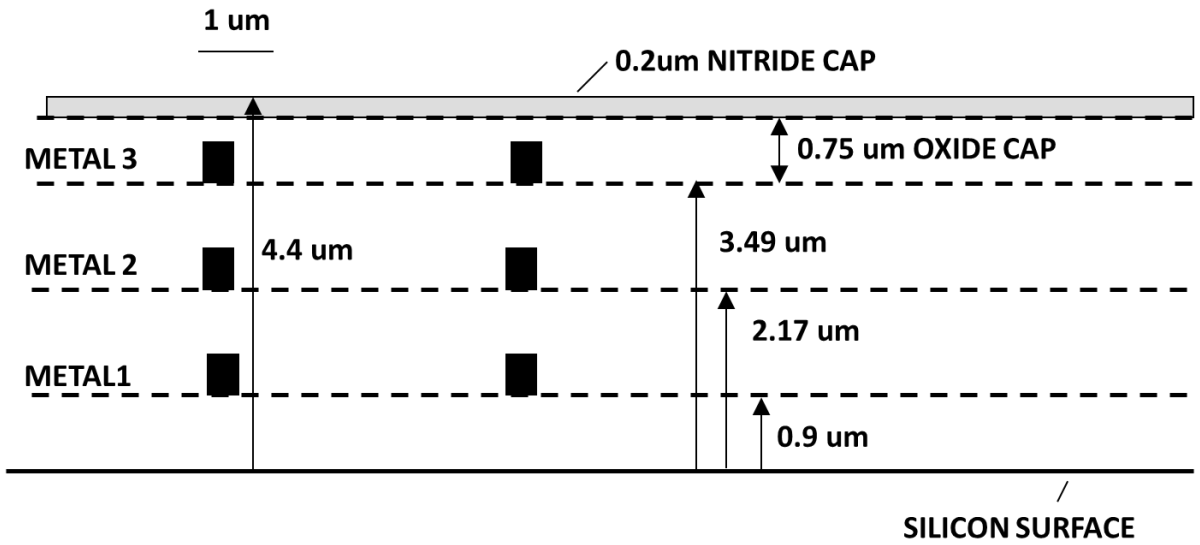


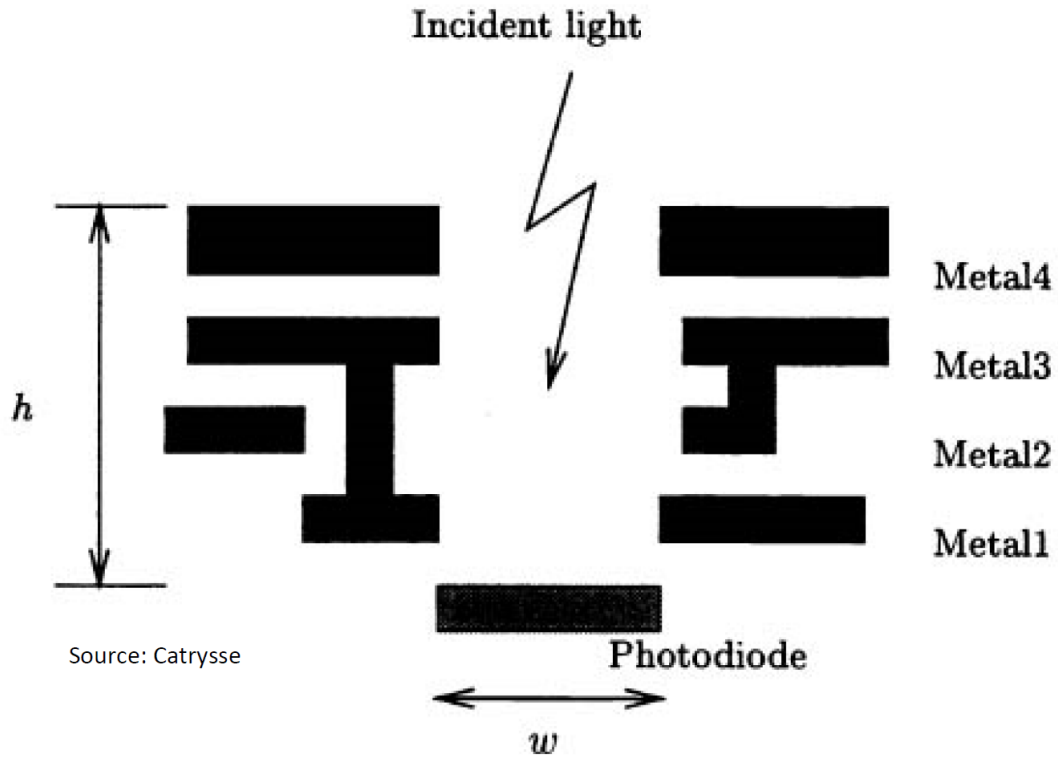
Stepper/Scanner 200 mm wafer

200mm & 300mm diameter wafers

Microlenses

Real world challenge: Getting light to the pixel

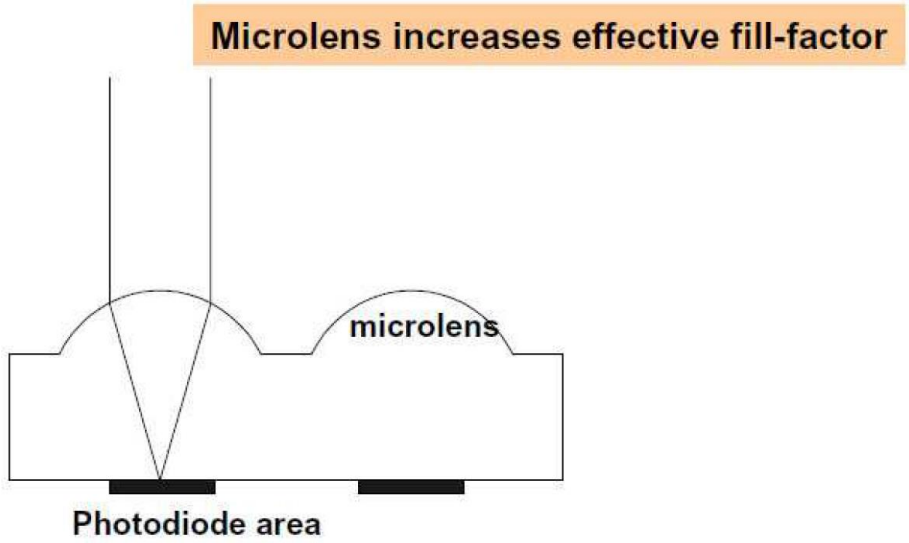




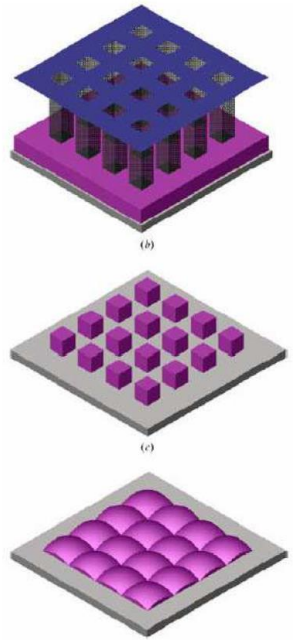
Source: Catrysse

Microlenses to the rescue?

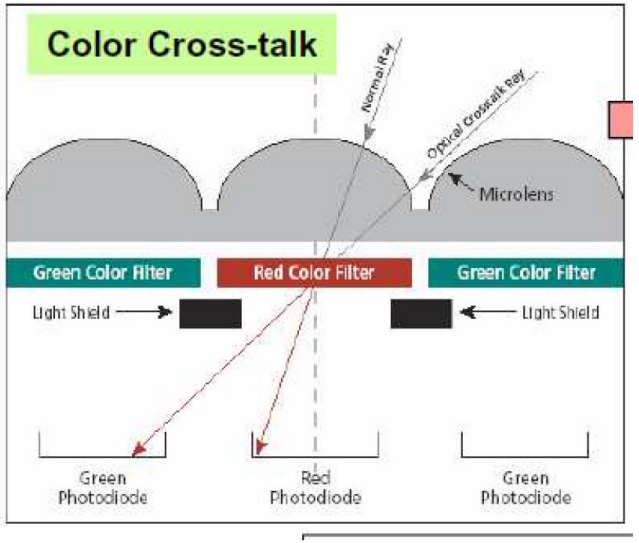
- Used to concentrate and redirect light onto photosensitive region of pixel



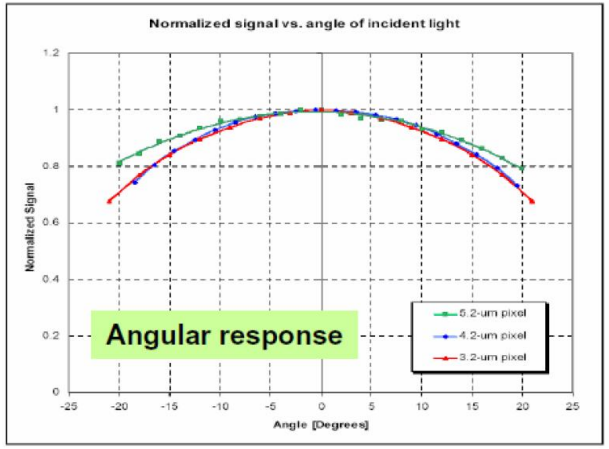
Source: Pain

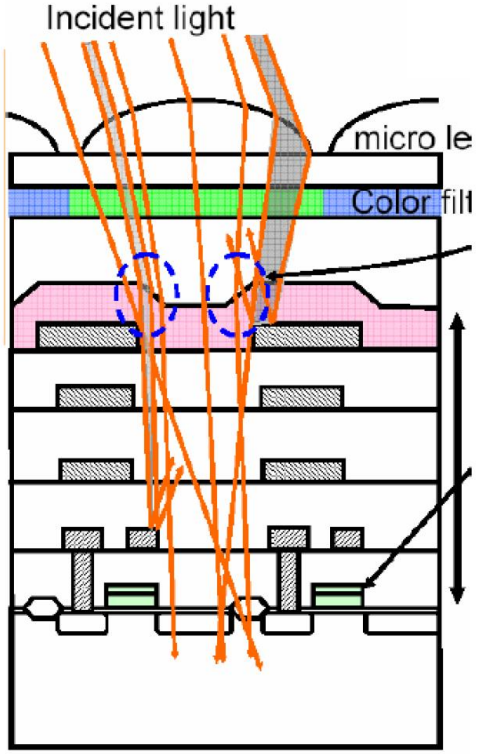


Microlens Application Problems



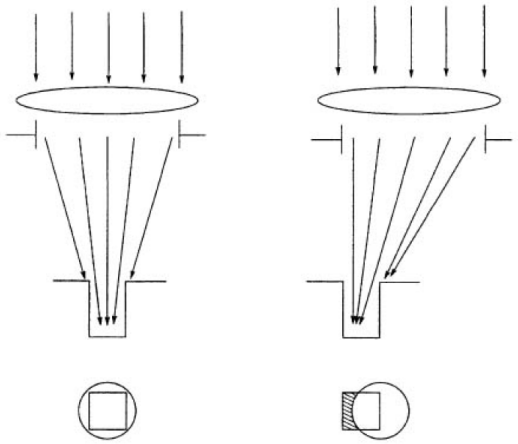
Source: Pain





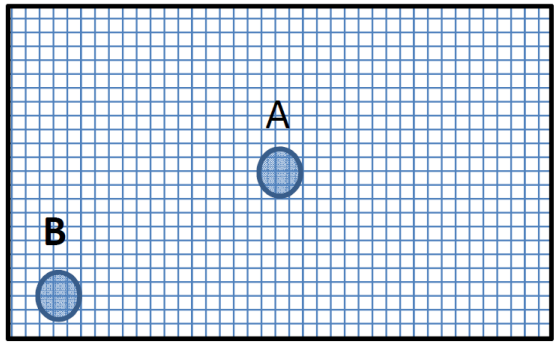
Obscuration, scattering

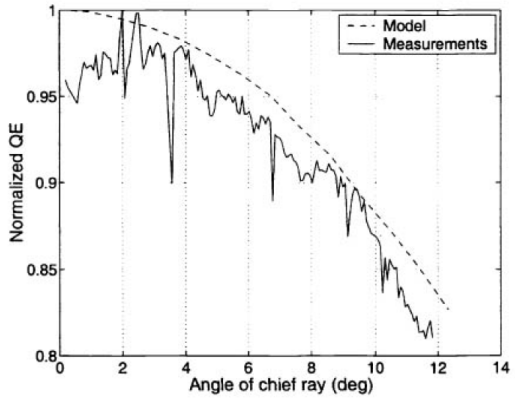
Pixel Vignetting:
QE reduction off axis by frontside wiring “optical tunnel”



Center of sensor (A)

Edge of sensor (B)



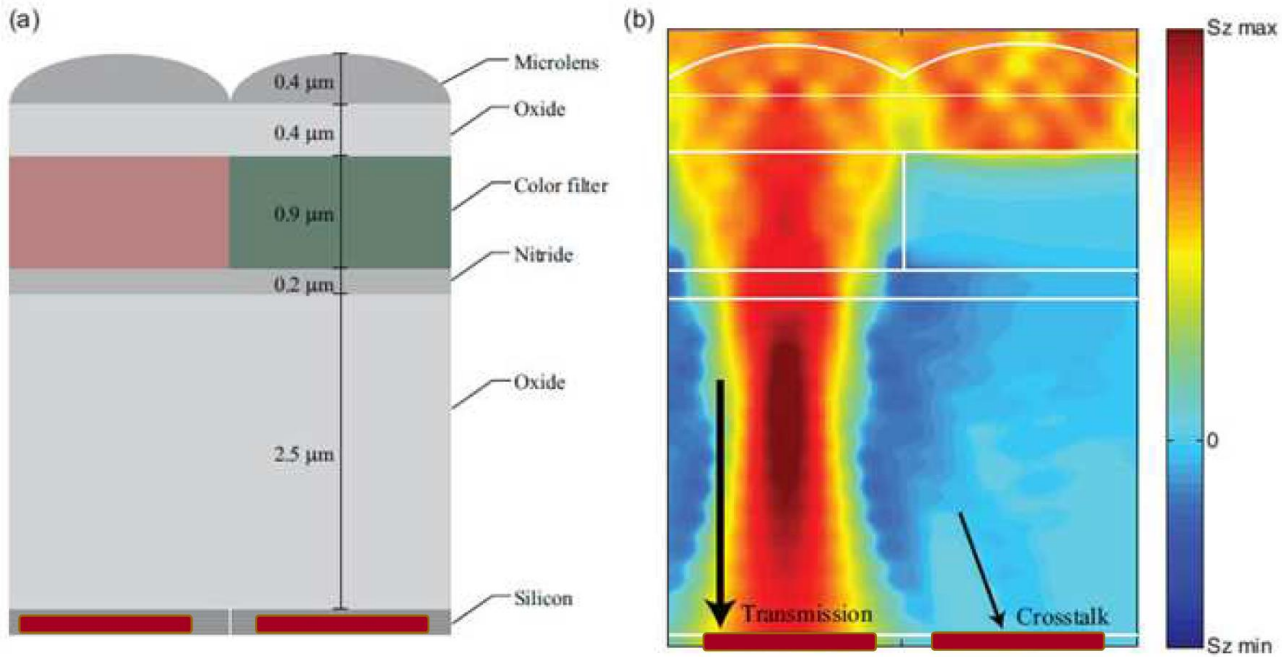


Source: Catrysse

QE reduction degrades SNR for off-axis portions of image

Microlens design: Energy flow analysis for small pixels

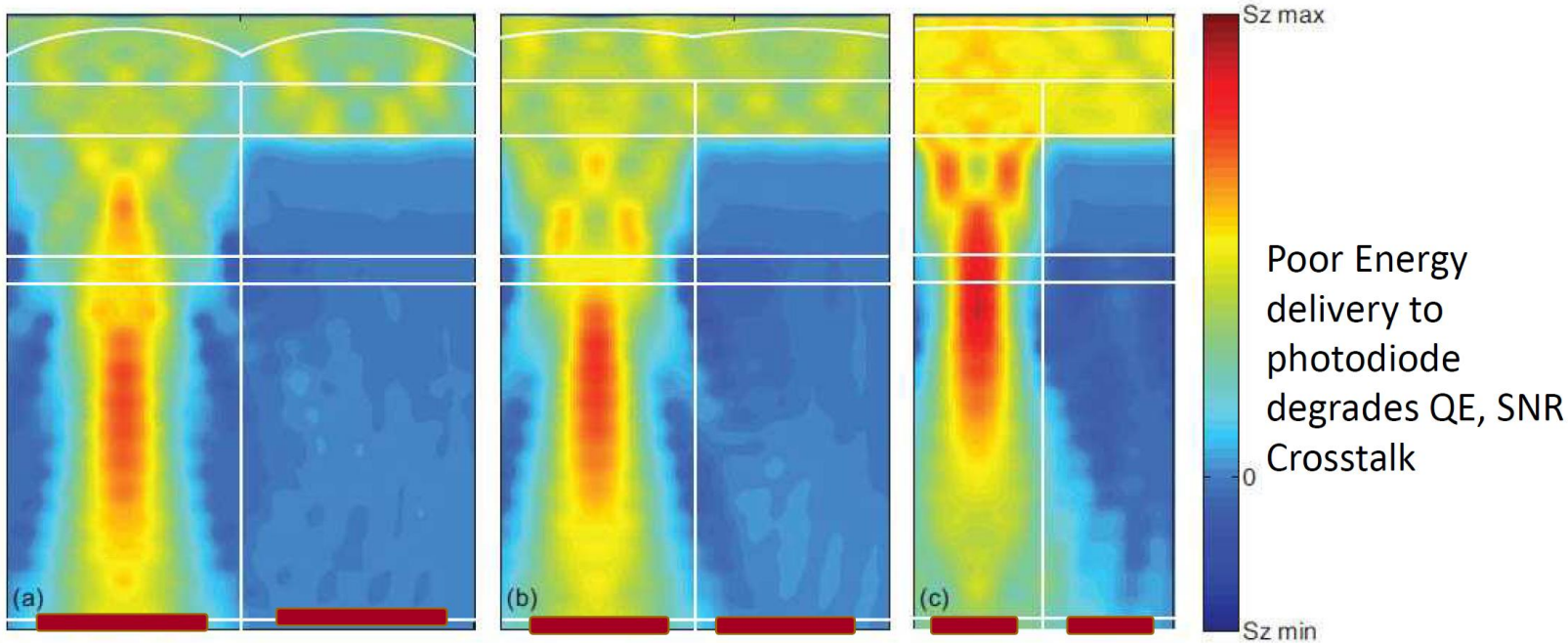
Used to concentrate and redirect light onto photosensitive region of pixel



Source: Huo

Smaller pixels: harder to get light to photodiode

Microlens challenges: sub 2 micron pixels

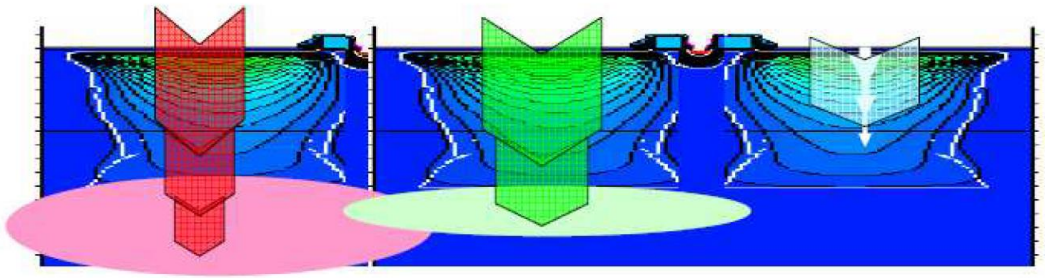


Source: Huo

Poor Energy delivery to photodiode degrades QE, SNR Crosstalk

1.75 micron 1.4 micron 0.97micron

FSI pixels working schematic



No xtalk from diffusion for the Blue
Low level of xtalk for the Green
Medium level of xtalk for the Red

Even if we have low level of signal ➔ The poor collection on the rear side of the photodiode ➔ color xtalk which is already a concern for FSI …

STMicroelectronics

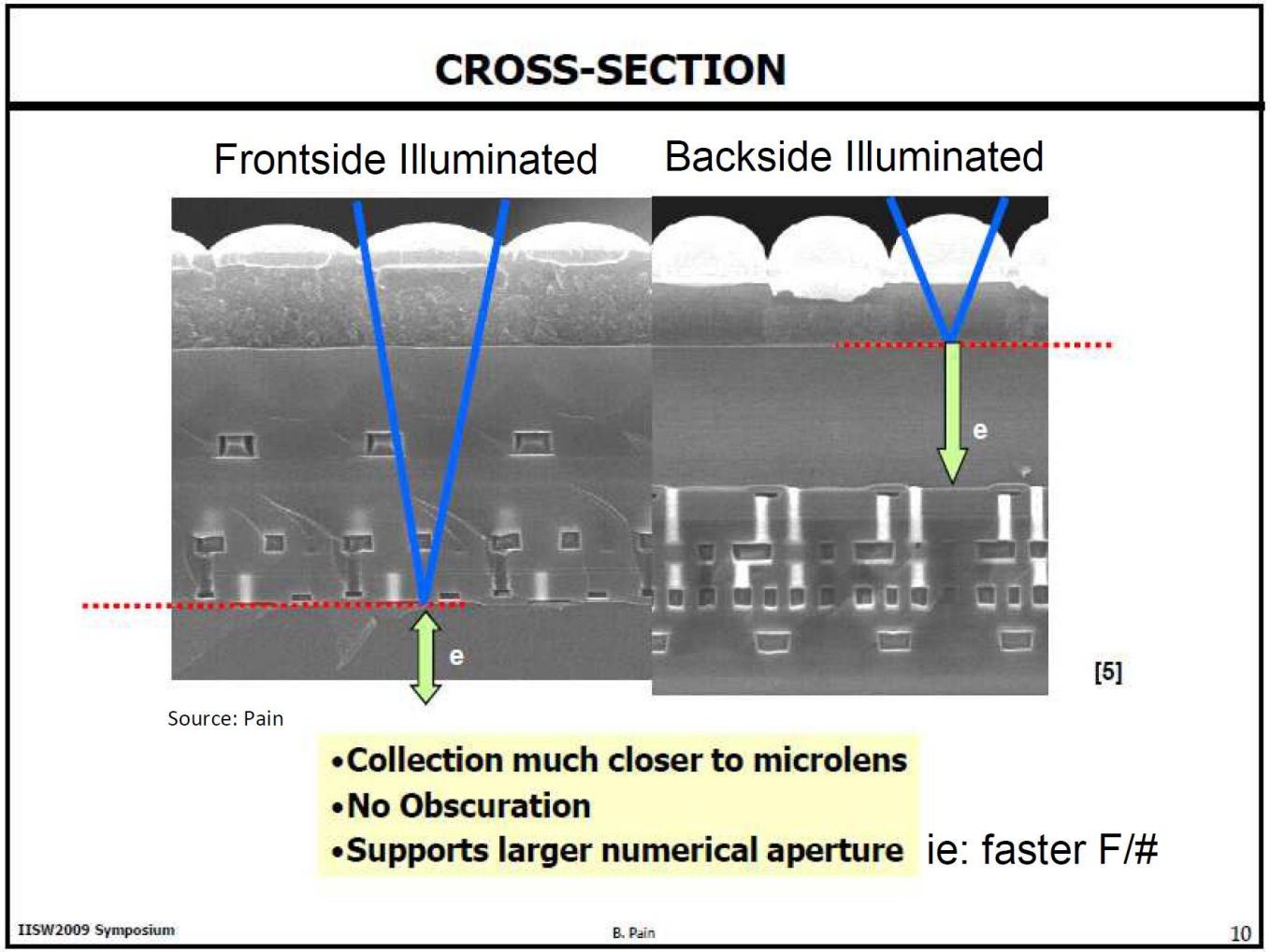
Source: Roy

For Frontside Illumination:

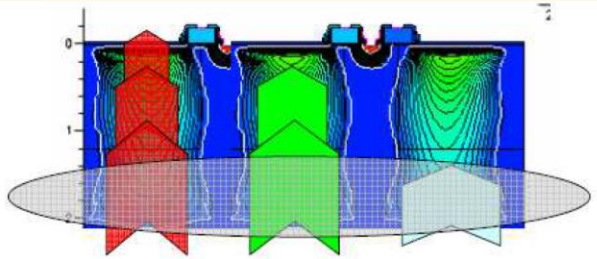
Red light penetrates deepest: has worst diffusion MTF/ Crosstalk

Backside Illumination

Fixing the Optical Tunnel with BSI



Back side illumination + Smaller pixel



High level of photon absorption for the three colors on the rear side of the diode

➔ collection efficiency must be managed as first priority

STMicroelectronics

Source: Roy

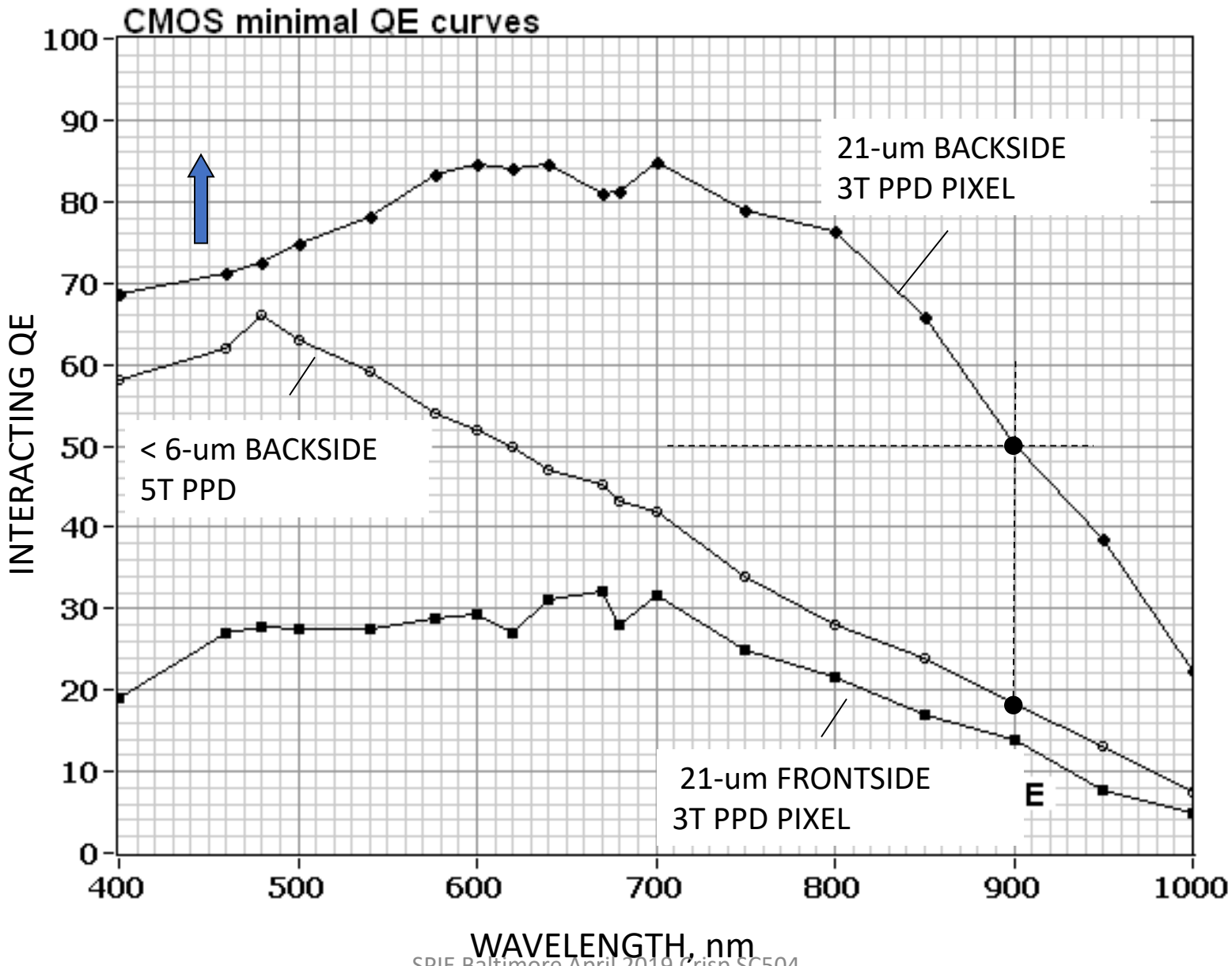
For Backside Illumination:

Blue light penetrates least: has worst diffusion MTF/ Crosstalk

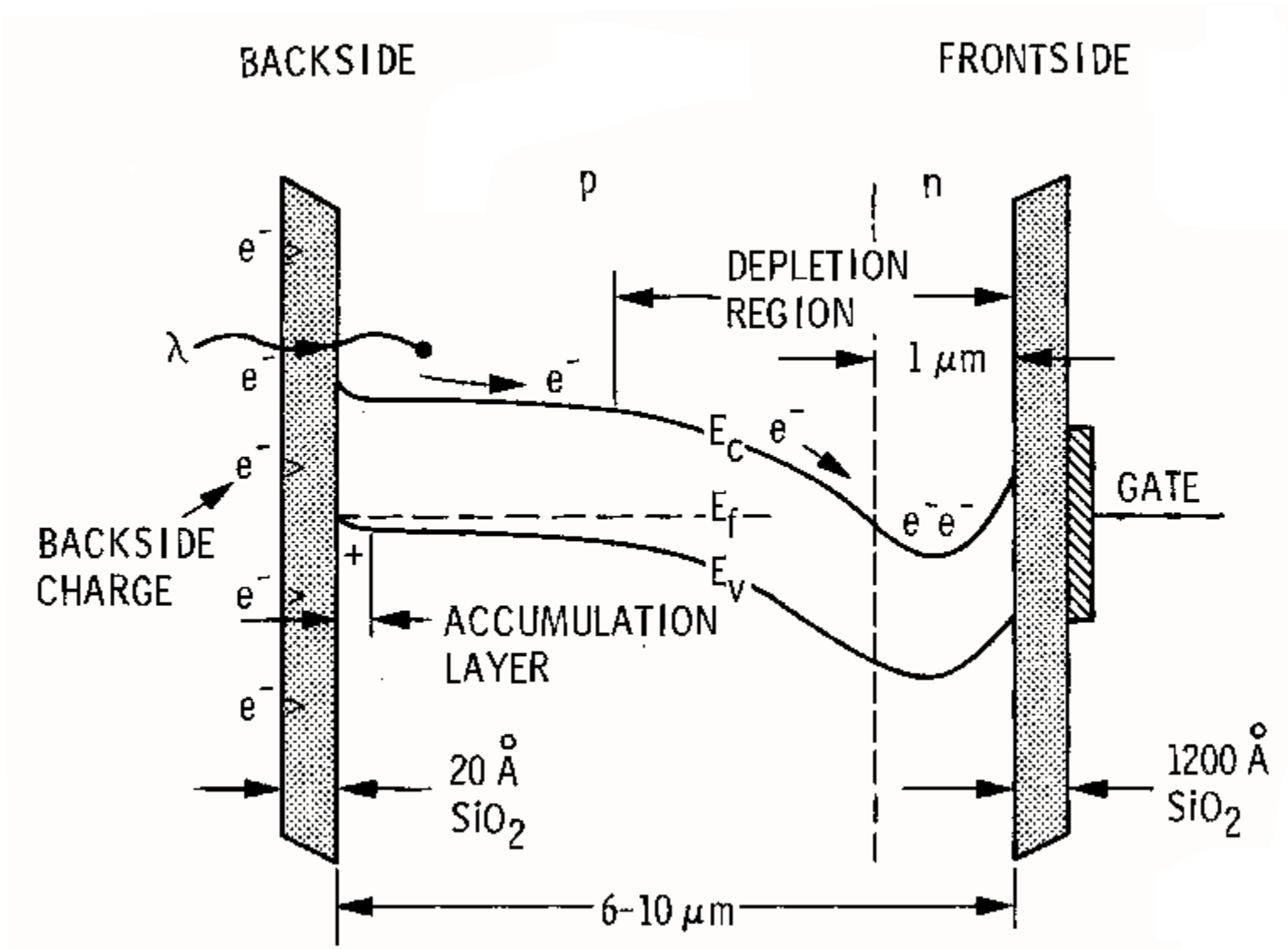
BSI Manufacturing Issues

- Thinning / handling the wafer
- Dark Current control
- Backside surface trapping prevention
- Packaging
- TSV stacking with other die?
- Microlens / Color Filter Array

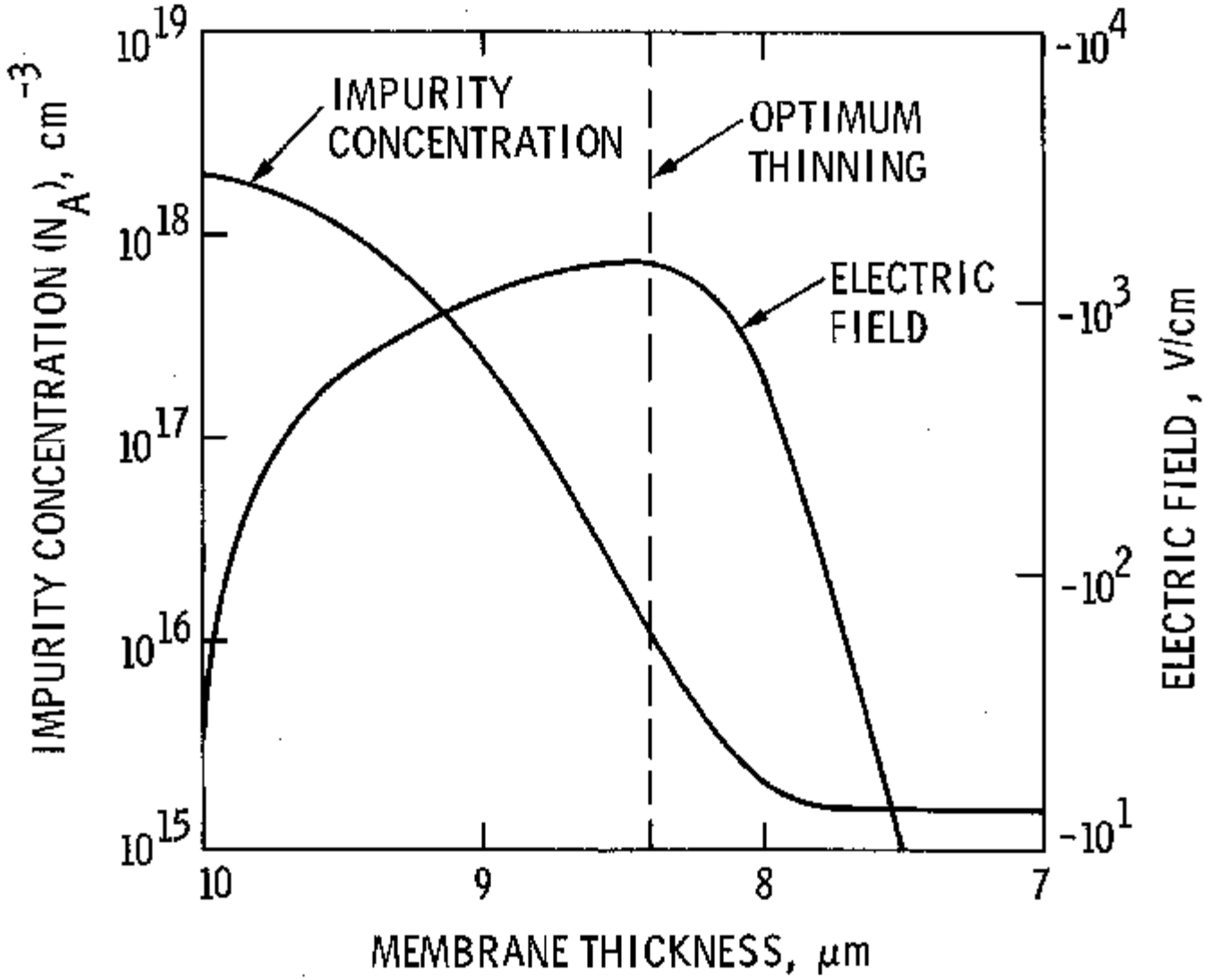
BACKSIDE ILLUMINATED CMOS



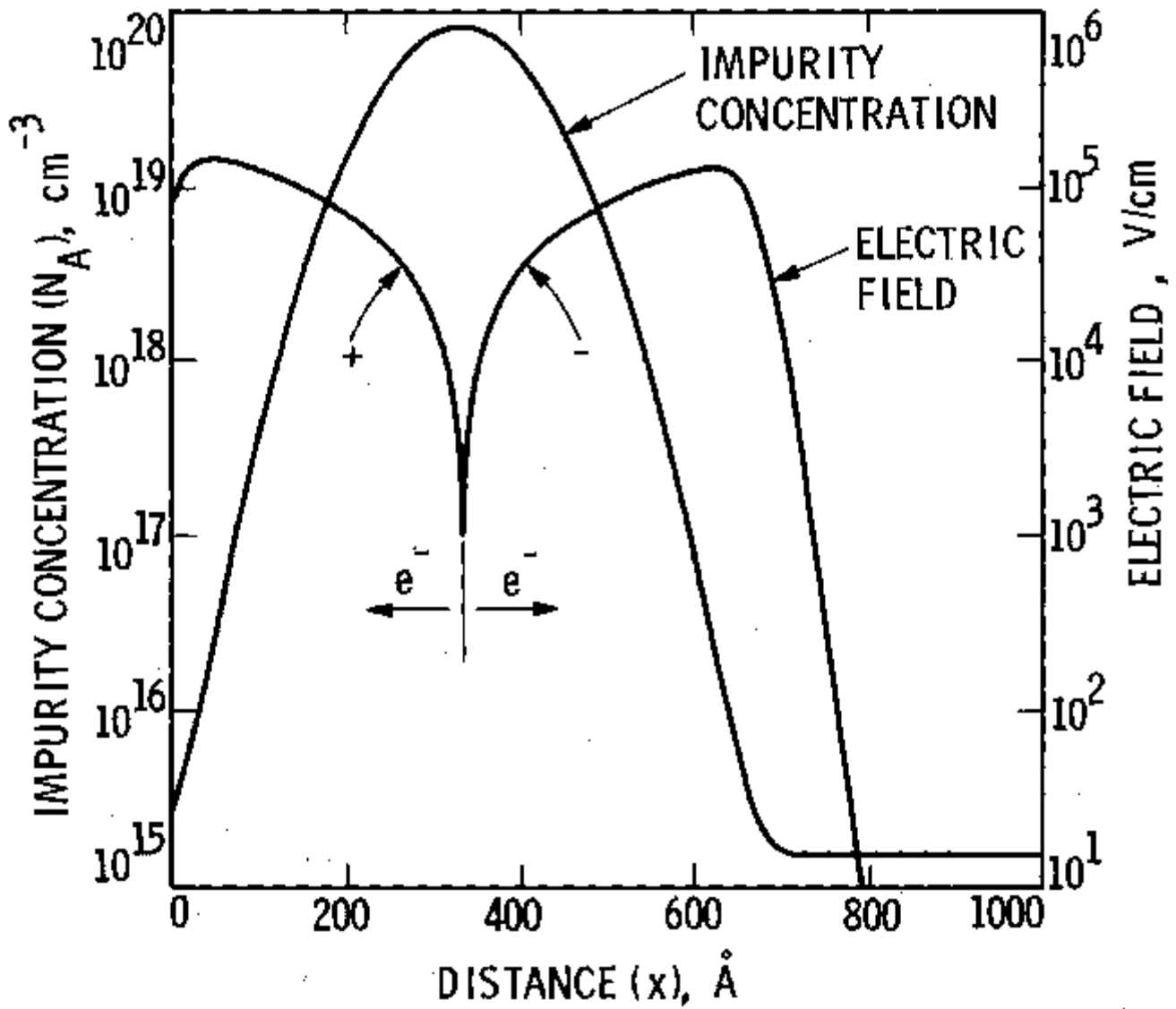
QE PINNING


BACKSIDE
FRONTSIDE
p
n
DEPLETION
REGION
1 μm
λ
e⁻
e⁻
e⁻
e⁻
e⁻
e⁻
e⁻
E_c
E_f
E_v
GATE
BACKSIDE
CHARGE
+
ACCUMULATION
LAYER
20 Å
SiO2
1200 Å
SiO2
6-10 μm

SELF ACCUMULATION



ION IMPLANTATION



BACKSIDE IMPLANTATION ISSUES

IMPLANT MUST BE HIGH DOSE AND VERY SHALLOW FOR HIGH BACKSIDE FIELD AND NEGLIGIBLE RECOMBINATION.

IMPLANT PROFILE MUST BE MAXIMUM AT THE IMMEDIATE SURFACE. ADDITIONAL THINNING MAY BE REQUIRED TO REMOVE LEADING EDGE OF THE IMPLANT PROFILE.

IMPLANT MUST BE ACTIVATED TO ELIMINATE BULK STATE TRAPS WHICH LEAD TO LOW QE AND HIGH DARK CURRENT. e.g., LASER ANNEALING, RAPID THERMAL ANNEAL, GLOBAL ANNEALING USING REFRACTORY METALS.

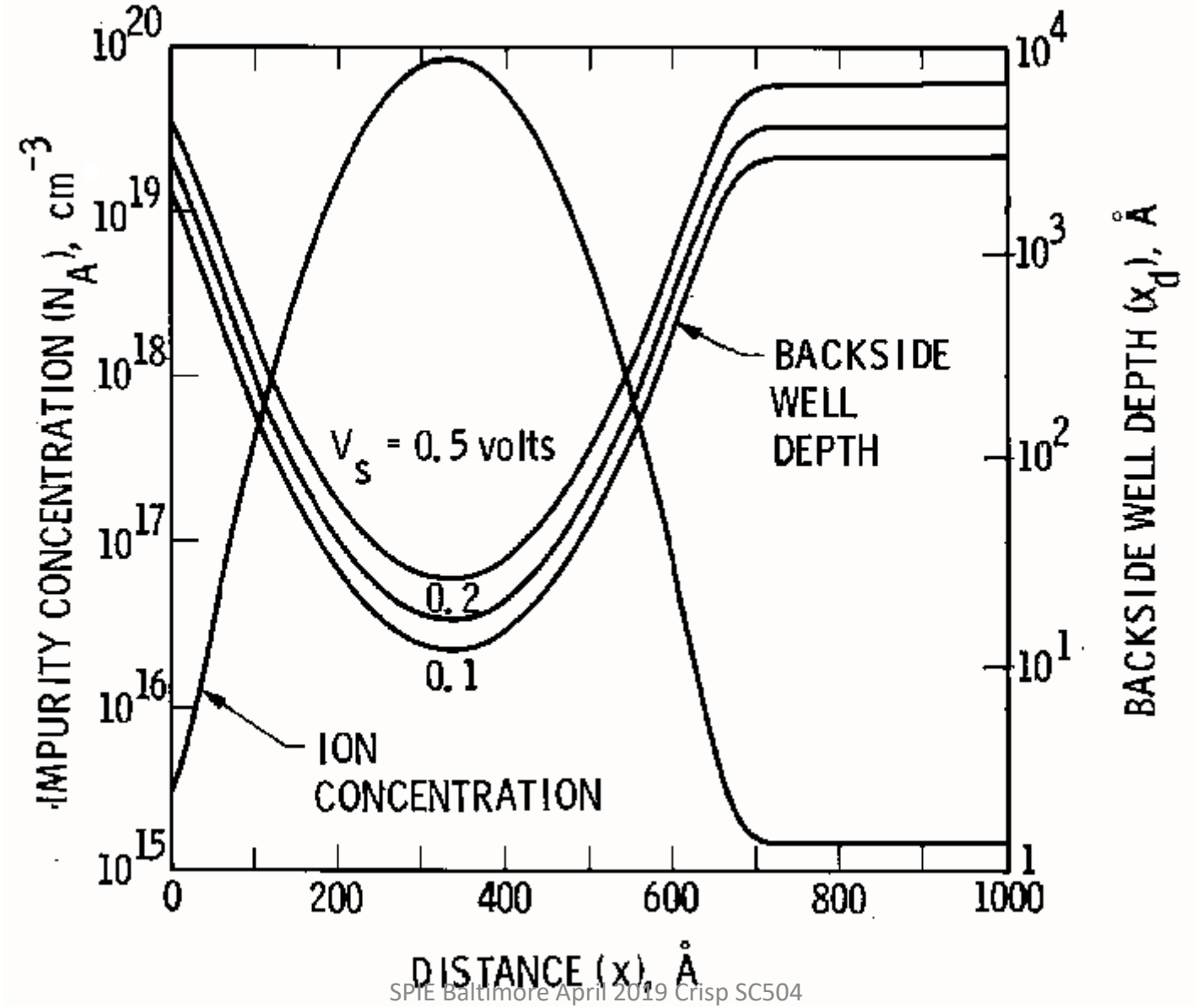
IMPLANT ANNEALING IS A TRIAL AND ERROR INTENSIVE AND TYPICALLY NOT A REPRODUCABLE PROCESS.

VERY LOW ENERGY IMPLANT IS REQUIRED TO DUPLICATE PASSIVE ACCUMULATION APPROACHES. NATIVE OXIDE THICKNESS MUST BE KNOW ACCURATELY. ACTIVATION DIFFUSES IMPLANT.

TYPICALLY DOES NOT REACH THE QE PINNED CONDITION AND EXHIBITS BACKSIDE DARK CURRENT.

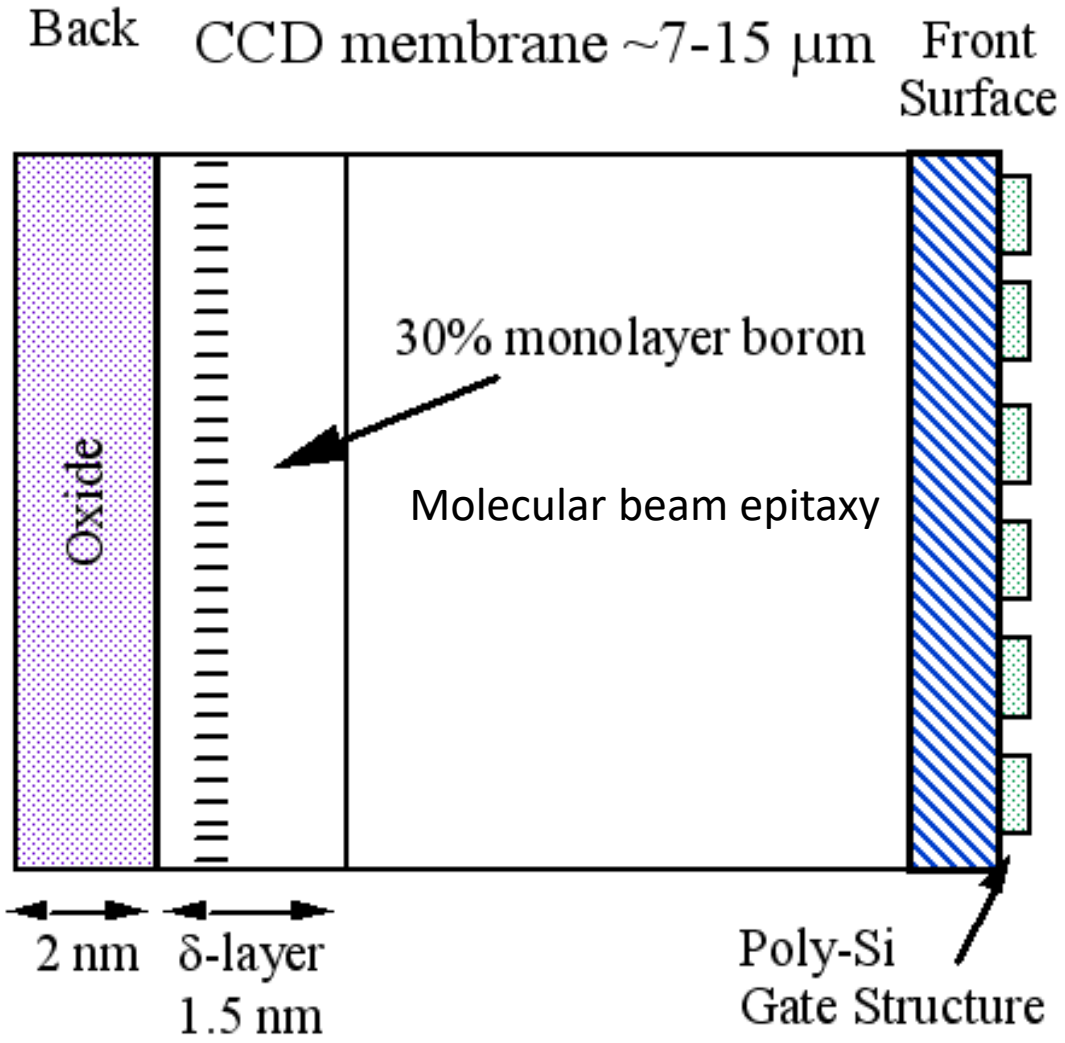
MANY GROUPS HAVE TRADED ION IMPLANTATION TO PASSIVE ACCUMULATION TECHNIQUES.

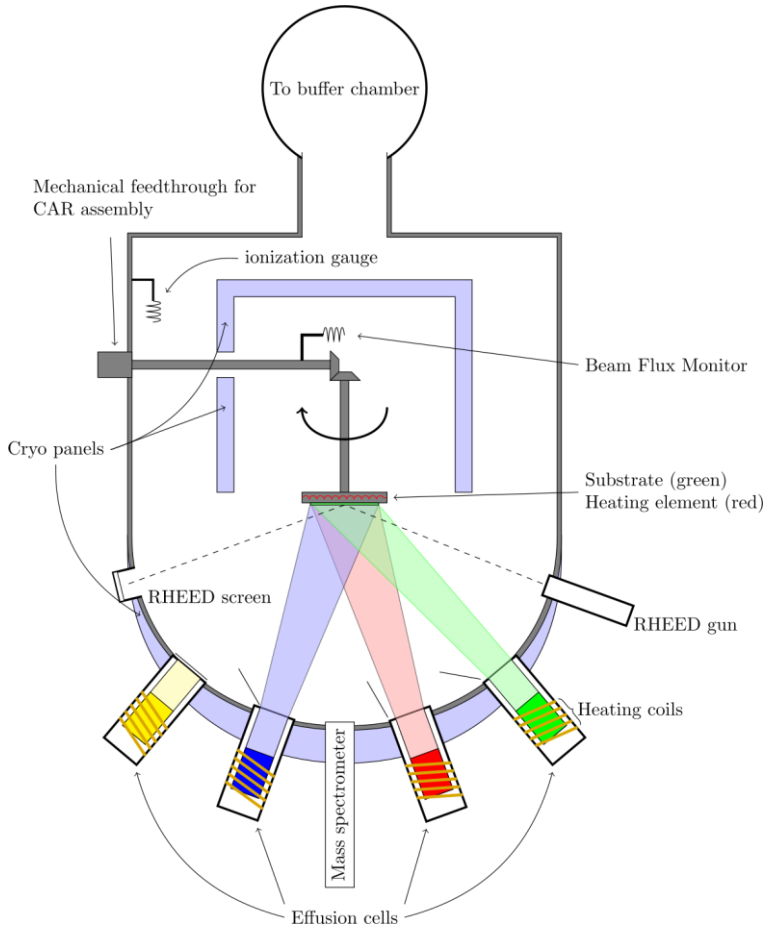
ION IMPLANTATION



DELTA DOPING

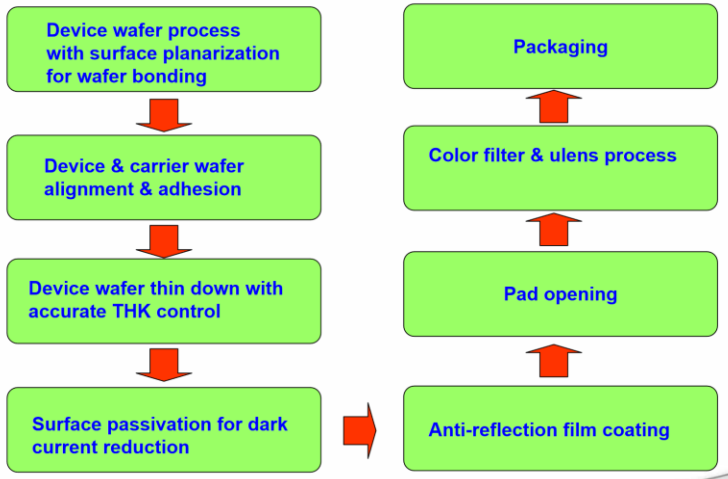
CONSIDERED TO BE THE BEST ACCUMULATION APPROACH AVAILABLE

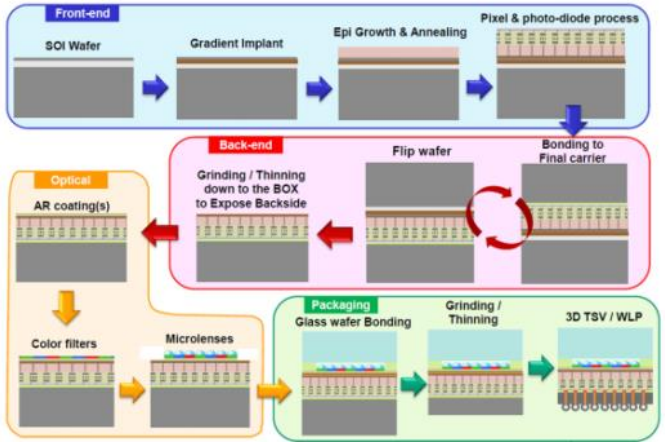




MBE Reactor

Schematic of Si Process Flow

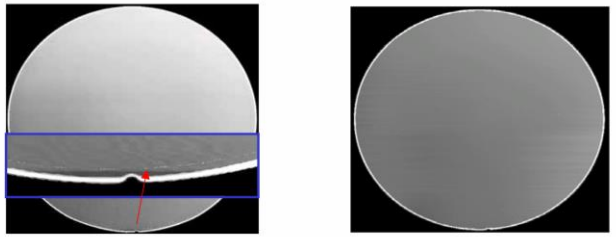




Alternate: S.O.I. method
(Silicon On Insulator)

BSI Bonding Progress

- Bubble free achieved
- Bubble monitor methodology established
- Good planarization before bond
- Particle reduction @ bonding interface
- Wafer bonder optimization

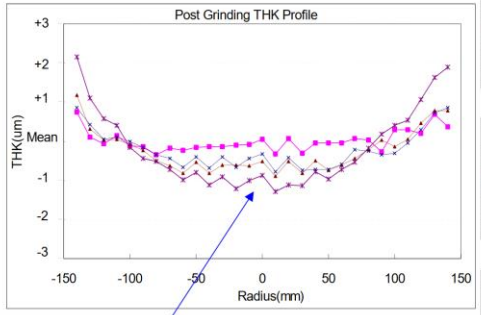


Bubble Bubble-free

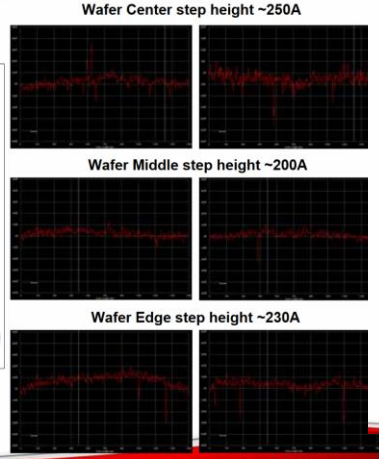
https://www.imagesensors.org/Past%20Workshops/2009%20Workshop/2009%20Papers/BSI%2005_Wuu.pdf

Grinding Performance

- TTW (Total Thickness Variation) within Wafer: 2~3 um
- No visible stripe pattern viewed by OM as demonstrated from small step height < 0.025um within 1.5mm scan range from Alpha-stepper

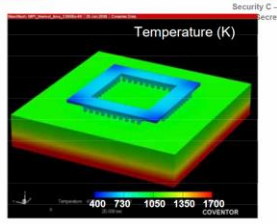


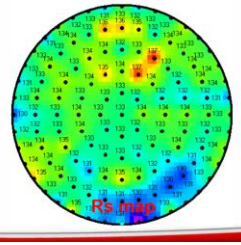
Grinder artificial profile compensation for wet etch thin down process

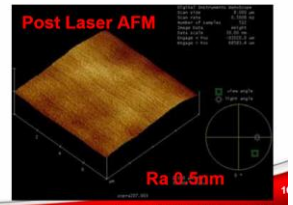


BSI Laser Anneal

- Short wavelength & duration time
- Si melting needed to achieve low Rs (i.e. good activation)
- Good WIW Rs uniformity: ≤ 1.5%
- No thermal damage to device & metal if Si melting
- Good surface roughness

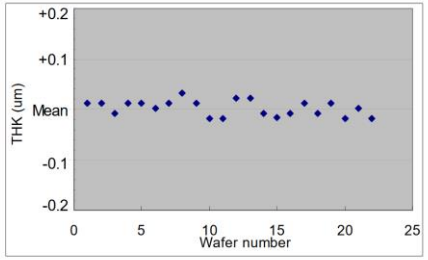


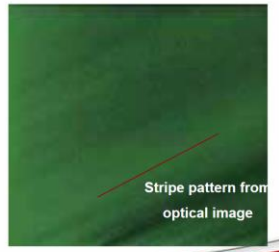




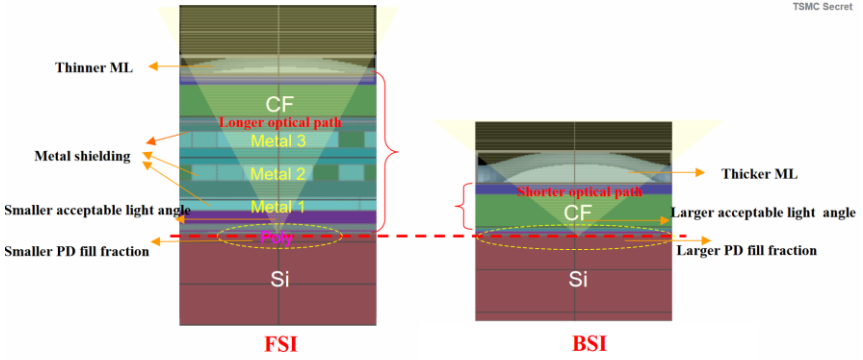
BSI Thin Down Process

- Non-SOI approach (TSMC IP chemicals for etch stop on Epi layer)
- Mechanical & Wet chemical thin down
- WTW THK uniformity controlled @ ≤ +/- 0.025um by establishing feed-forward system
- Good surface roughness with stripe pattern free





BSI vs FSI Optical Performance



Optical Performance Comparison						
	Optical path	ML thickness	Metal shielding	Acceptable light angle	PD fill fraction	Energy on PD
FSI	long	thinner	yes	small (F# 2.8)	small (~30%)	27%
BSI	short	thicker	no	large (F# 2)	lager (~50%)	56%

Empowering Innovation

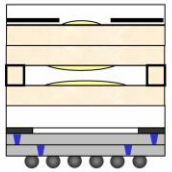
Advanced Camera Module Technology Integration Trend

BSI + TSV-CSP technology integration realize

- **True chip size CSP solution**

Compact camera module through integration with wafer level lens

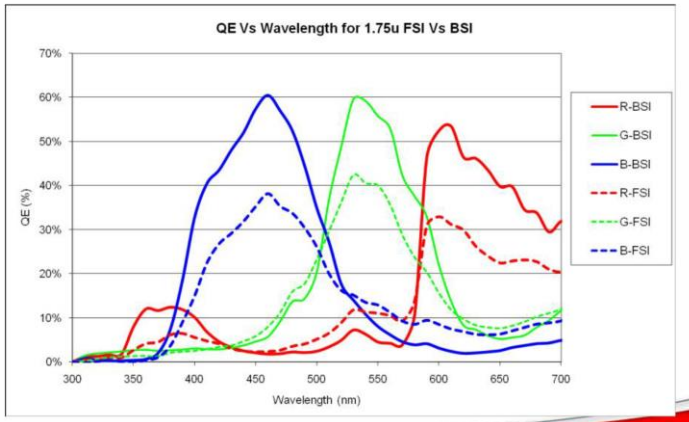
Smart camera module by 3D CCM + DSP stacking



Empowering Innovation

1.75um FSI vs BSI Performance

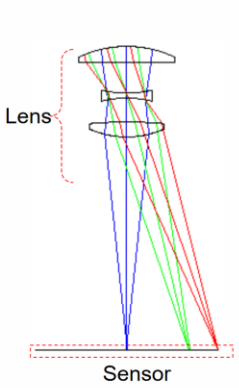
- **Quantum Efficiency: 40-60% improvement for BSI vs. FSI**
- **Crosstalk: 30-80% improvement for BSI vs. FSI**

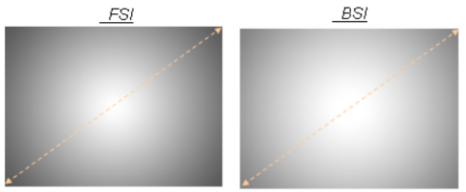


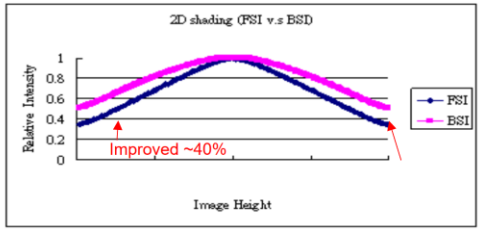
Empowering Innovation

Shading Effect Improvement in BSI

- Compared to FSI, the shading effect in BSI can be improved 40% by integrating sensor and lens in 1.4um pixel



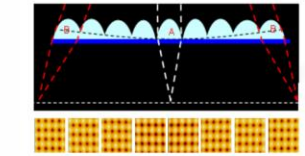


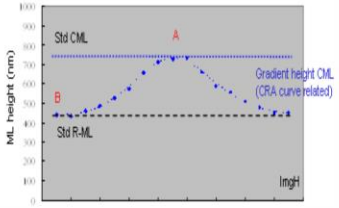


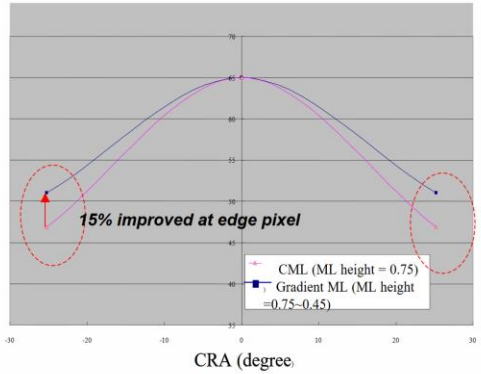
Empowering Innovation

Future Trend-Gradient CML

- Different ML height and shifting arrangement based on CRA
  - **Combined ML shifting and gradient height ML for shading optimization**



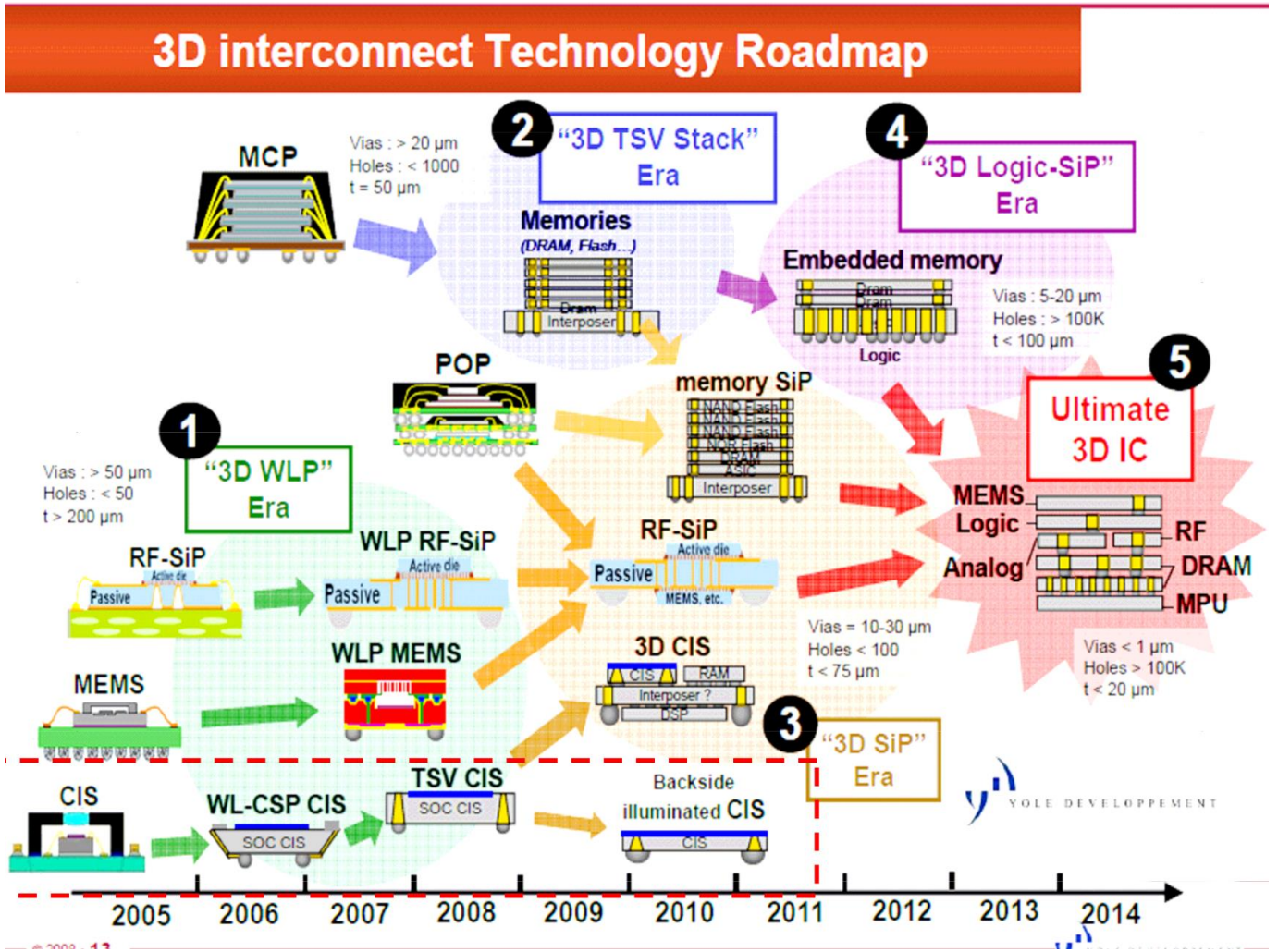




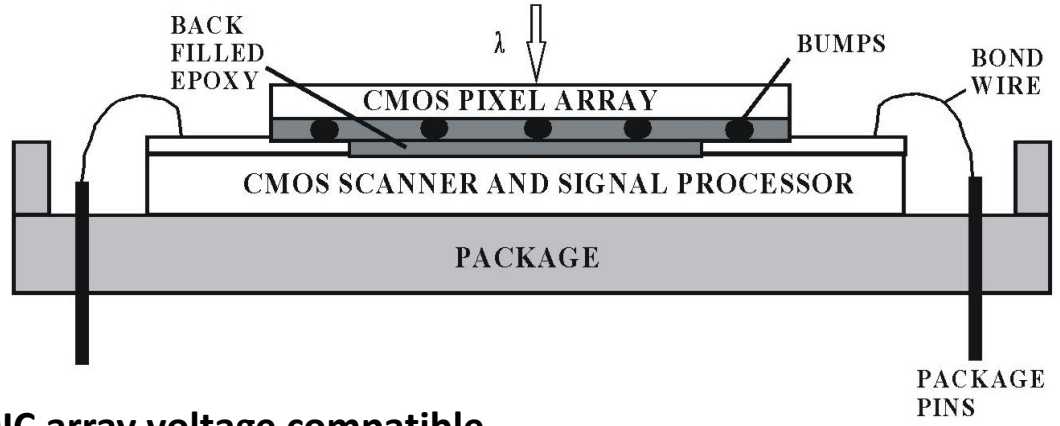
Sensitivity of edge pixel with large CRA
(Shading Profile Simulation)

Empowering Innovation

Multi Die Stacking


3D interconnect Technology Roadmap
MCP
Vias : > 20 µm
Holes : < 1000
t = 50 µm
2
"3D TSV Stack" Era
Memories
(DRAM, Flash...)
Interposer
4
"3D Logic-SiP" Era
Embedded memory
Logic
Vias : 5-20 µm
Holes : > 100K
t < 100 µm
POP
memory SiP
Interposer
5
Ultimate 3D IC
MEMS
Logic
RF
Analog
DRAM
MPU
Vias < 1 µm
Holes > 100K
t < 20 µm
1
"3D WLP" Era
Vias : > 50 µm
Holes : < 50
t > 200 µm
RF-SiP
Passive
WLP RF-SiP
Active die
Passive
RF-SiP
Active die
Passive
MEMS, etc.
WLP MEMS
MEMS
3D CIS
CIS
RAM
Interposer ?
DSP
Vias = 10-30 µm
Holes < 100
t < 75 µm
3
"3D SiP" Era
CIS
WL-CSP CIS
SOC CIS
TSV CIS
SOC CIS
Backside illuminated CIS
CIS
YOLE DEVELOPPEMENT
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014

HYBRID ARRAYS: CMOS TO CMOS



↑ CMOS pixel array CMOS ROIC array voltage compatible.

↑ CMOS pixel array is fabricated independently from ROIC array (allowing pixel optimization and isolation).

↑ Sparse bumping can take place within the array for vertical integration.

↑ Tolerant to high-energy radiation sources.

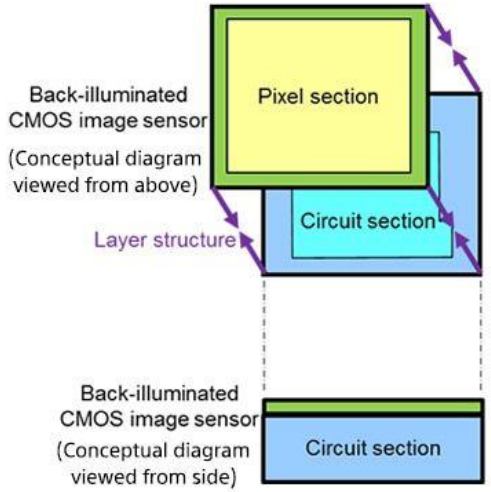
↑ Very high resolution – ultra high speed operation.

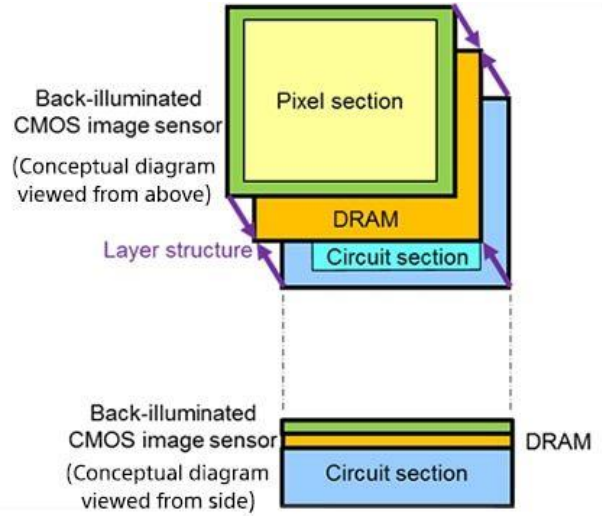
↑ Read noise independent of array size or frame rate.

↑ Low power / compact sensor designs.

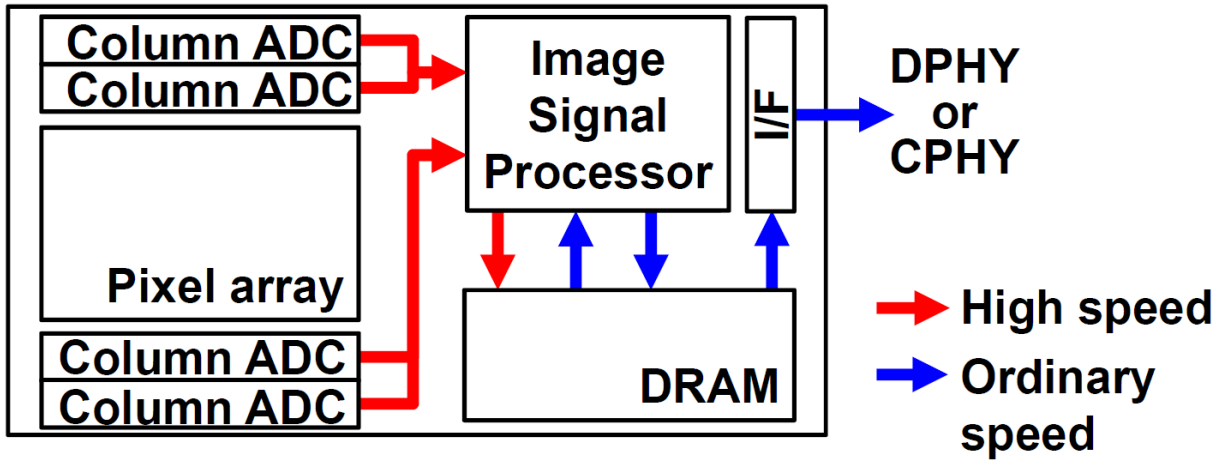
↓ High cost for custom pixel CMOS processing.

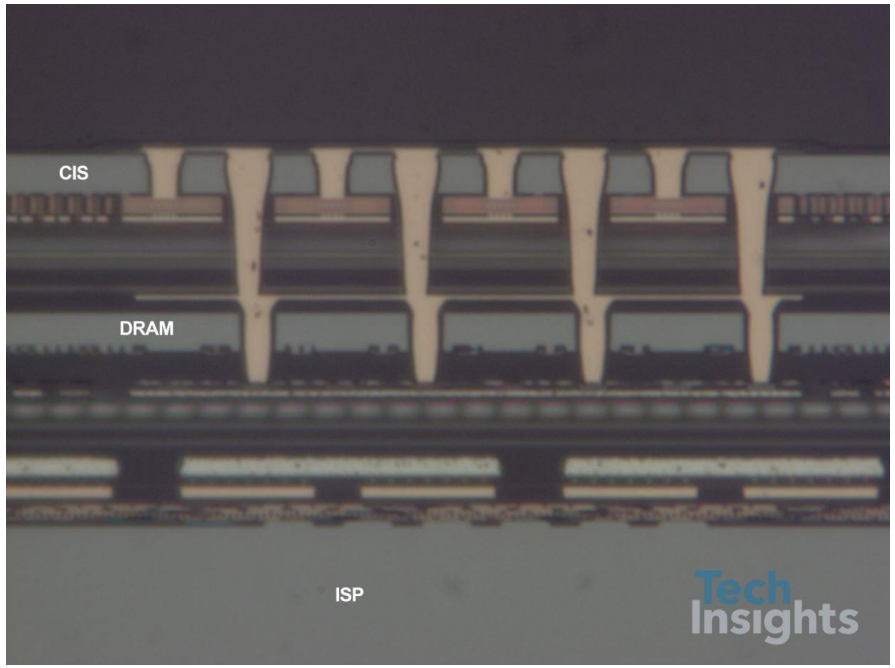
TSV (Sony, Huruta et al, ISSCC 2017)





Architecture





Benefit: very rapid readout using many parallel channels transferring directly to DRAM

1/30 sec readout (progressive scan)

1/120 sec readout (progressive scan)

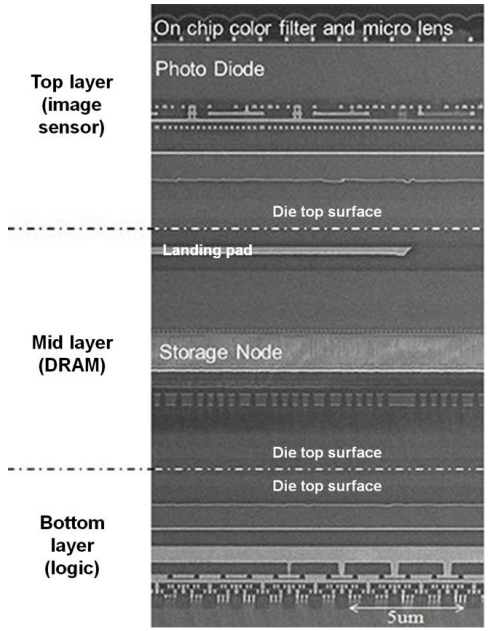
4x faster

But only for short bursts: not sustainable

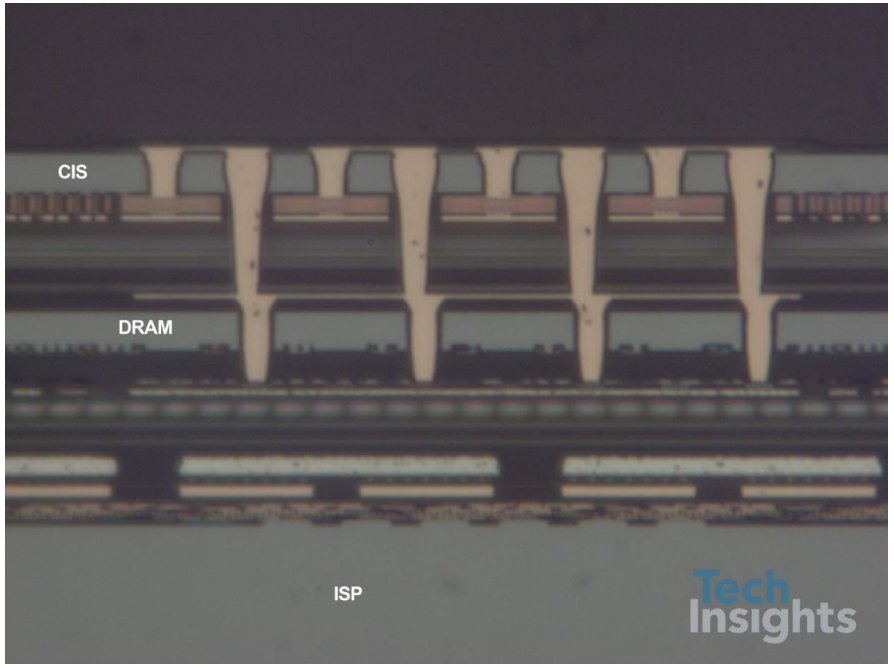
Super Slow Motion (960 F/s)

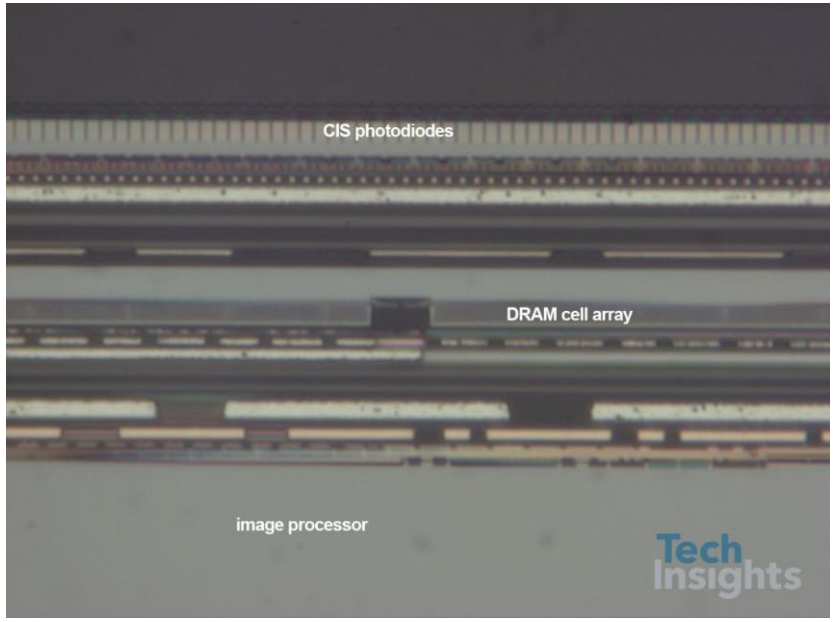
Maximum # frames in burst limited by DRAM capacity

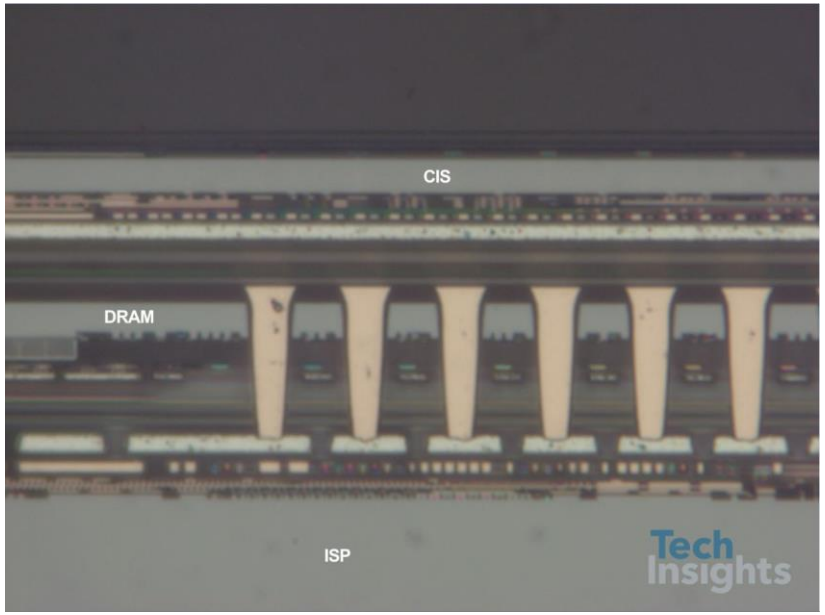
Cross Sections

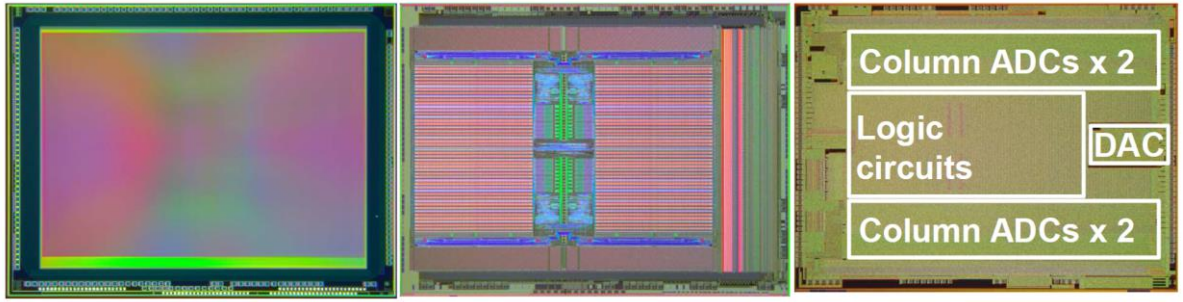


Source: Sony









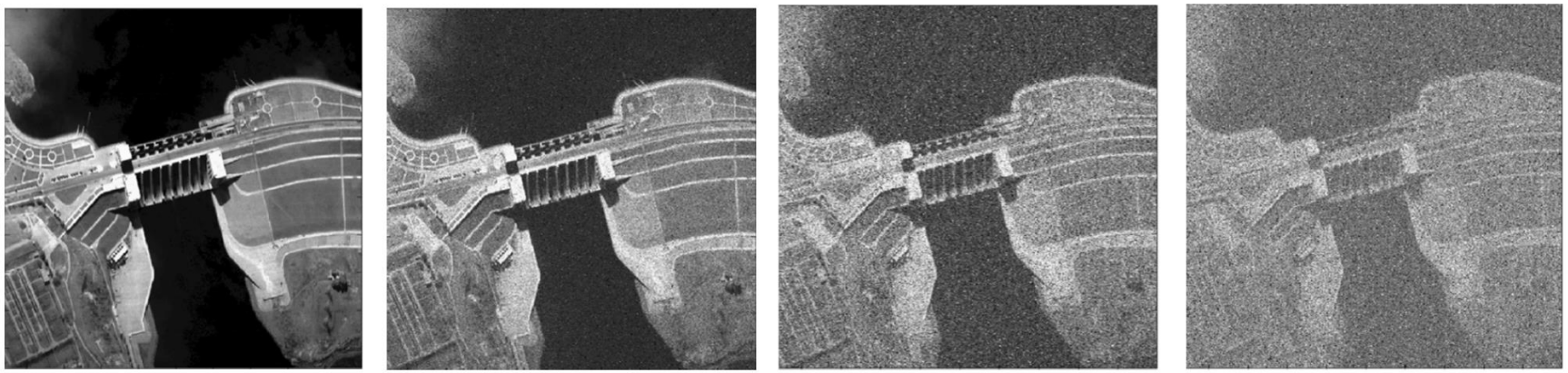
Pixel array | DRAM + row drivers | Image processor

Source: Sony/ISSCC

Part 10:
CMOS Pixel Scaling

Key Question

- Q: How small can pixels be and what limits them?
- A: How good of an image do you want?



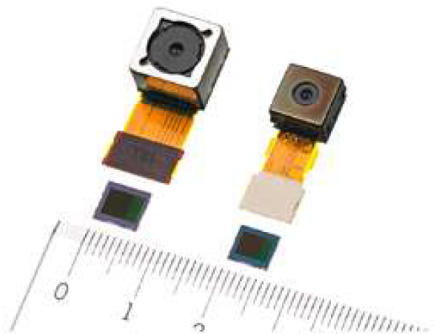
Source: Janesick

S/N = 28 S/N = 5.3 S/N = 3.6 S/N = 0.83

Photon Shot Noise impact on S/N

Key issues for cellphone application

- *Number one problem* is getting enough photons to the image sensor considering:
  - Overall module size
    - Limits image sensor photosensitive area
  - Exposure parameters
    - Max integration time, minimum lux
  - Imaging Optics
    - F#, magnification

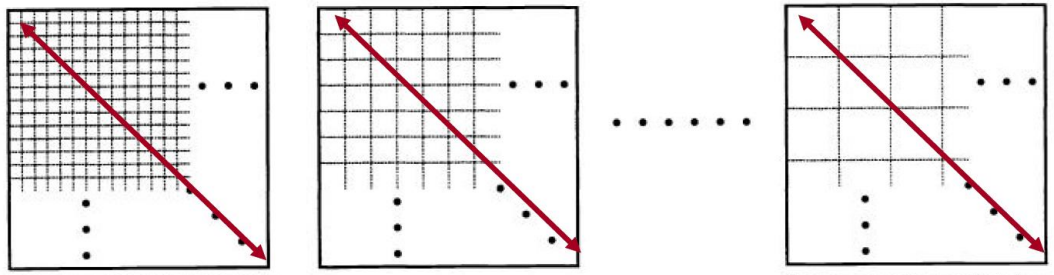


Source: Sony

- You must trade-off:
  - Signal to Noise ("SNR") vs Resolution
    - Resolution ↑, Pixel size ↓ = Less signal (photons) per pixel

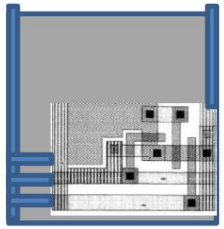
→ **Lower SNR**

Fixed sensor die size:
Pixels must shrink for higher resolution cameras

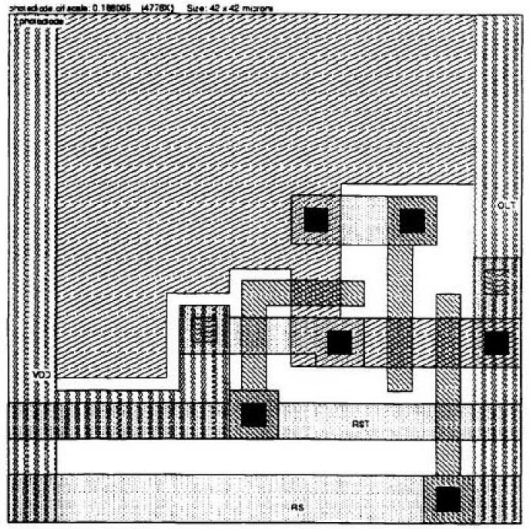


Source: Chen

3T Pixel Layout



Fixed die sizes
Sensor diagonals of:
1/2.3”
1/3.2”
1/4”
1/10”
etc

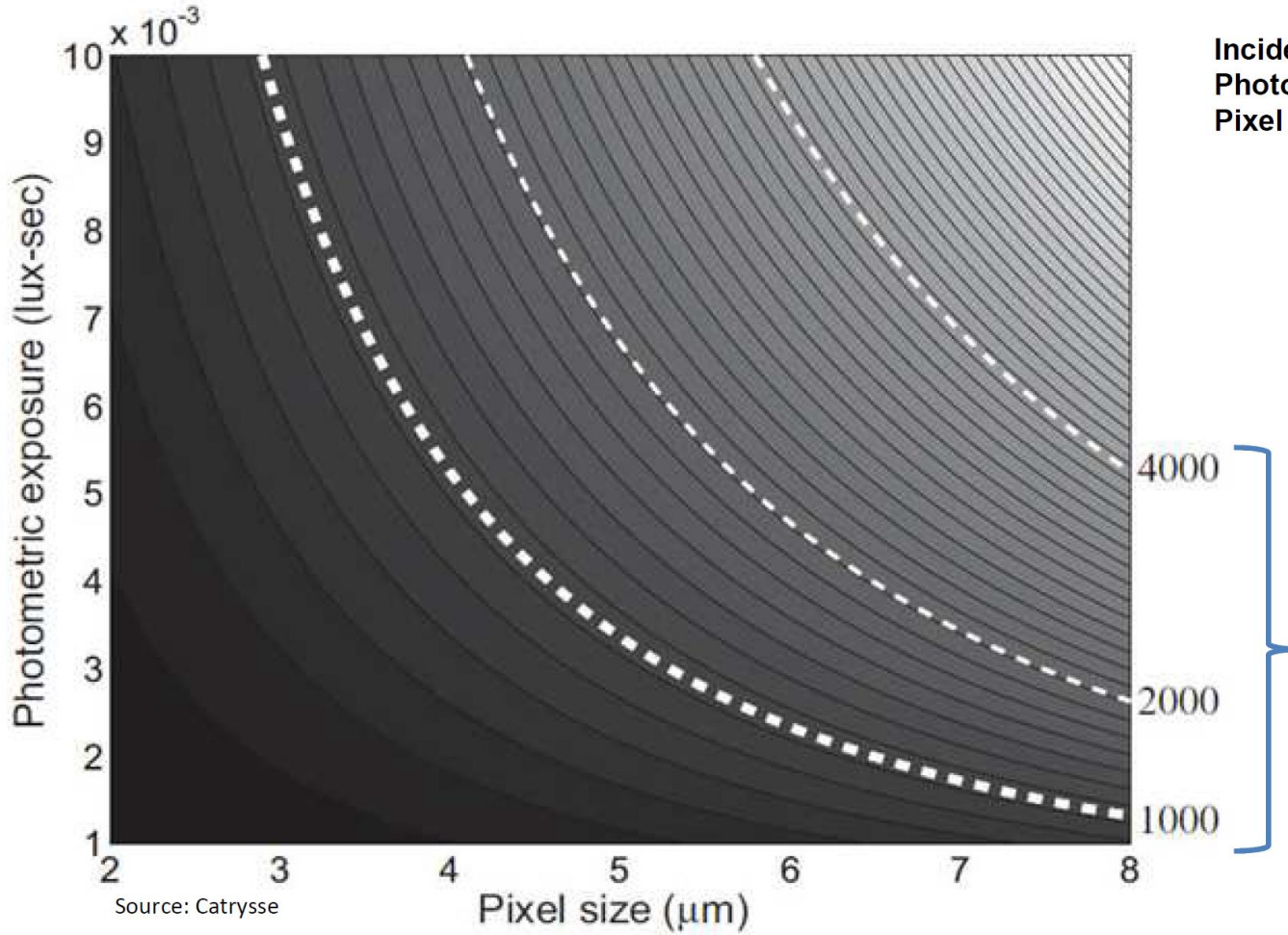


Highest resolution
Poorest low light response
Highest LP/mm req’t

Lowest resolution
Best low light response
Lowest LP/mm req’t

Delivering Light to the Sensor

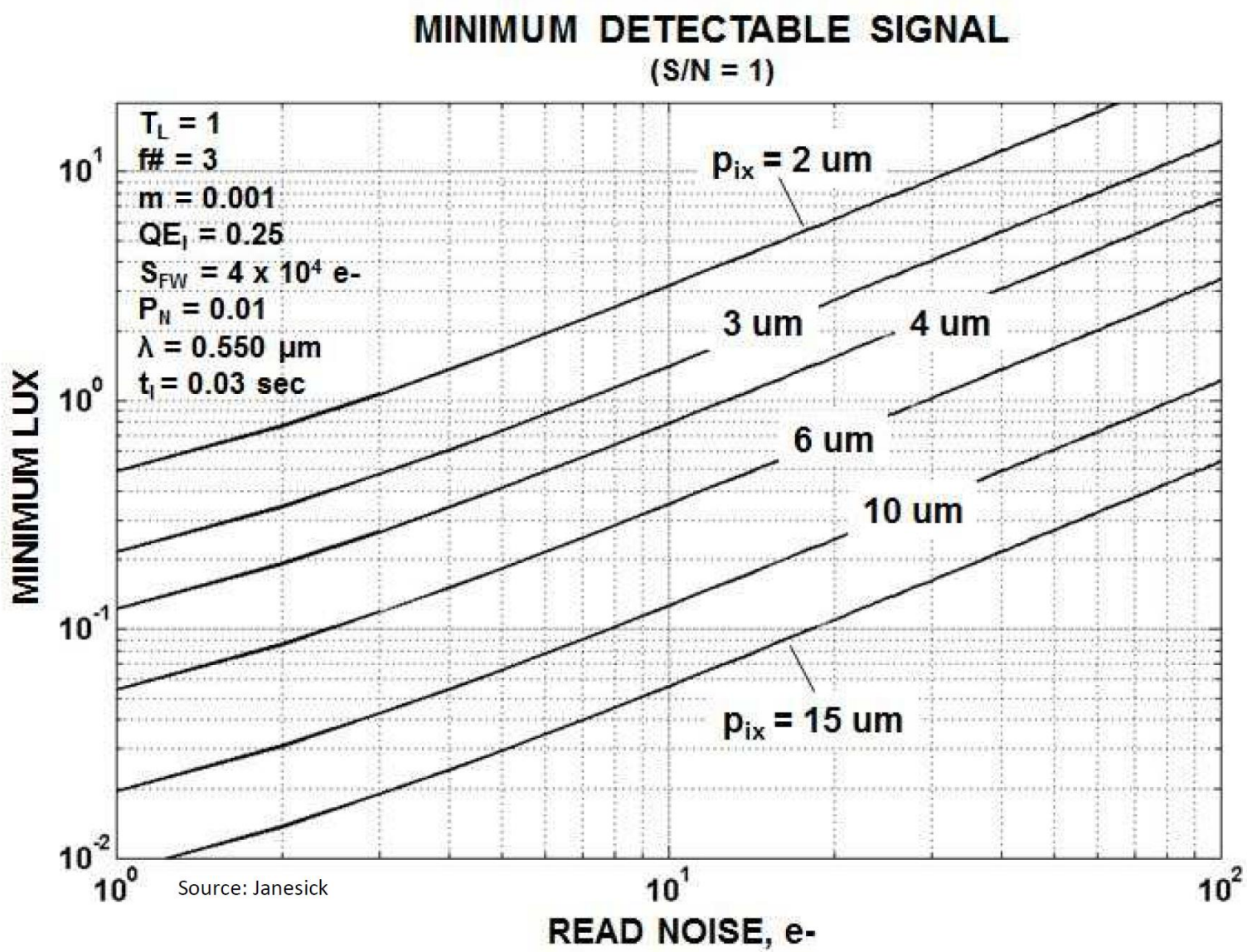
Pixel Geometry:
How many photons is your pixel receiving?



Source: Catrysse

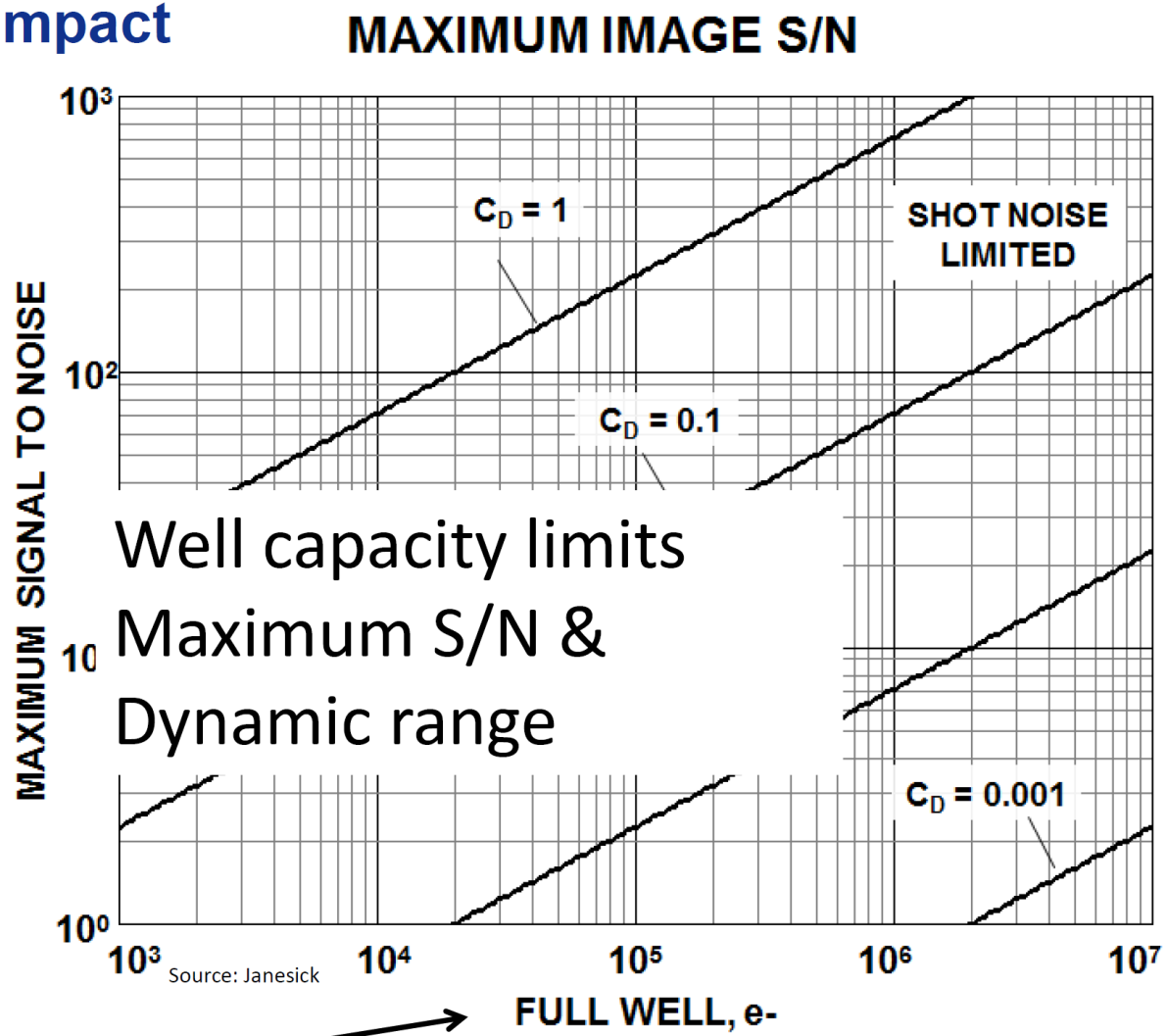
Incident Photons/ Pixel	Maximum Theoretical SNR
4000	63.25
2000	44.72
1000	31.62

Pixel Size, System Noise Impact



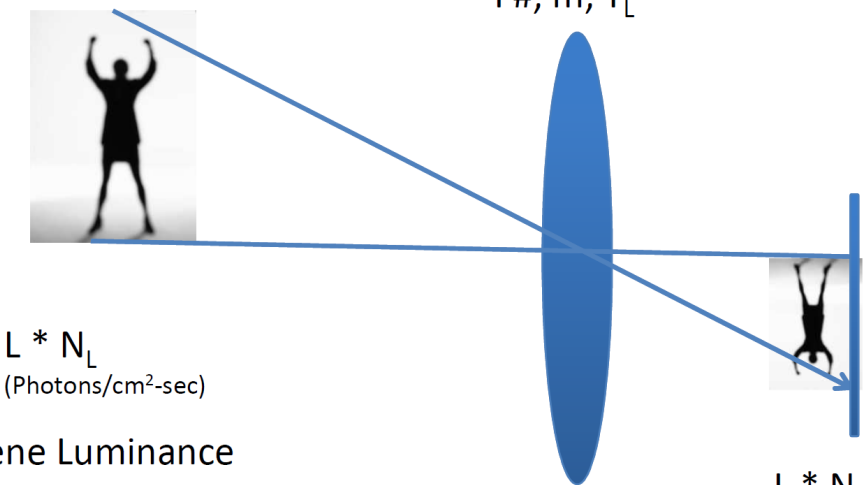
Pixel Size Impact

C_D = contrast



Limited by pixel size

Delivering photons to the sensor: the impact of Imaging Lens F# and magnification



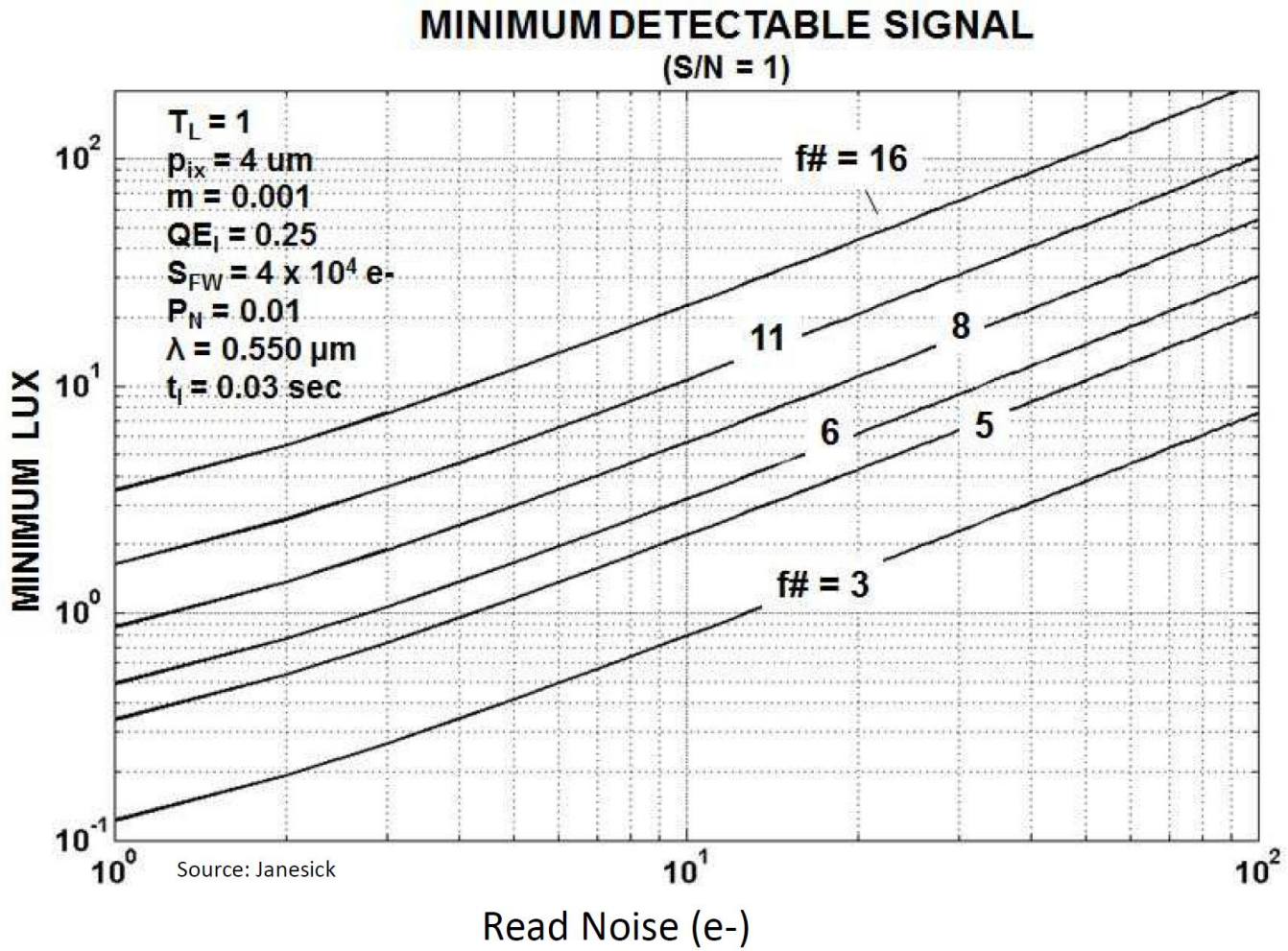
m = magnification
T_L = Transmission of Optics
N_L= photons/cm^2-sec/lux
L=Luminance level (lux)

$$\frac{T_L}{4*F\#^2*(1+m)^2}$$ (Photons/cm2-sec)

Incident Luminance at Sensor

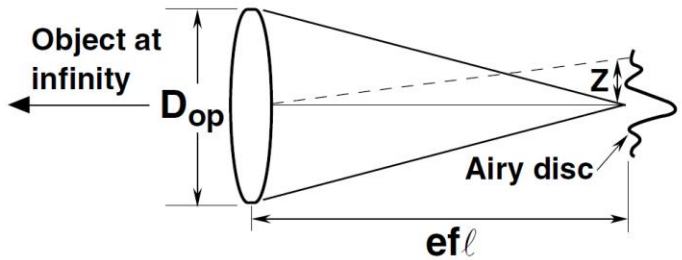
How much does the lens spread the light flux? (magnification)

F#, system noise impact

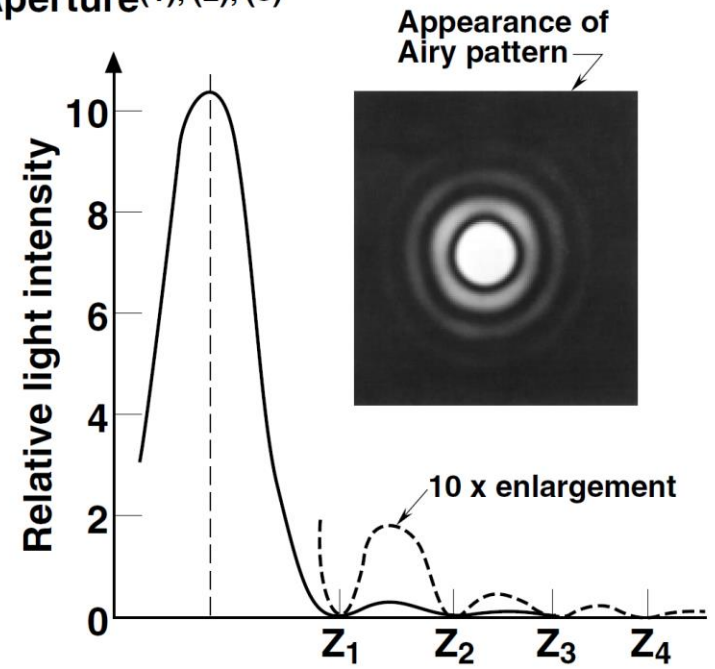


Spatial Impulse Response of an Optical System

The Airy Pattern: Optical Diffraction of a Circular Unobscured Aperture[1], [2], [3]



$\overline{\lambda}$ = mean wavelength
f# = focal ratio = $ef\ell/D_{op}$
$ef\ell$ = effective focal length
D_{op} = optical aperture diameter

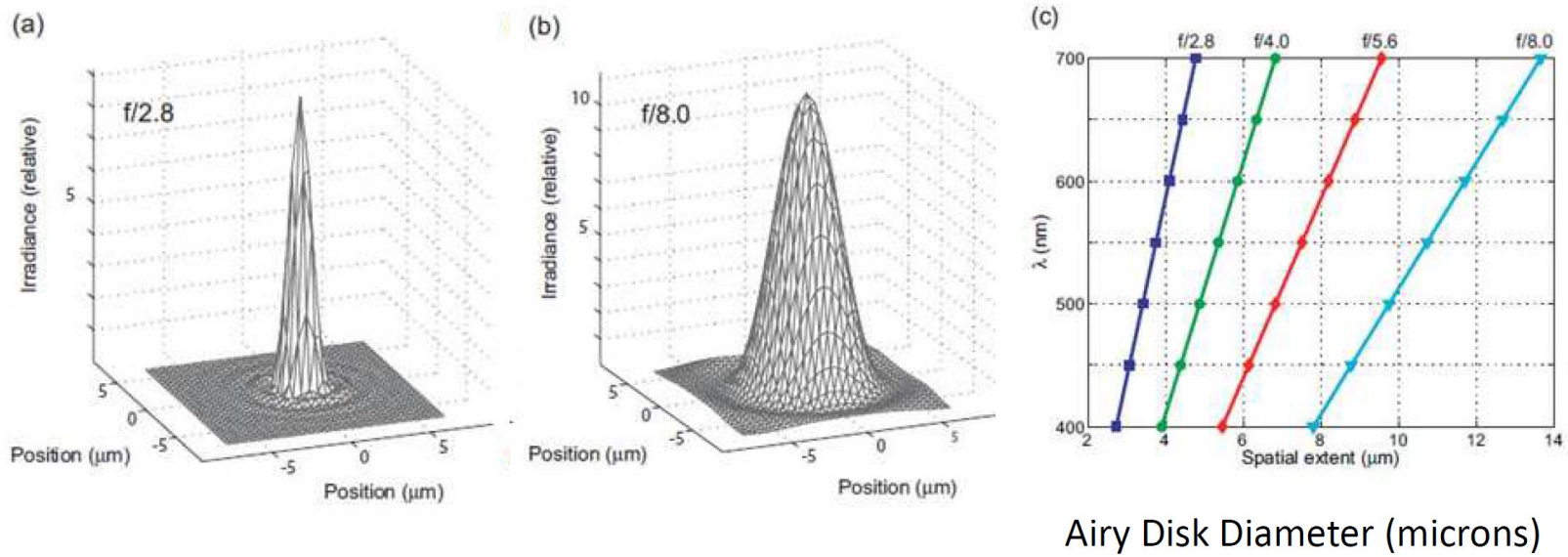


$Z_1 = 1.22\,\overline{\lambda}\,f\# = 1.22\,\overline{\lambda}ef\ell/D_{op}$

$Z_n = nZ_1$

[1] W. J. Smith, *Modern Optical Engineering*, McGraw-Hill, New York, 1966, pp. 135 – 139.
[2] J. W. Goodman, *Introduction to Fourier Optics*, McGraw-Hill, New York, 1968, pp. 63 – 66.
[3] M. Born and E. Wolf, *Principles of Optics*, Pergamon Press, 5th Edition, Oxford, 1975, pp. 394 – 398.

Optics and the Airy Disk:
Focal ratio: Sets spot size for diffraction limited optics



Airy Disk Diameter (microns)

Source: Catrysse

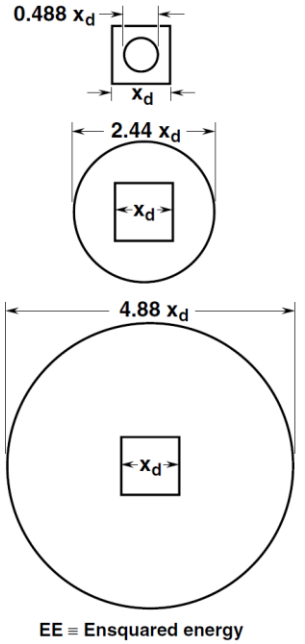
~3 microns, f/2.8

~10 microns, f/8.0

OPTIMUM PIXEL SIZE

Q Parameter Determines Optical Blur Sampling

Detector Size and Airy Disk vs Q



Q = 0.2 EE = 0.904

Q = 1.0 EE = 0.499

Q = 2.0 EE = 0.170

Increasing Q

Decreasing EE

Radius of first zero of airy disk = 1.22* λ/D;
Linear obscuration ratio = 0.20
Fraction of PSF energy with circle of first zero = 0.76

EE ≡ Ensquared energy

0692-96

Optical Q Parameter

Definitions

- Optical Q parameter is useful in quantifying spatial sampling of system optical blur
  - Specifies ratio of optical blur diameter to the pixel pitch (or pixel size)
- $Q \equiv \frac{\bar{\lambda} f\#}{x_p} = \frac{\bar{\lambda} ef\ell}{x_p D_{op}} = \frac{2f_n}{f_{co}}$

where

$f\# = \frac{ef\ell}{D_{op}}$; $f_n = \frac{1}{2x_p}$; $f_{co} = \frac{1}{\bar{\lambda} f\#}$

  - β ≡ number of detector widths that fit inside first zero of optical Airy pattern

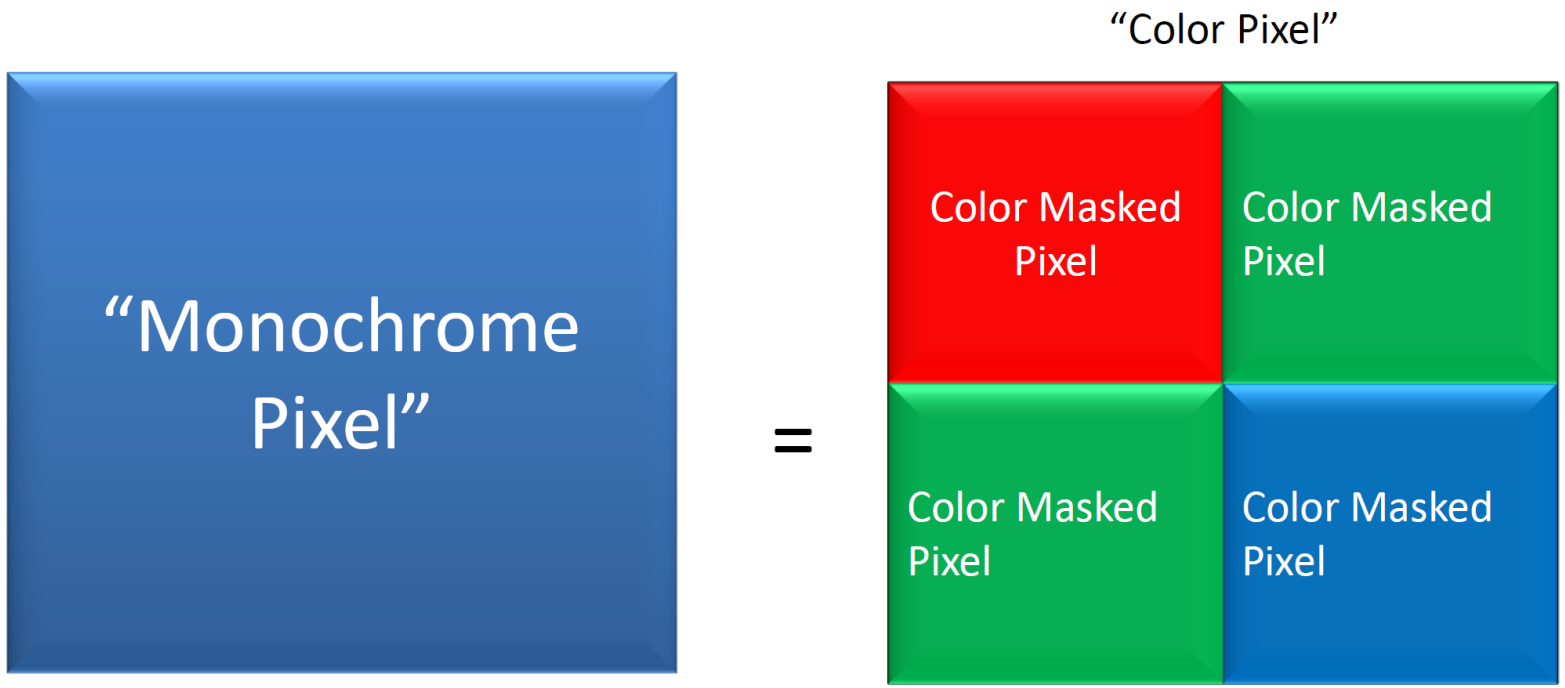
$\bar{\lambda}$	= center wavelength
f#	= focal ratio
D_{op}	= optical diameter
$ef\ell$	= effective focal length
x_p	= detector pitch distance
x_{det}	= detector width
f_n	= spatial frequency at which Nyquist criteria is met
f_{co}	= optical system spatial cutoff frequency
EE	= ensquared energy

Q	β	f_n/f_{co}	EE	Interpretation
0.5	1.22	0.25	0.88	Optical blur under sampled by 4 ×
1.0	2.44	0.50	0.50	Optical blur under sampled by 2 ×
1.5	3.66	0.75	0.31	Optical blur under sampled by 1.3 ×
2.0	4.88	1.00	0.17	Exact Nyquist sampling of optical blur

Note: High fill factor assumed then: $x_p \equiv x_{det}$

0285-03

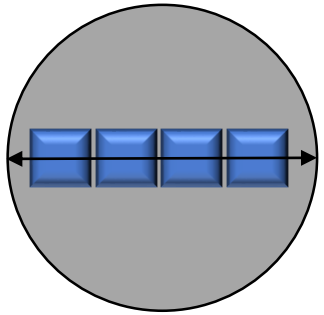
What changes for color imaging?



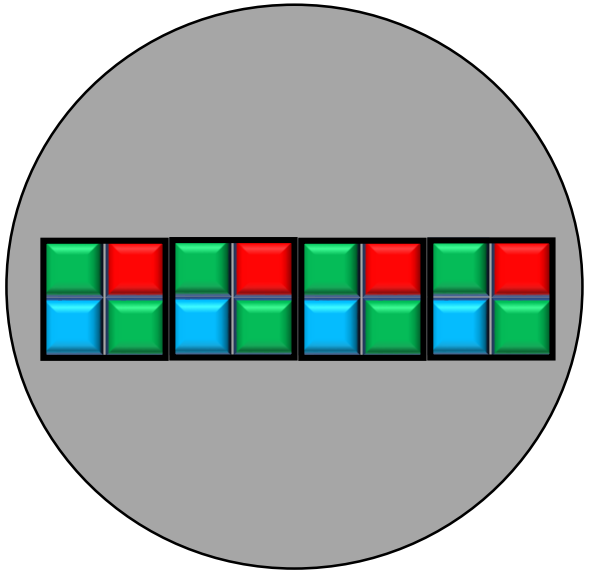
Color Masked vs Monochrome Pixels: Optimum spot size, F# must double

Adding color mask to monochrome pixel means sampling unit is 2x the width vs mono, so Airy Diameter must be 2x larger
-> make F# for color 2X F# for mono

Pixel size = Airy Diameter/4.88



Pixel size = Airy Diameter/4.88



Why Proper Sampling is important: Aliasing Artifact Example: Color image

Source: Catrysse

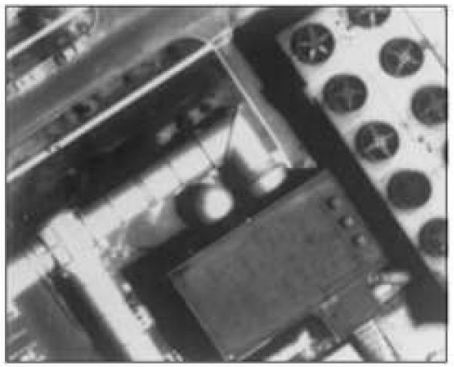
Undersampled
f/2.8, 3 micron pixel

Undersampled
f/8, 3 micron pixel

Proper sampling
f/2.8, 1.5 micron pixel

Must properly match F# to pixel size to avoid aliasing artifacts

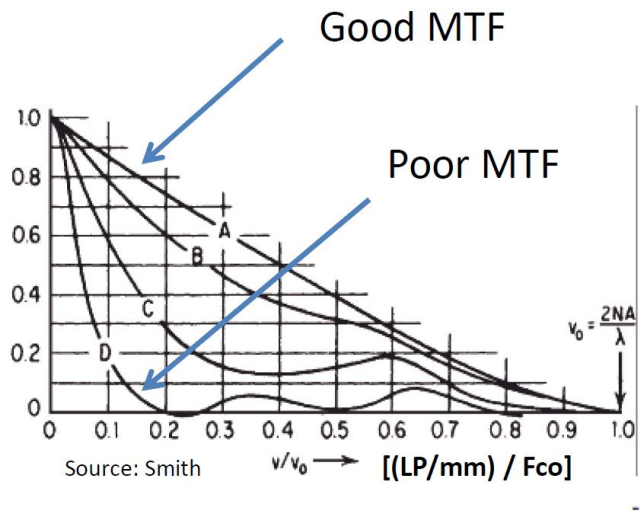
Imaging optics:
MTF impact on image quality



Good MTF
Sharp Image

Source: Lomheim

Poor MTF
Blurry Image



Source: Smith

Fco = Fcutoff = $1/(\lambda * f\#)$

Part 11:
Design Problem: Selecting the right Image Sensor for the job

Points for Consideration

- How bright is target and background?
  - If really dim target:
    - Long (minutes) exposures: cooled sensors. Concern over dark signal: dark shot noise, dark FPN
      - Big pixels collect more light but can mean physically large sensor with corresponding very expensive optics
      - High QE: doubled QE means exposure time cut in half for same SNR target
      - Full frame CCD has highest fill factor, BSI for even higher QE, esp in blue (scattering)
      - CCD typically better choice: big sensors, big pixels, simple wafer fab process & photolithography
      - Charge trapping/residual image concern in full frame CCD
        - Might need light flood protocol (Cassini, Galieo)
        - Concern about increased dark shot noise (extra cooling to compensate

Points for Consideration

- If really bright target:
  - Concern about saturated pixels
    - Larger pixels have higher well capacity but:
      - Either smaller # pixels for fixed format sensor
      - Larger format sensor
        - Larger illuminated circle: more costly optics
        - Greater distance from rear optical element to focal plane (thicker camera)
  - Very short exposures
    - Prefer electronic shutter: interline CCD, CMOS
      - If motion also present:
        - Global snap shutter CMOS or Interline CCD (global snap shutter)

Points for Consideration

- Video:
  - Full Frame CCD needs mechanical shutter: not reliable for spaceflight.
  - Frame Transfer CCD can offer Full Frame CCD performance w/o a mechanical shutter, but if exposure time is short compared to frame transfer time, then smearing is a problem
  - Interline CCD can provide short exposures & global shutter with sensitive and large pixels, but still is a serial readout limiting frame rate / pixel count
  - CMOS rolling shutter offers good low light performance (3T pixel) but suffers from distortion with motion video if motion is high compared to scan rate
    - Global snap shutter CMOS avoids distortion but has lower QE (less optically active circuitry/pixel), higher noise (dark signal on storage node, aggravated by LOW frame rate, elevated temperature)
  - BSI CMOS can reduce exposure time via QE boosting (less shutter-open time means less smear)
  - High bandwidth data transfer on-chip using TSV technology can provide good results with rolling shutter and motion video (fast scan rate from high bandwidth connection on-chip to buffer memory)
    - Can use pixel with higher fill factor (3T): more sensitive to support high frame rate w/o excessive scene brightness

Points for Consideration

- Very High frame rate video:
  - CMOS wins hands down
    - Can have A/D converter per column: can split columns top/bottom to get 2 ADCs/column
    - Use multiple high bandwidth SERDES for output links
    - How much bandwidth can you capture on the system side?
      - 16Mpixel/frame x 1000 frames/sec = 16 Gigapixels/sec
      - 16bits/pixel = 256gigabits/sec, 32Gigabytes sec

      Link standards:
      - SATA3 (HDD): 6 Gbits/sec
      - NVME (SSD): 16Gigabits/sec

      Run multiple parallel links to RAID array of SSDS?
    - How much storage can you provide?
      - 32Gigabytes/sec fills a 4Terabyte “drive” in 125 seconds
  - Short bursts can be stored on-chip in DRAM using TSV technology in stacked die configurations

Points for Consideration

- Special Purpose: NearIR
  - Deep penetration of NIR Photons means poor diffusion MTF unless deep depletion regions
    - High resistivity substrates
    - BSI with high reverse bias
      - ITO (transparent rear electrode with reverse bias?)
  - CCD or CMOS is OK
- Special purpose: NearUV (dermatology)
  - No frontside illumination: too much scattering of light
  - BSI wins. CMOS or CCD. Cheap BSI CMOS from cellphone camera?
- Special Purpose: XRAY
  - Scintillator for down-conversion to visible: reduce shot noise, improve SNR
    - But must be accommodated in illumination path
  - Direct XRAY
    - Will work but will be noisy

Points for Consideration

- Wide FOV
  - Single aperture, staring array: lens corner distortion, light intensity roll-off (proportional to cosine^4 of chief ray angle)
    - Realtime flat fielding to correct light rolloff
    - Or simple lens shading correction model
  - Multi smaller-FOV apertures stitched: less cosine^4 rolloff, less lens corner distortion correction, need image registration/stitching. Cheap CMOS for 360 cameras (ie AR)?