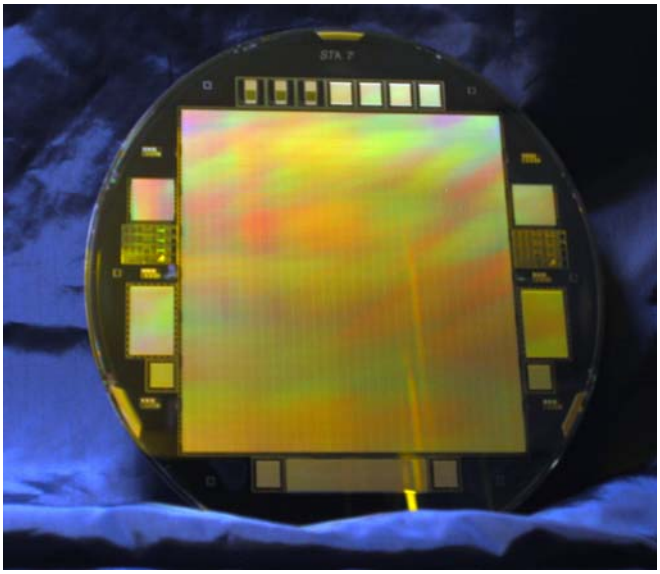
SEMICONDUCTOR TECHNOLOGY ASSOCIATES, Inc

STA1600A
10600 x 10600 Element Image Area Full Frame CCD Image Sensor

FEATURES

- 10560 x 10560 Photosite Full Frame CCD Array
- 9 μm x 9 μm Pixel
- 95.22mm x 95.05mm Image Area
- 100% Fill Factor
- Readout Noise Less Than 20 Electrons at 10MHz
- Dynamic Range > 75dB
- 16 Two Stage Source Follower Output Channels
- Three-Phase Buried Channel NMOS Image area
- Three-Phase Buried Channel Readout Registers
- Multi-Pinned Phase (MPP) optional



GENERAL DESCRIPTION

The STA1600 is a 10560 x 10560 image element solid state Charge Coupled Device (CCD) Full Frame sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The STA1600 is organized in two halves each containing an array of 10560 horizontal by 5280 vertical photosites. The pixel spacing is 9μm x 9μm. For dark reference, each readout line is proceeded by 8 dark pixels. This imager is available in a full frame transfer configuration (shown) or a split frame transfer configuration with shield metalization covering half of the imager. The split frame transfer architecture allows higher frame rate operation through four readout quadrants, whereas the single-sided approach allows readout through two readout quadrants. The STA1600 is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

Vertical Charge Shifting: The Full Frame architecture of the STA1600 provides video information as a single sequential readout of 5280 lines containing 1330 photosite. At the end of an integration period the ϕA_1, ϕA_2, and ϕA_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into an Upper and Lower half. Each 10580 x 5280 halve may be clocked independently or together. Horizontal Transport registers along the top and bottom permit simultaneous readout of both halves. The STA1600 may be clocked such that the full array is readout by the Upper or Lower Transport registers.

Horizontal Charge Shifting: ϕS_1, ϕS_2 and ϕS_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the eight amplifiers at the bottom or top of the image frame storage region

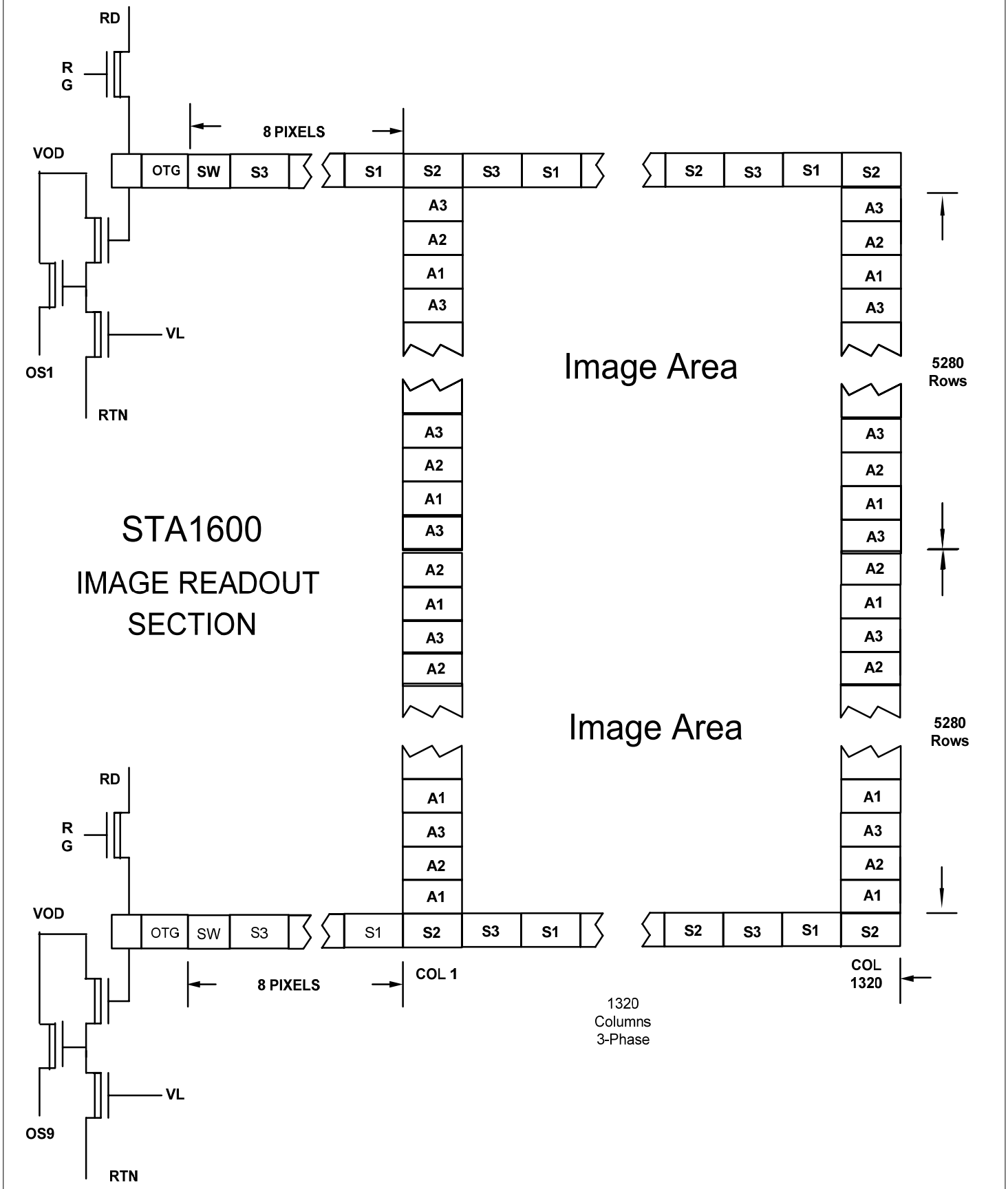
The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 8 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

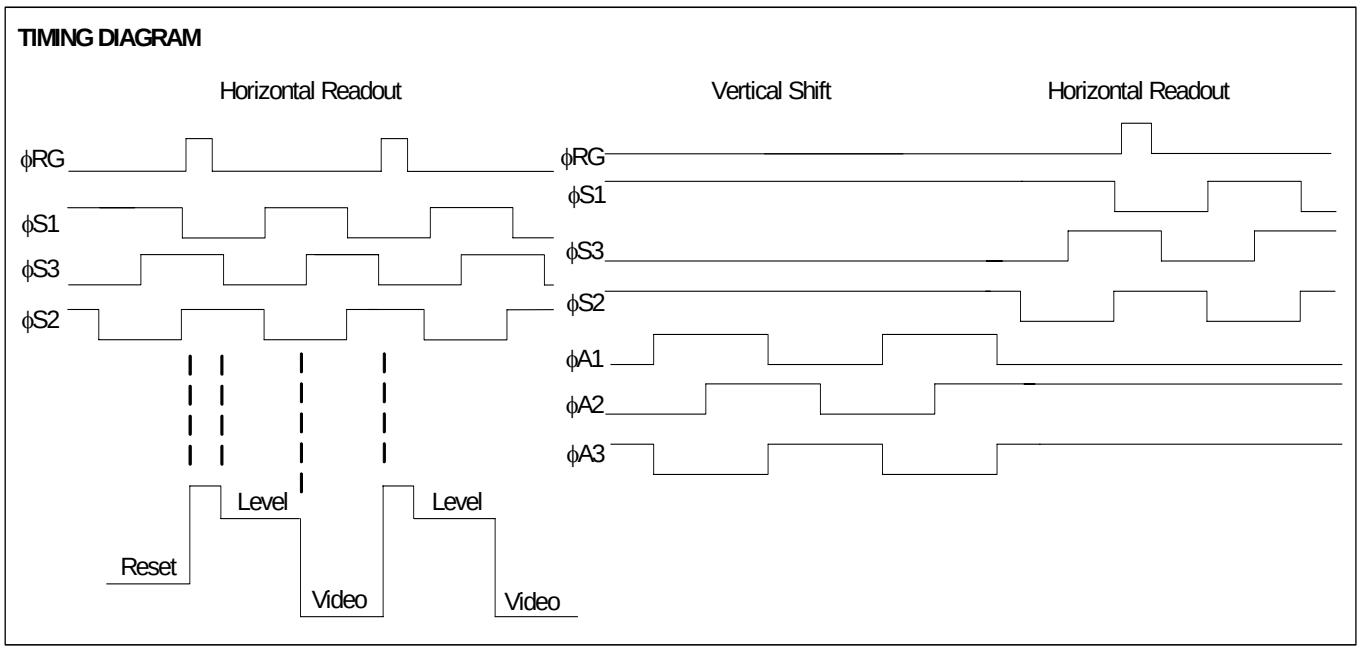
The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ϕH_2 for normal full resolution readout.

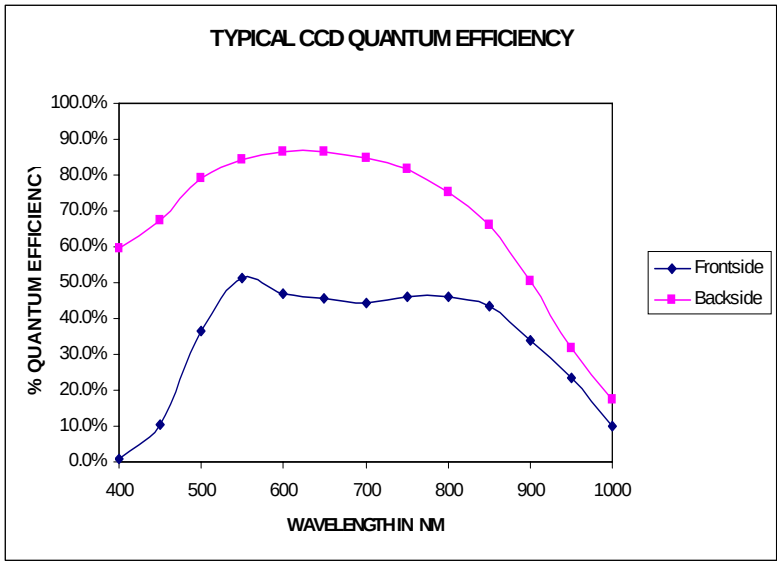
The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

Output Amplifier: The STA1600 has one output amplifier at the end of each Horizontal register. They are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced. The capacitor is then reset via the reset MOSFET with ϕRG to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground and constitutes the video output from the device.


RD
R
G
VOD
OTG
SW
S3
8 PIXELS
S1
S2
S3
S1
S2
S3
S1
S2
A3
A2
A1
A3
VL
OS1
RTN
Image Area
5280
Rows
STA1600
IMAGE READOUT
SECTION
A1
A3
A2
A1
A3
A2
Image Area
5280
Rows
RD
R
G
VOD
OTG
SW
S3
S1
S2
S3
S1
S2
S3
S1
S2
8 PIXELS
COL 1
COL
1320
1320
Columns
3-Phase
VL
OS9
RTN





DEFINITION OF TERMS

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕA_1, ϕA_2, ϕA_3 the clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕS_1, ϕS_2, ϕS_3 the clock signals applied to the horizontal transport registers.

Reset Clock ϕRG the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal The output signal is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ϕVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

Pixel Picture element or sensor element, also called photo element or photosite

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{OD}	DC Supply Voltage		+25.0		V	
V_{RD}	Reset Drain Voltage		16.0		V	
V_{OTG}	Output Voltage	-2.0	1.0	2.0	V	
V_{VLD}	Output Load Voltage		+3.0		V	
V_{RTN}	Output Return Voltage		+2.0		V	
V_{SC}	Scupper Voltage		+20.0		V	
V_{SUB}	Substrate Ground		0.0		V	

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V\phi_{S(1,2,3)}$	Horizontal Multiplexer Clock	+5.0	-5.0	V	Note 1
$V\phi_{SW}$	Summing Gate Clock	+5.0	-5.0	V	Note 1
$V\phi_{V(1,2,3)}$	Vertical Array Clocks	+3.0	-10.0	V	Note 1
$V\phi_{RG}$	Reset Array Clock	+5.0	-5.0	V	Note 1

Note 1: ϕH = 200pF, ϕV = 15,000pF. All clock rise and fall times should be > 10 ns.

AC CHARACTERISTICS Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MH_z Horizontal Data Rate, 6µSec Vertical shift cycle.

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{ODC}	Output DC Level		16.0		V	
Z	Suggested Load Register	1.0	5.0	20.0	kΩ	

PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{SAT}	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	 70K	700 80K 7.0	 100K	mV e- µV/e-	Note 1
PRNU	Photo Response Non- Uniformity Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025	<1.0	2.0	nA/cm^2	Note 2
R	Responsivity		1.0		$V\mu j/cm^2$	
rms	Noise		5 -20		e-	

Note 1: Maximum well capacity is achieved in Buried Channel Mode.
Note 2: Values shown are for 25^0C. Dark current doubles for every 5^0- 7^0C.

QUANTUM EFFICIENCY ENHANCEMENTS

The STA1600 CCD area arrays can be backside thinned for increased QE. The incident illumination enters through the backside of the array, and since no photons are absorbed in the polysilicon gate structures, the QE is increased. Also available are front side illuminated devices which can be coated with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The STA1600 is available in various standard grades, as well as custom selected grades. Consult Semiconductor Technology Associates for available grading information and custom selections.

WARRANTY

Within twelve months of delivery to the end customer Semiconductor Technology Associates will repair or replace, at our option, any image sensor product if any part is found to be defective in materials or workmanship. Contact Semiconductor Technology Associates for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Semiconductor Technology Associates certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under which it is furnished

STA1600 Image Sensor Connector Pin Designation

J1	Label
1	OD4
2	RTN4
3	VLD4
4	OS4
5	OD3
6	RTN3
7	VLD3
8	OS3
9	OD2
10	RTN2
11	VLD2
12	OS2
13	OD1
14	RTN1
15	VLD1
16	OS1
17	OTG1
18	RD
19	RG
20	S3
21	S1
22	SC
23	A1-1
24	A3-1
25	A1-2
26	A3-2
27	GND
28	OTG4
29	GND
30	GND
31	GND
32	GND
33	OTG3
34	GND
35	GND
36	GND
37	GND
38	OTG2
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	SW
46	S2
47	GND
48	GND
49	A2-1
50	GND
51	A2-2

J2	Label
1	A3-4
2	A1-4
3	A3-3
4	A1-3
5	SC
6	S1
7	S3
8	RG
9	RD
10	OTG8
11	OS8
12	RTN8
13	OD8
14	OTG7
15	OS7
16	VLD7
17	RTN7
18	OD7
19	OS6
20	VLD6
21	RTN6
22	OD6
23	OS5
24	VLD5
25	RTN5
26	OD5
27	A2-4
28	GND
29	A2-3
30	GND
31	GND
32	S2
33	SW
34	GND
35	GND
36	VLD8
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	OTG6
49	OTG5
50	GND
51	GND

J3	Label
1	A3-5
2	A1-5
3	A3-6
4	A1-6
5	SC
6	S1
7	S3
8	RG
9	RD
10	OTG9
11	OS9
12	RTN9
13	OD9
14	OTG10
15	OS10
16	VLD10
17	RTN10
18	OD10
19	OS11
20	VLD11
21	RTN11
22	OD11
23	OS12
24	VLD12
25	RTN12
26	OD12
27	A2-5
28	GND
29	A2-6
30	GND
31	GND
32	S2
33	SW
34	GND
35	GND
36	VLD8
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	OTG11
49	OTG12
50	GND
51	GND

J4	Label
1	OD13
2	RTN13
3	VLD13
4	OS13
5	OD14
6	RTN14
7	VLD14
8	OS14
9	OD15
10	RTN15
11	VLD15
12	OS15
13	OD16
14	RTN16
15	VLD16
16	OS16
17	OTG16
18	RD
19	RG
20	S3
21	S1
22	SC
23	A1-8
24	A3-8
25	A1-7
26	A3-7
27	GND
28	OTG13
29	GND
30	GND
31	GND
32	GND
33	OTG14
34	GND
35	GND
36	GND
37	GND
38	OTG15
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	SW
46	S2
47	GND
48	GND
49	A2-8
50	GND
51	A2-7