RBI/CHARGE TRAPPING
&
CMOS IMAGE SENSORS

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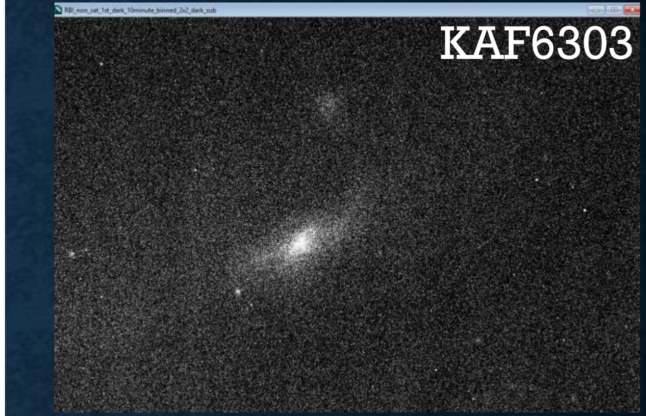
Residual Image Management

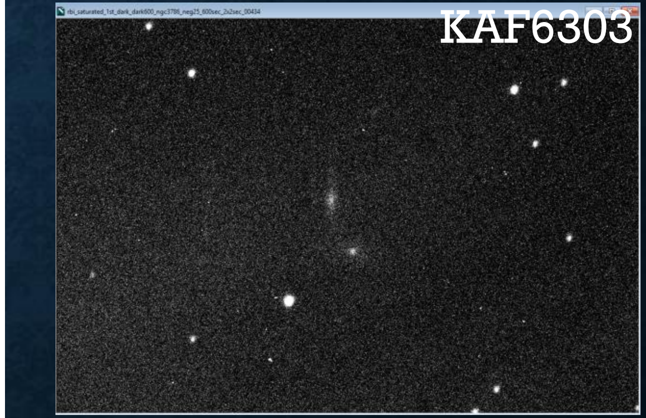
Residual Image

Image

5 Minute Dark
Immediately
following
image

5 Minute Dark
One hour
following
image





Residual Image

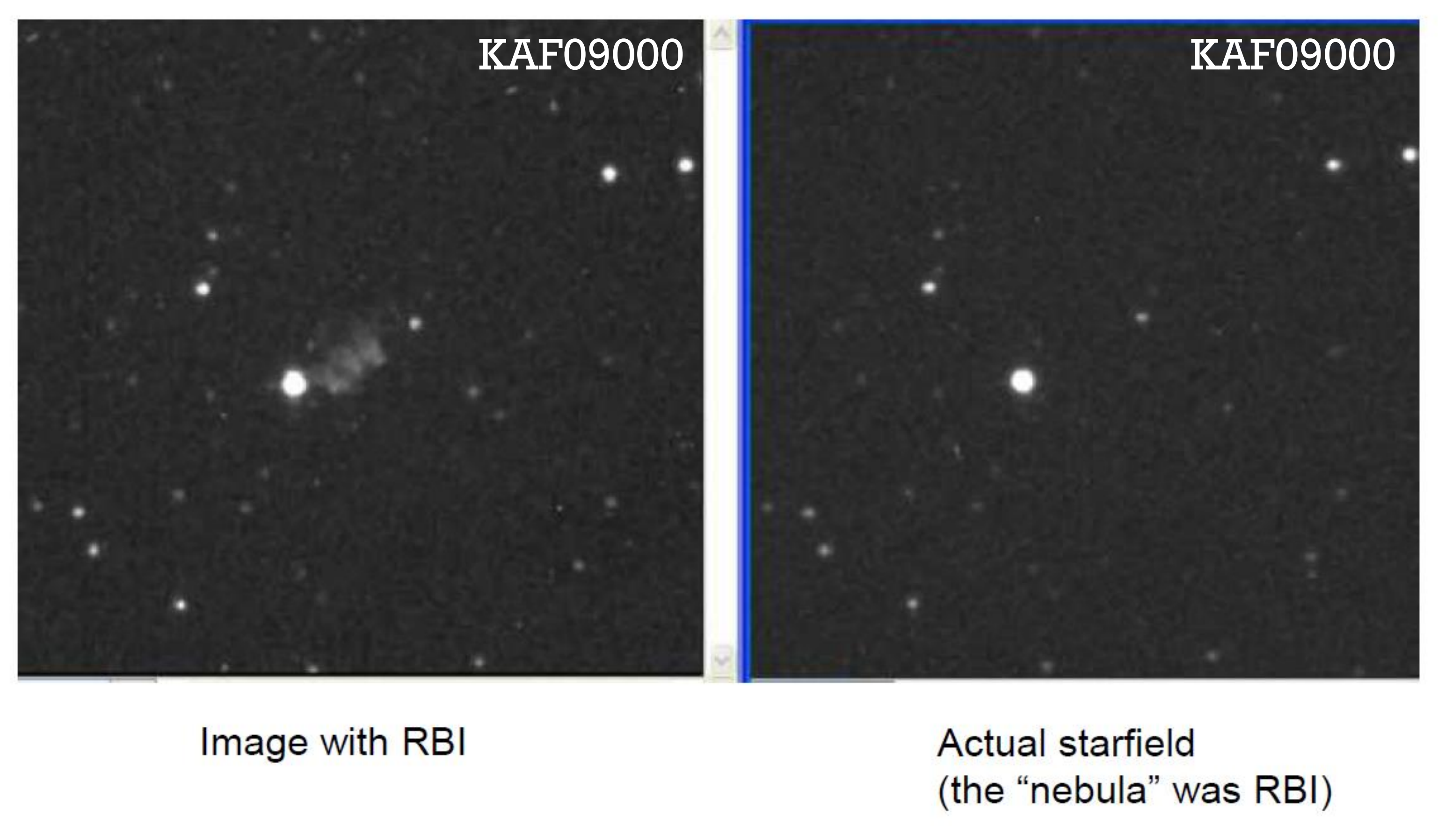
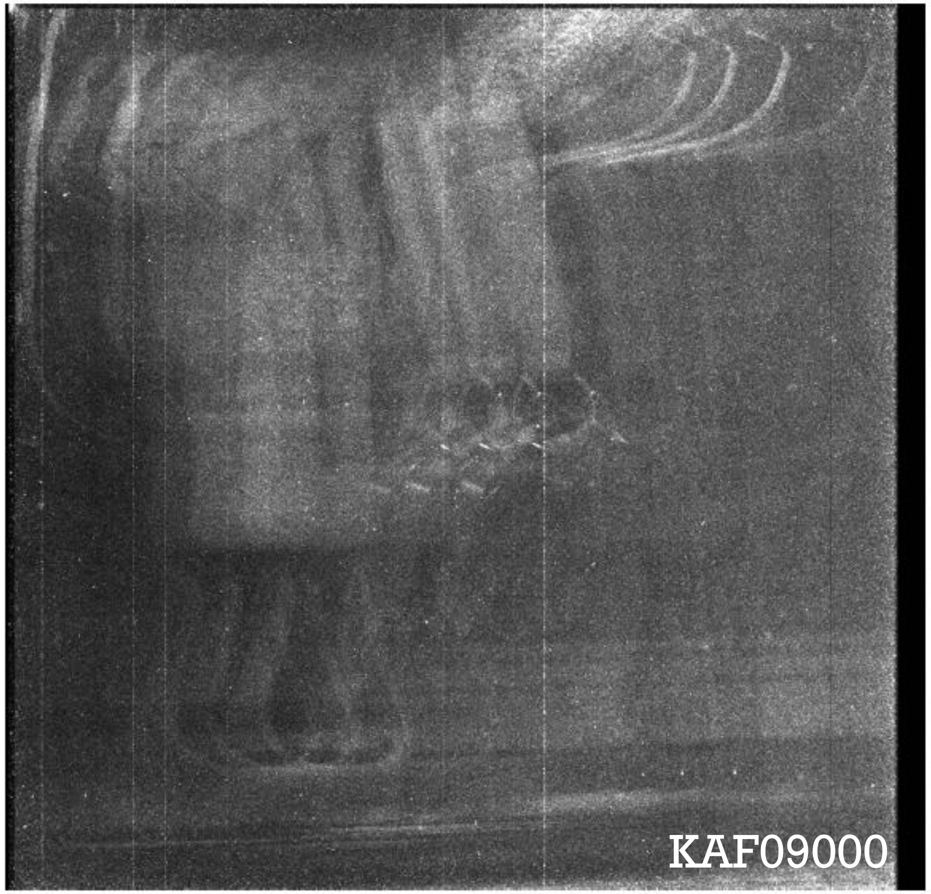


Image with RBI

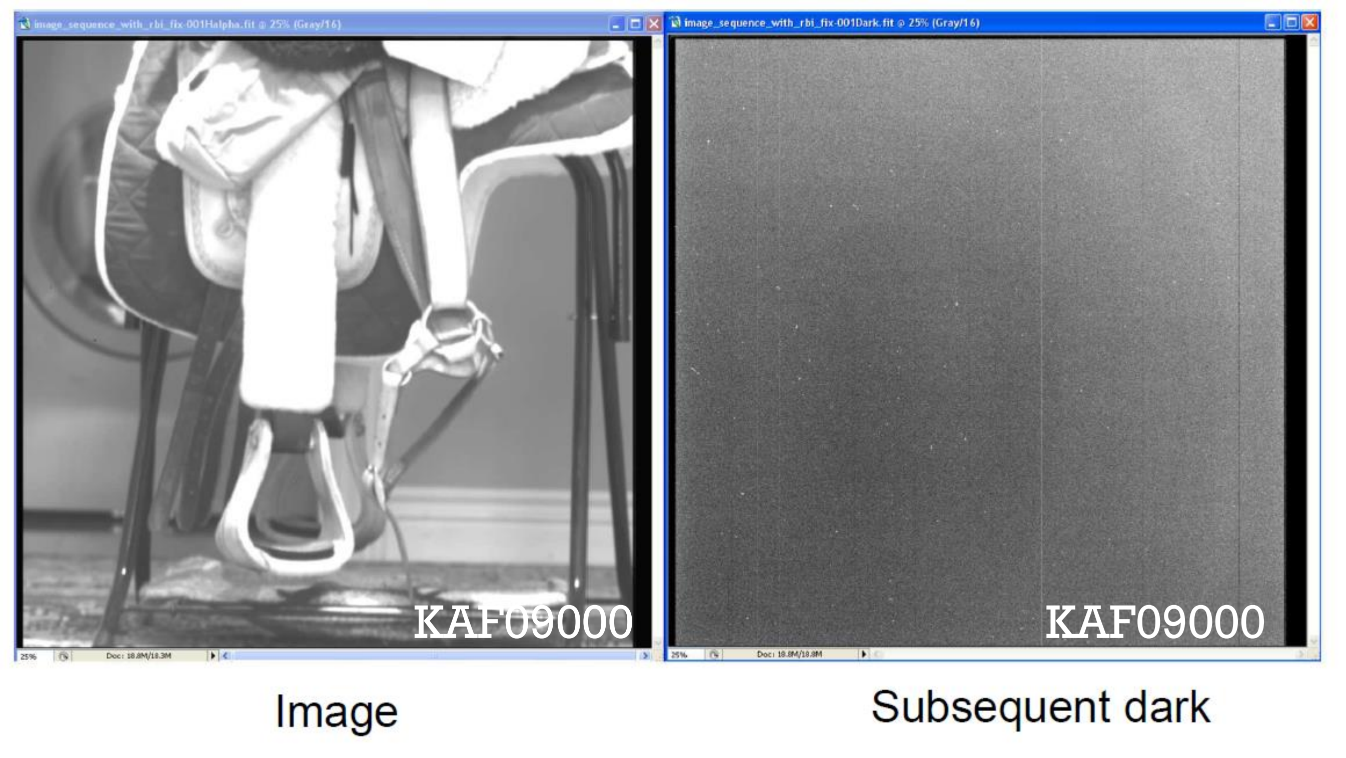
Actual starfield
(the “nebula” was RBI)

Residual Image



Five minute dark exposure
following
four light exposures

Residual Image Avoidance using Light Flood



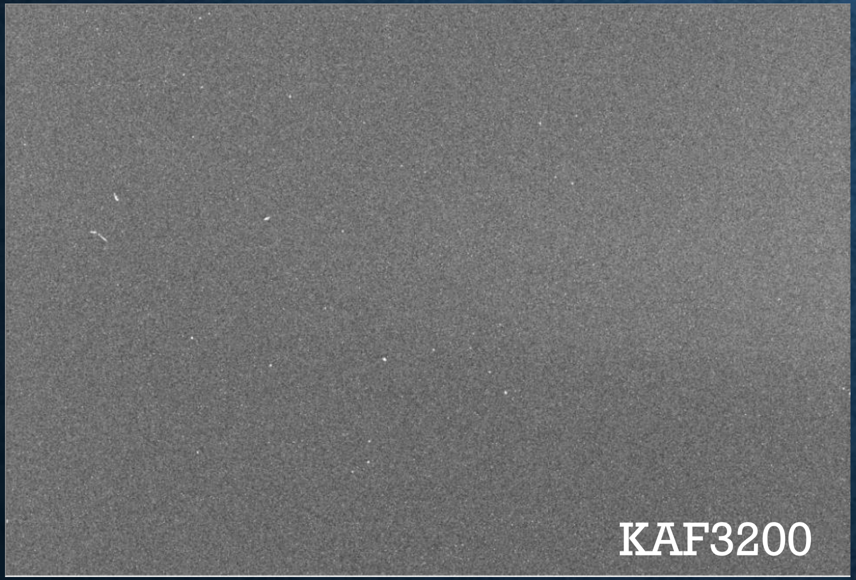
Image

Subsequent dark

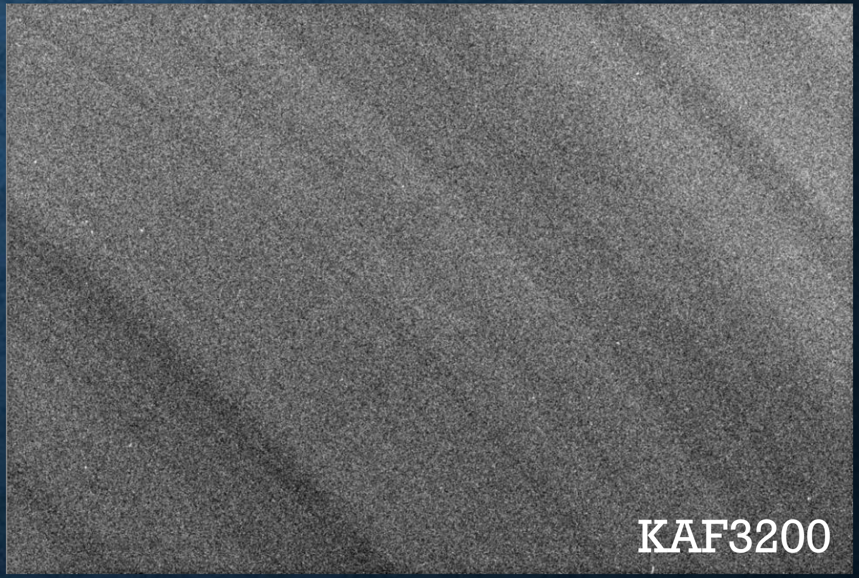
With light flood: the dark shot noise is increased significantly unless deep cooling is used

Non Uniformity of Trap Distribution

These patterns can occur after shooting flats:
<u>If not using RBI light flood, may not be able to remove pattern via calibration</u>



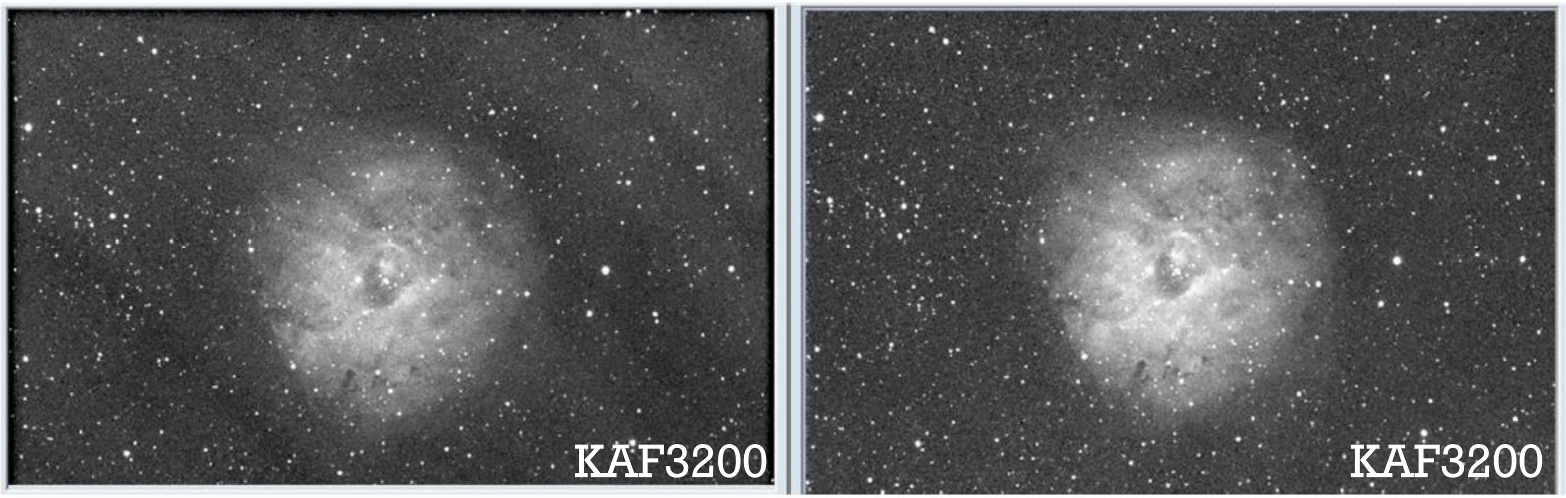
No Light Flood: Neg 15C, 300sec dark frame



With Light Flood: Neg 15C, 300sec dark frame

FULL CALIBRATION (FLATS AND DARKS)

Without RBI management you can have uncalibratable images, due to partially filled traps

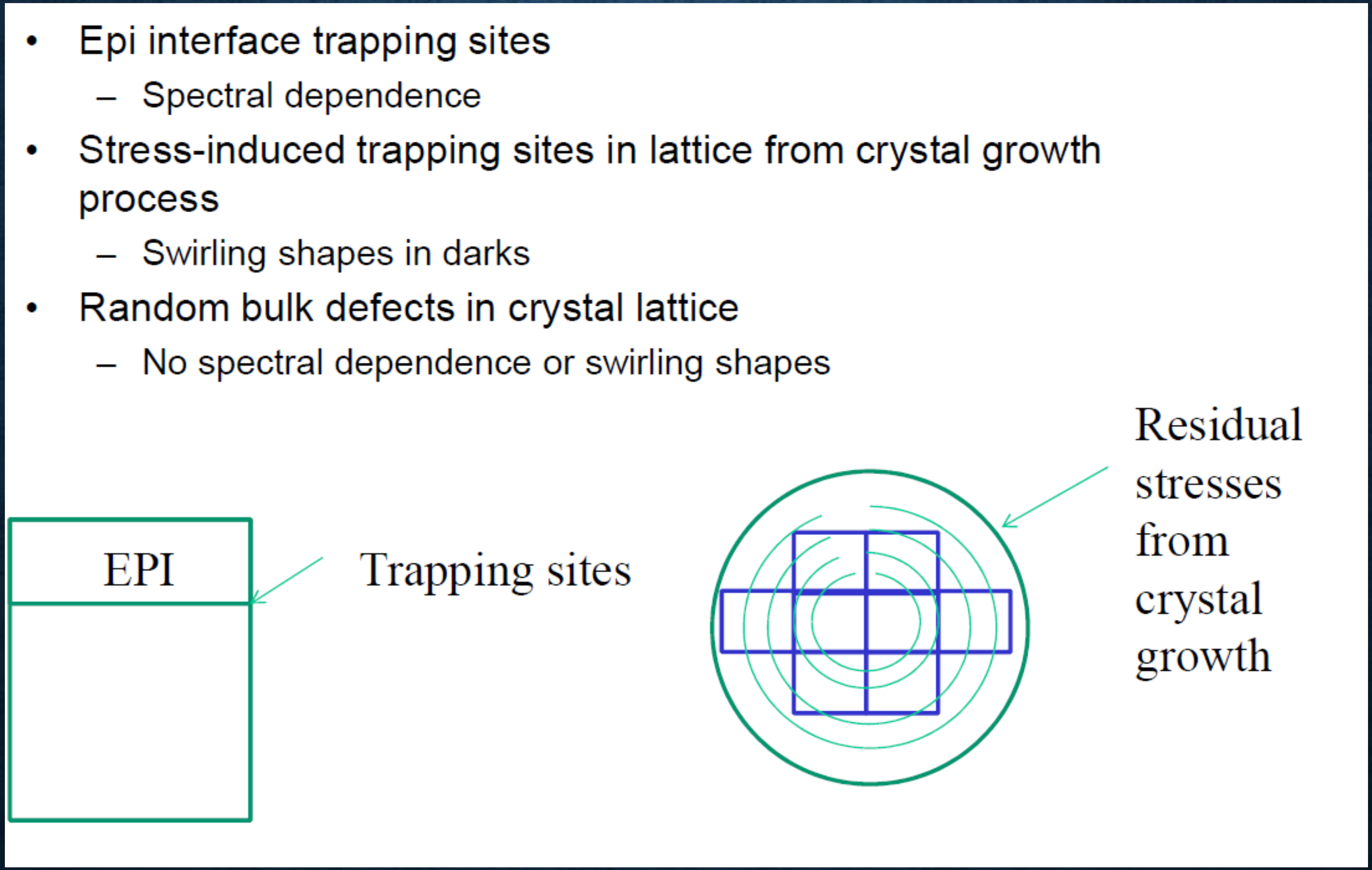


Not Calibrated
(900 second exposure)

Calibrated
(900 second exposure)

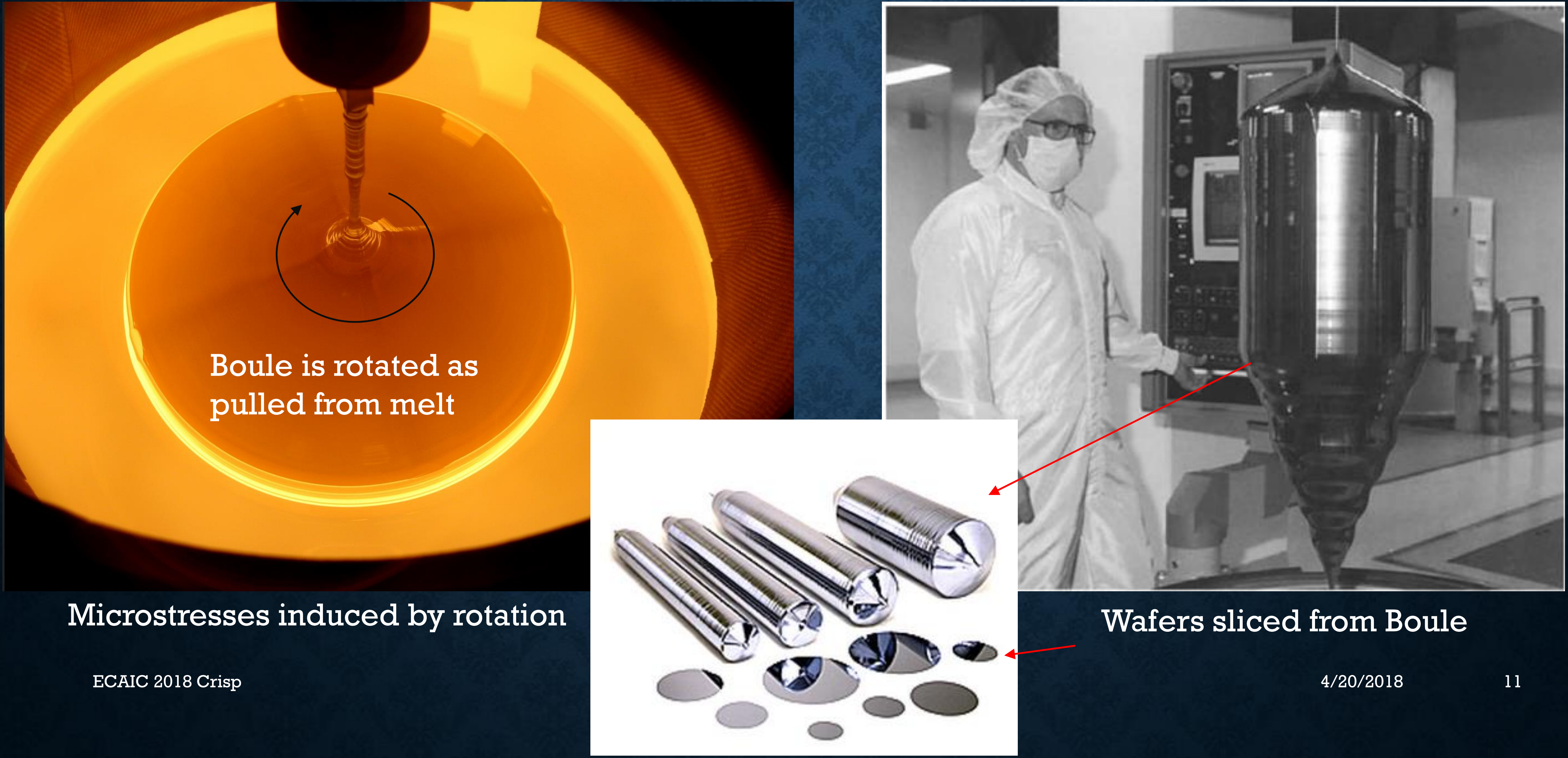
Trapping Sources

Trapping Sources



- Epi interface trapping sites
  - Spectral dependence
- Stress-induced trapping sites in lattice from crystal growth process
  - Swirling shapes in darks
- Random bulk defects in crystal lattice
  - No spectral dependence or swirling shapes

Silicon Boule Manufacturing (Czochralski Process)

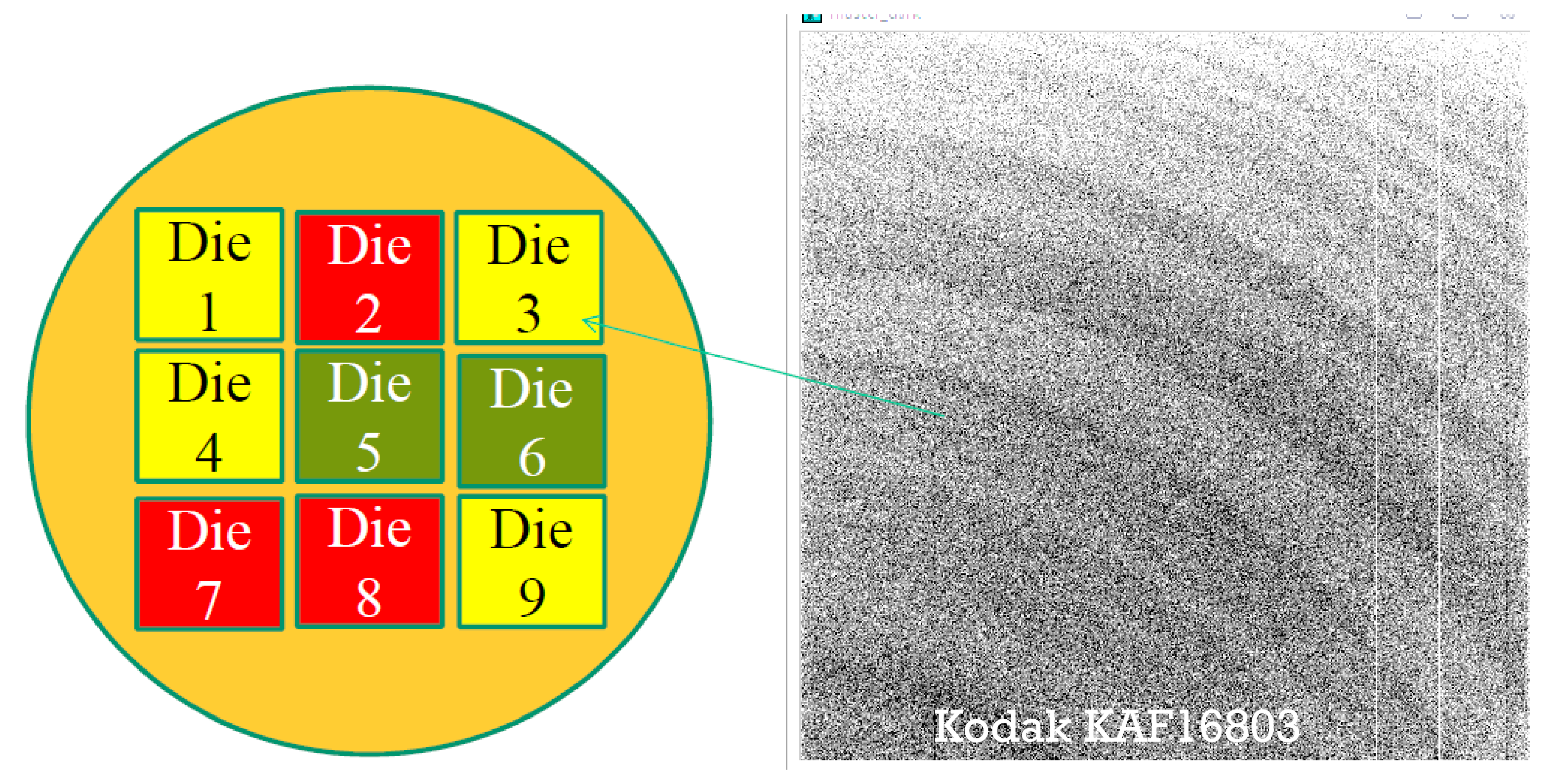


Boule is rotated as pulled from melt

Microstresses induced by rotation

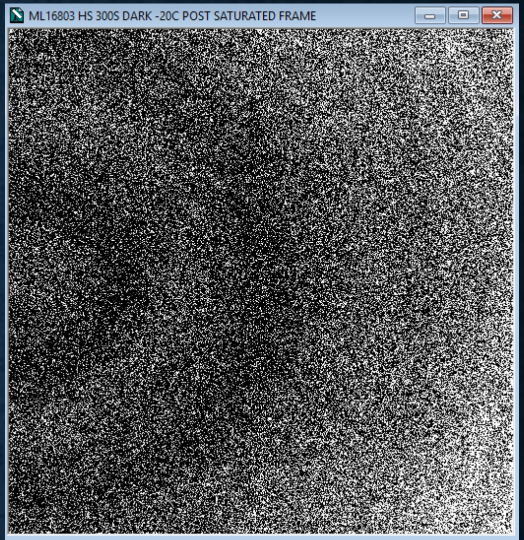
Wafers sliced from Boule

Wafer Mapping Example

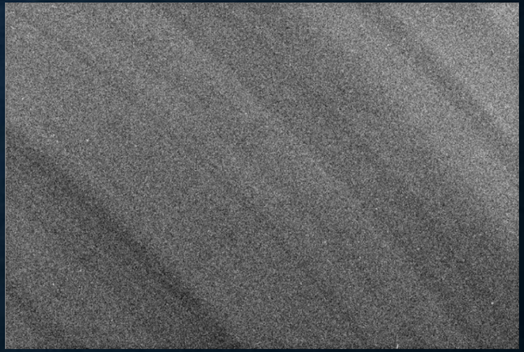


Die 1	Die 2	Die 3
Die 4	Die 5	Die 6
Die 7	Die 8	Die 9

Kodak KAF16803



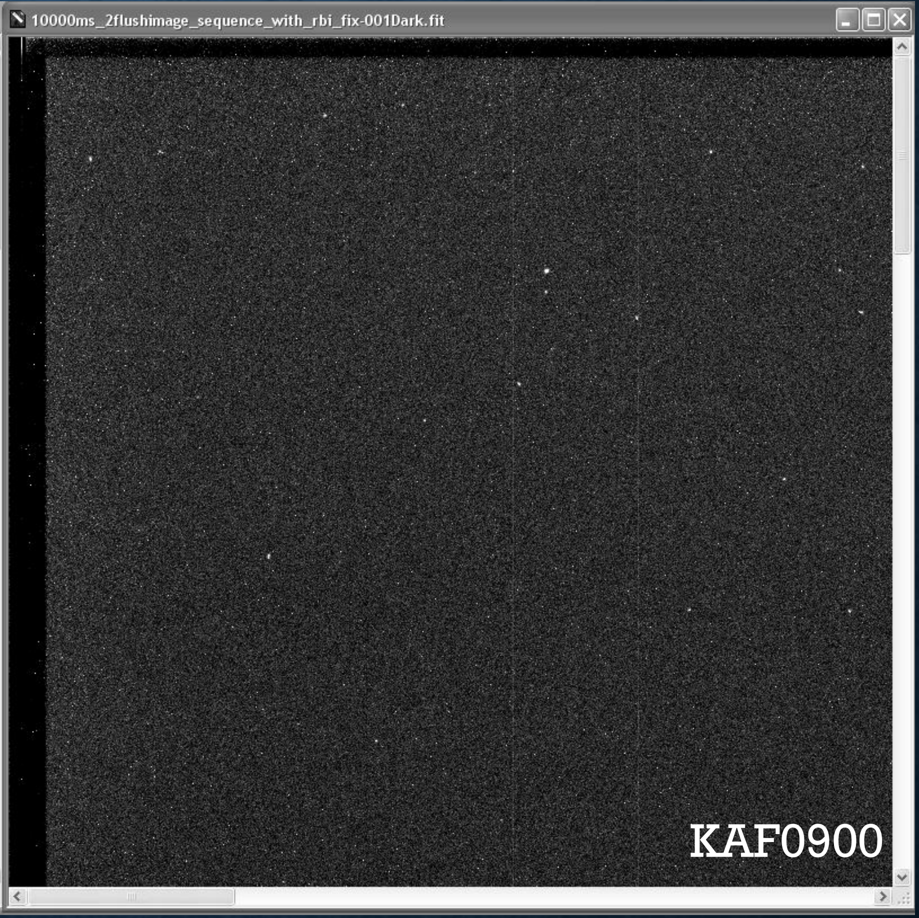
ON-Semi KAF16803



KAF3200

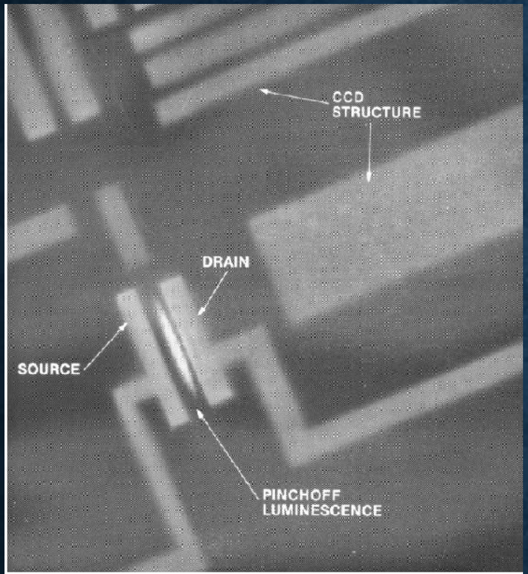
Amplifier Luminescence wo/w Light Flood

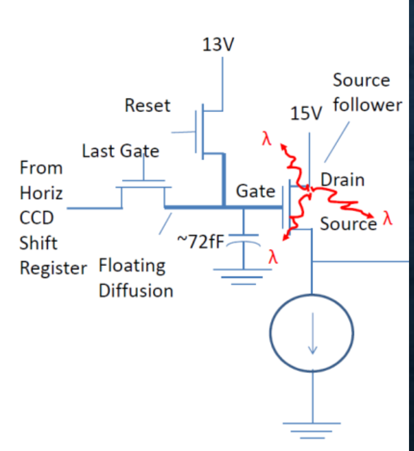
No Light Flood: Neg 40C,
1800 sec dark frame



With Light Flood: Neg 40C,
1800sec dark frame

Amplifier Luminescence Root Cause

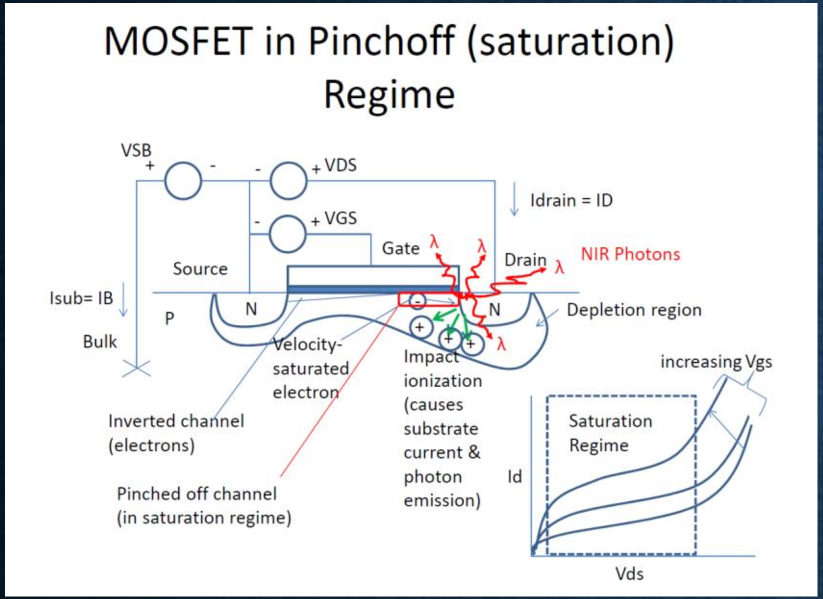




Sensor Array is saturated at power-up

- Output Source Follower Transistor is in Pinchoff region (high drain electric field)
- High drain field causes impact ionization leading to luminescence at NIR wavelengths
- This occurs at power up and may not occur again (can be a one-shot occurrence)
- Light from luminescence loads nearby trapping sites and gradually decays. If sensor cold then decay is very slow (like RBI: same traps are loaded)

Amplifier Luminescence Root Cause


MOSFET in Pinchoff (saturation) Regime

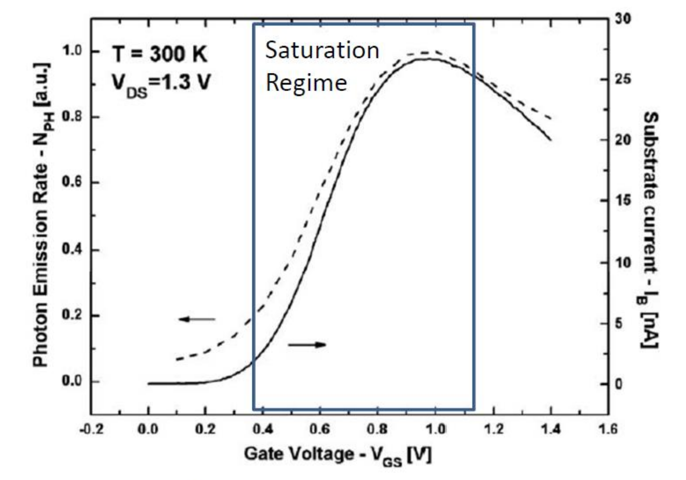


Fig. 1. Photon emission rate (dashed curve) and substrate current (solid curve) as a function of gate bias at $V_{DS} = 1.3$ V.

Saturation regime: VDS > (VGS – VT)

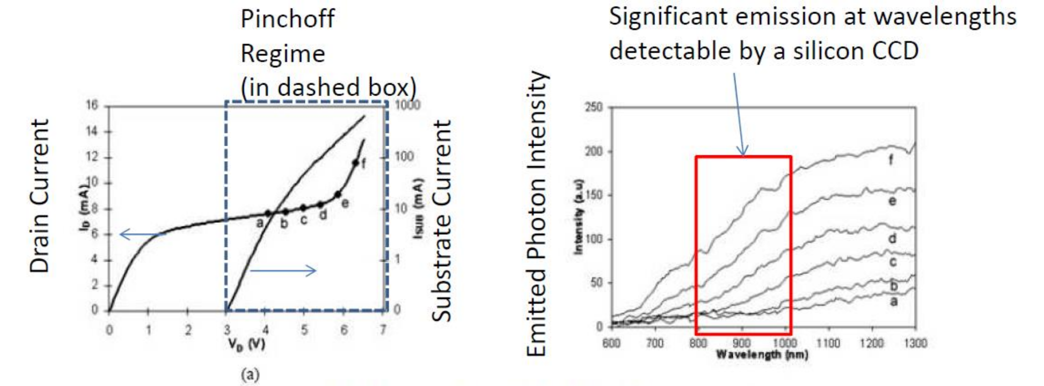
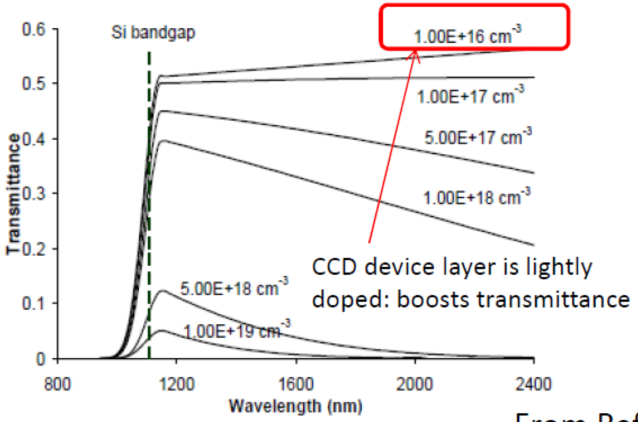


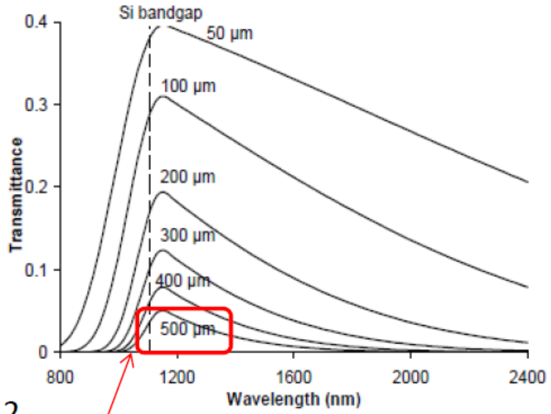
Fig. 11: (a) I_D and I_{sub} versus V_D at $V_{GS} = 3$V and (b) emission spectra at operating points a – f for 1.0μm gate length nMOSFET (nMOS1) [16]

(b)

NIR Light Transmittance Through Silicon



CCD device layer is lightly doped: boosts transmittance

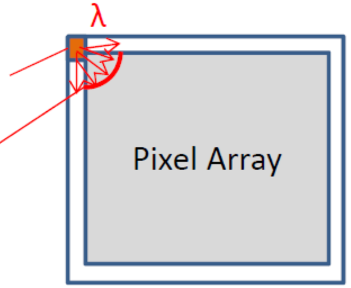


From Ref 2

Fig. 2a: Photon transmittance of 500 µm p-Si for different doping concentrations

Fig. 2b: Photon transmittance of p-Si doped at 10^{19} cm^{-3} for different backside thicknesses

Emission is in all directions



Amplifier (light source)

Affected Region

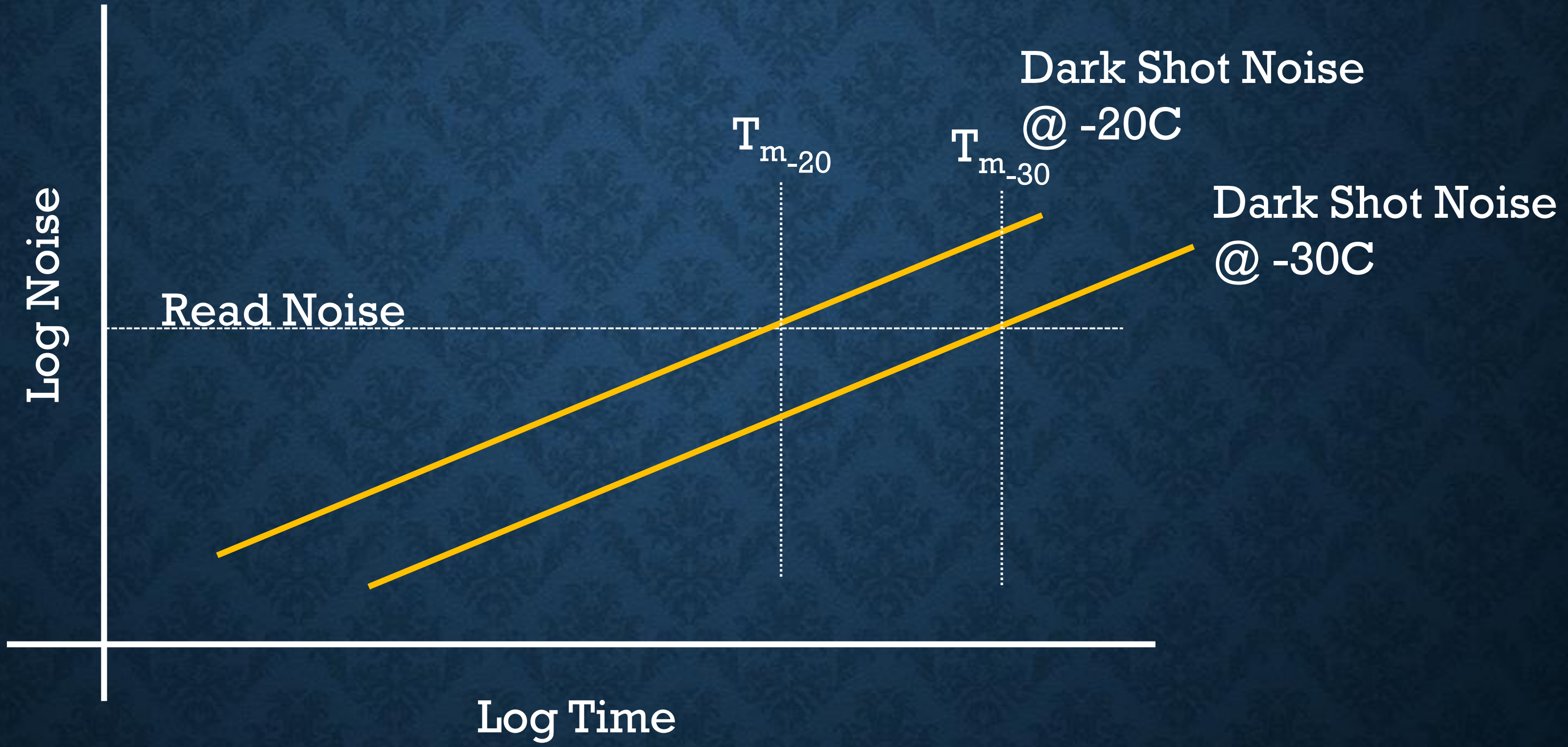
Affected Region (~ 1-2 mm)

Characterizing Sensor Charge Trapping

TRAP CHARACTERIZATION

- Determine Trap Capacity
- Determine dark shot noise vs time for different temperatures with and without light flood mitigation
- Determine maximum practical exposure time (vs temperature) with and without Light Flood Mitigation

IMPORTANT METRIC: MAXIMUM PRACTICAL EXPOSURE LIMIT



__Exposure limit: Dark Shot Noise > Read noise__

Trapped Charge PTC Investigation Methodology

Use Photon Transfer Methods (my Friday night workshop)

- Use PTC characterization data for Read Noise and Camera Gain measurement
- Measure Dark Shot Noise versus Time
- Two major cases: with and without light flood
- Examine at -15, -20, -25, -30, -35 & -40C operating temperature

$$Total\_noise = \sqrt{Read\_noise^2 + Dark\_shot\_noise^2} \tag{1}$$

$$Dark\_shot\_noise = \sqrt{Total\_noise^2 - Read\_noise^2} \tag{2}$$

$$Dark\_shot\_noise = \sqrt{Total\_dark\_signal} \tag{3}$$

$$Total\_dark\_signal = Thermal\_dark\_signal + Trap\_leakage \tag{4}$$

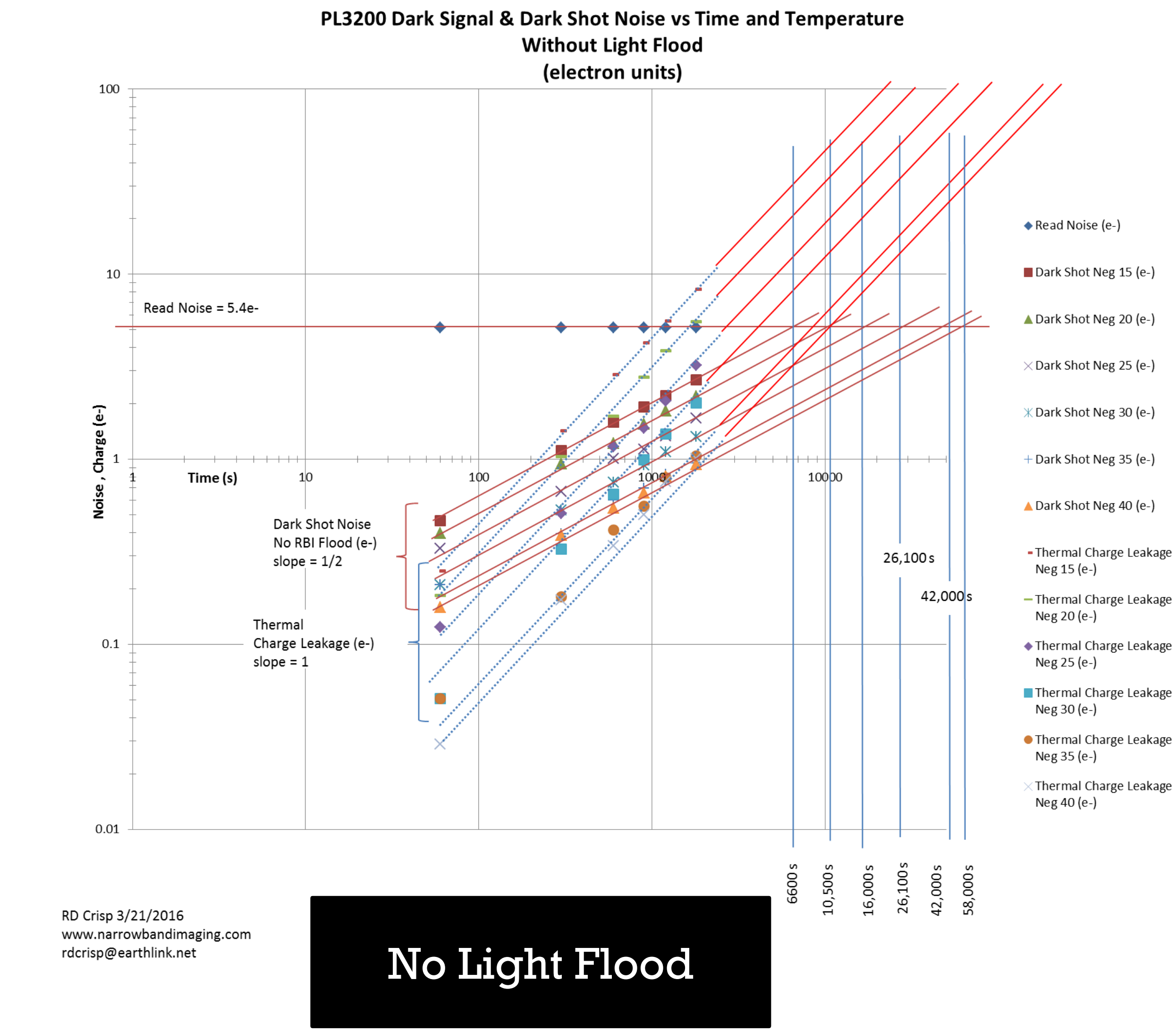
For no-light flood case, Trap_leakage is zero:

$$Total\_dark\_signal = Thermal\_dark\_signal \tag{5}$$

ESTABLISHING A BASELINE: DATA COLLECTION PROCEDURE

- **Collect non light-flood dark data**
  - Start camera from power-off regime with sensor at room temperature
  - Leave cooler off: wait 5 minutes, then take 100 bias frames and discard
  - Enable cooler: let temperature stabilize
  - Collect pairs of identical darks: two each of bias and various timed dark frames (60s, 300s, 600s, 900s, 1200s, 1800s) without using Light Flood
  - Reduce sensor temperature and let stabilize (data collected at -15C to -40C in 5C steps
  - Repeat the collection of pairs of darks

Noise Baseline Case: No Light Flood/No Trap Leakage



PL3200 Dark Signal & Dark Shot Noise vs Time and Temperature
Without Light Flood
(electron units)

RD Crisp 3/21/2016
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No Light Flood

LIGHT FLOOD CASE:
DATA COLLECTION PROCEDURE

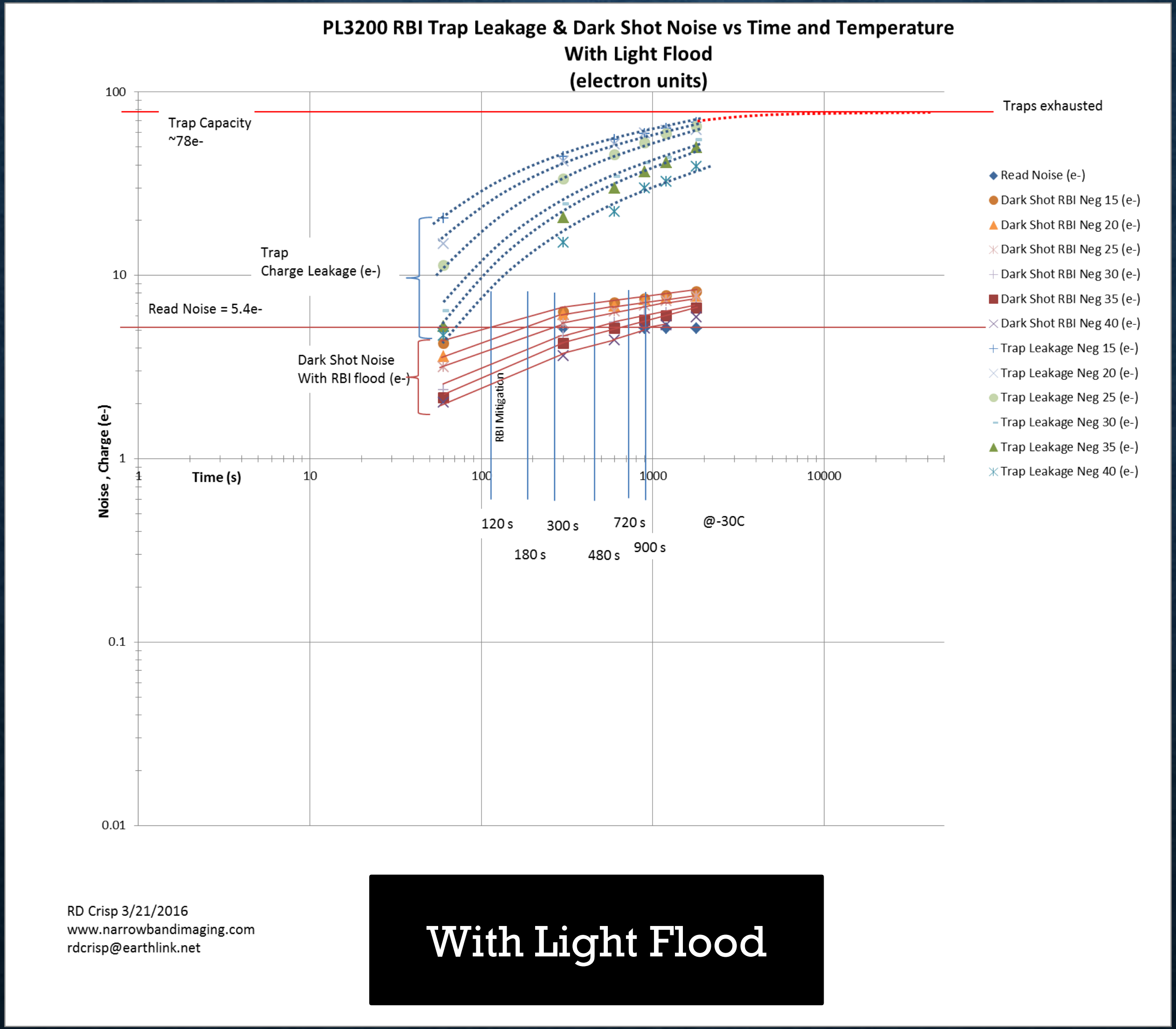
- **Collect Light-flood dark data**
  - Start camera from power-off regime with sensor at room temperature
  - Enable cooler: let sensor temperature stabilize at target
  - Collect set of pairs of darks: two each of bias and various timed dark frames (60s, 300s, 600s, 900s, 1200s, 1800s) **using Light Flood**
  - Reduce sensor temperature and let stabilize (data collected at -15C to -40C in 5C steps
  - Repeat the collection of pairs of darks

Calculating Trap Leakage

To determine the trap leakage you use the thermal dark signal data from the non light-flooded case and the Total Noise from the light-flooded case

$$Trap\_leakage = Total\_noise^2 - Read\_noise^2 - Thermal\_dark\_signal \qquad (6)$$

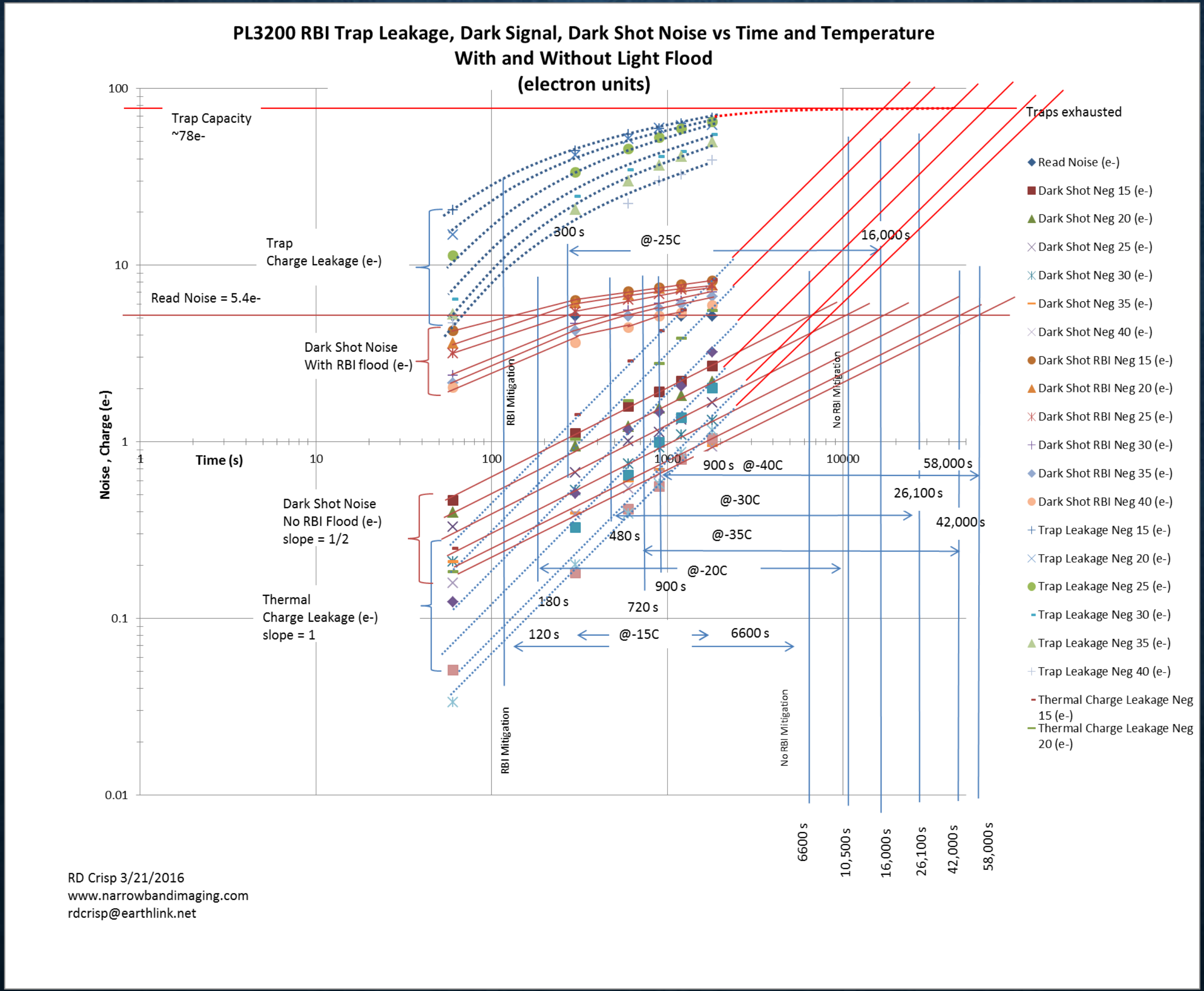
Noise With Filled Traps: Light Flood Case



With Light Flood

-40C: good for 15 minutes
-25C: good for 5 minutes

Noise: With and Without Light Flood



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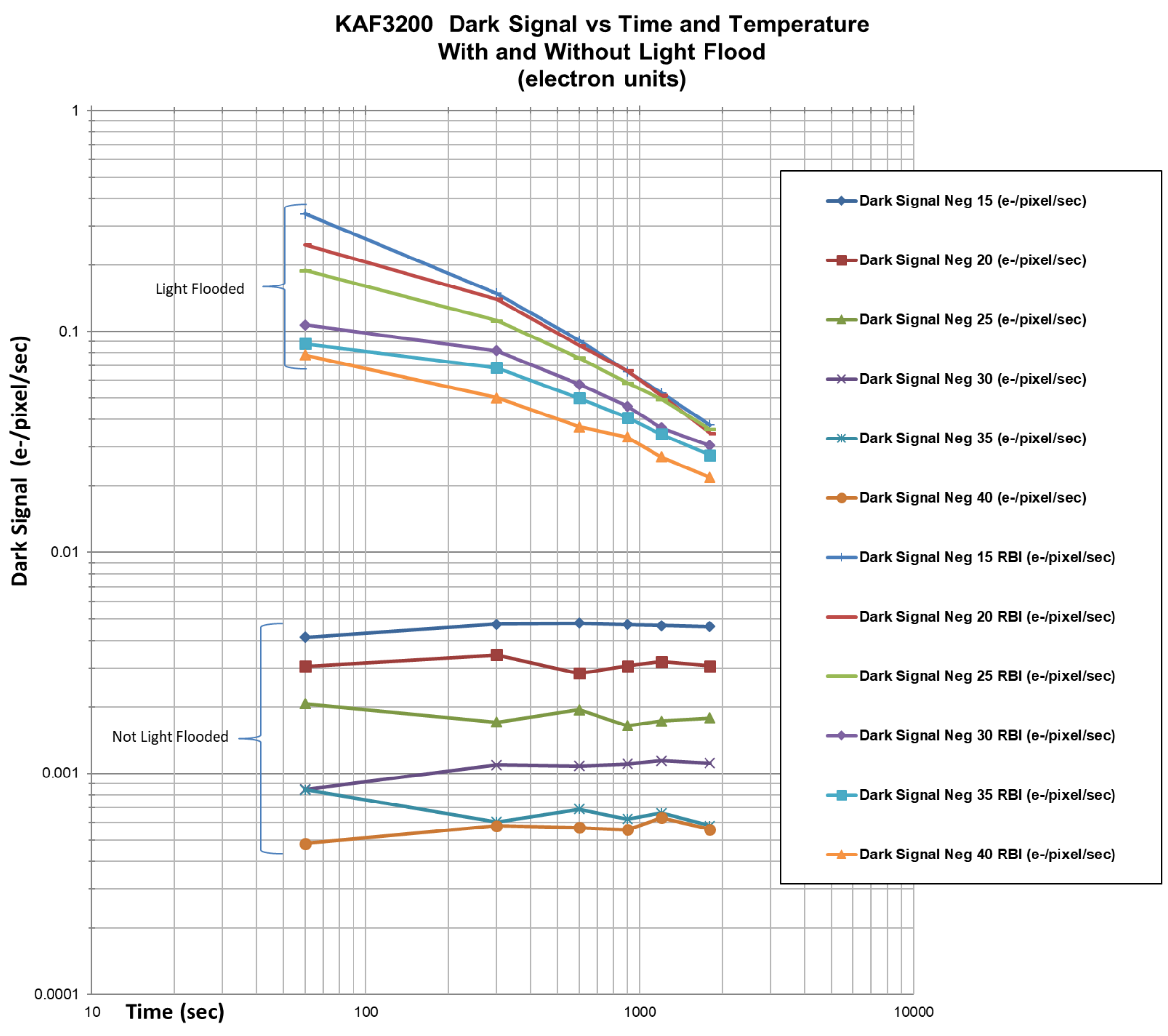
Dark Signal With and Without Light Flood



SUMMARY OF RESULTS (FLI PROLINE 3200)

Operating Temperature (Celsius)	Max Practical Exposure* W/O RBI Mitigation (seconds)	Max Practical Exposure with RBI Mitigation (seconds)
-15	6,600	120
-20	10,500	180
-25	16,000	300
-30	26,100	480
-35	42,000	720
-40	58,000	900

Read Noise = 5.4 e-

Kadc = 0.8668 e-/DN

*Maximum Practical Exposure Time
Defined as that exposure time when the Dark Shot noise matches the Read Noise

Conclusions

Light Flood Method is effective at mitigating residual image

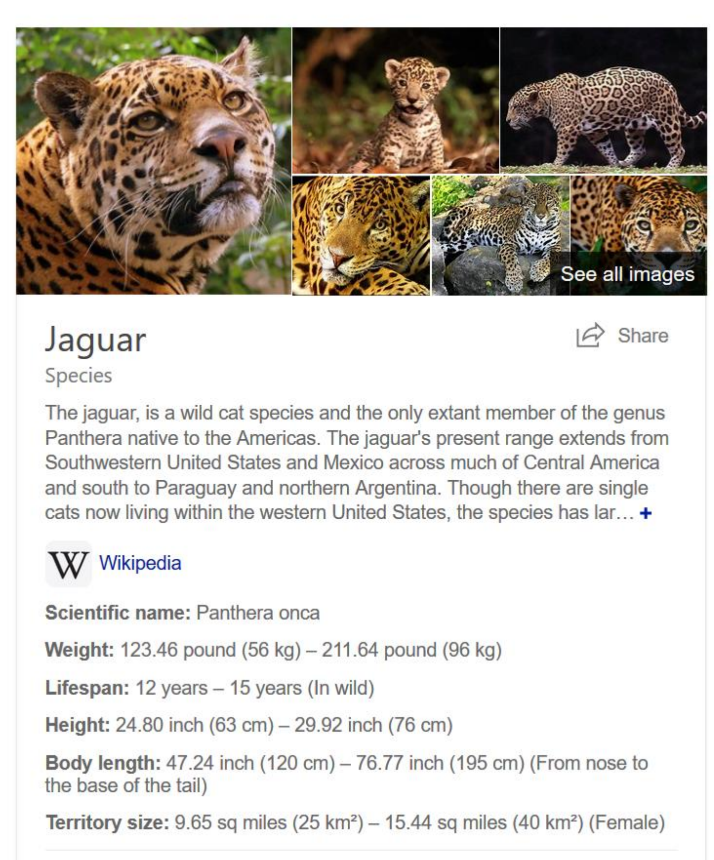
- Eliminates residual image
- Removes Dark Fixed Patterns from non-uniform trap distribution
- Avoids bad effects from Amplifier Luminescence
- Can reduce effects of radiation hits

Photon Transfer Methods can be used to characterize trap capacity and leakage characteristics

- Trap leakage
- Trap capacity
- Maximum practical exposure time vs Temperature behavior

CMOS IMAGE SENSOR:
MAJOR PERFORMANCE DIFFERENCES VS CCD

CCD VS CMOS:
JAGUAR VS LEOPARD



Jaguar

Species

The jaguar, is a wild cat species and the only extant member of the genus Panthera native to the Americas. The jaguar's present range extends from Southwestern United States and Mexico across much of Central America and south to Paraguay and northern Argentina. Though there are single cats now living within the western United States, the species has lar… +

Wikipedia

Scientific name: Panthera onca

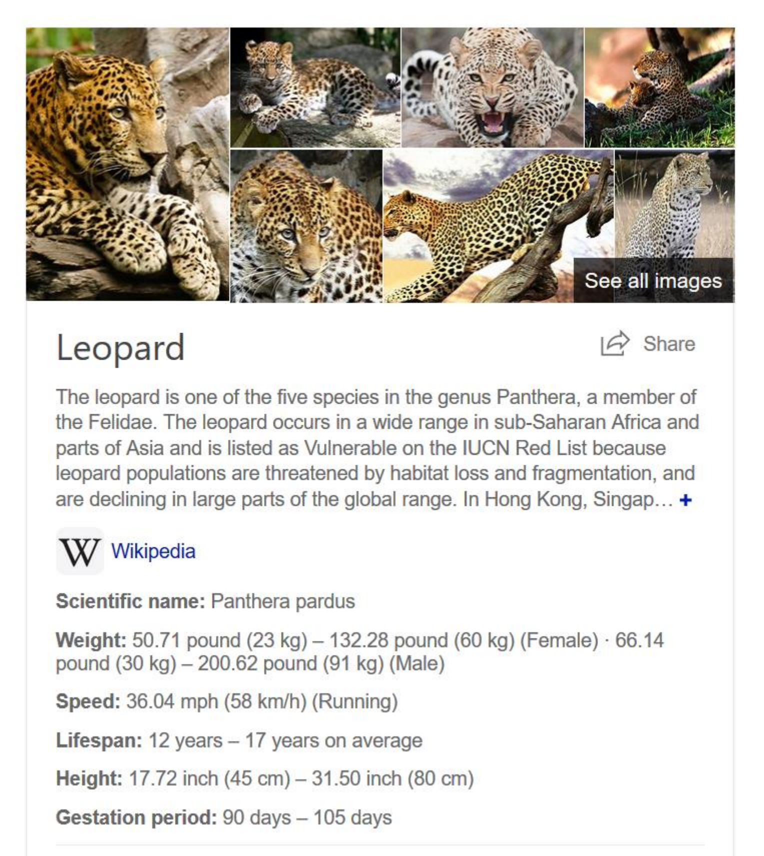
Weight: 123.46 pound (56 kg) – 211.64 pound (96 kg)

Lifespan: 12 years – 15 years (In wild)

Height: 24.80 inch (63 cm) – 29.92 inch (76 cm)

Body length: 47.24 inch (120 cm) – 76.77 inch (195 cm) (From nose to the base of the tail)

Territory size: 9.65 sq miles (25 km²) – 15.44 sq miles (40 km²) (Female)



Leopard

The leopard is one of the five species in the genus Panthera, a member of the Felidae. The leopard occurs in a wide range in sub-Saharan Africa and parts of Asia and is listed as Vulnerable on the IUCN Red List because leopard populations are threatened by habitat loss and fragmentation, and are declining in large parts of the global range. In Hong Kong, Singap… +

Wikipedia

Scientific name: Panthera pardus

Weight: 50.71 pound (23 kg) – 132.28 pound (60 kg) (Female) · 66.14 pound (30 kg) – 200.62 pound (91 kg) (Male)

Speed: 36.04 mph (58 km/h) (Running)

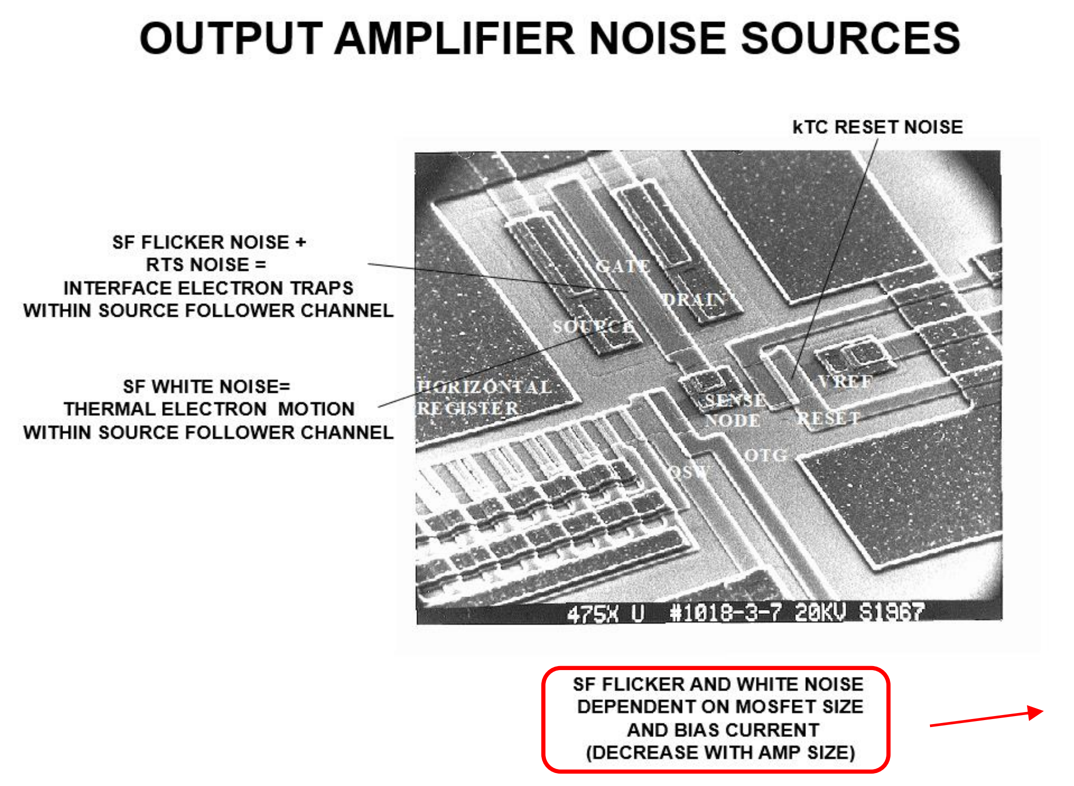
Lifespan: 12 years – 17 years on average

Height: 17.72 inch (45 cm) – 31.50 inch (80 cm)

Gestation period: 90 days – 105 days

“similar but different”

CMOS: OFTEN LOWER READ NOISE THAN CCD



OUTPUT AMPLIFIER NOISE SOURCES

kTC RESET NOISE

SF FLICKER NOISE + RTS NOISE = INTERFACE ELECTRON TRAPS WITHIN SOURCE FOLLOWER CHANNEL

SF WHITE NOISE= THERMAL ELECTRON MOTION WITHIN SOURCE FOLLOWER CHANNEL

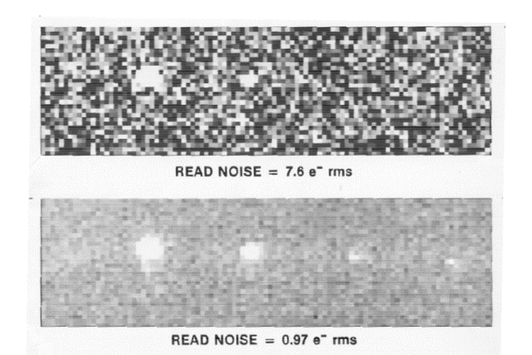
SF FLICKER AND WHITE NOISE DEPENDENT ON MOSFET SIZE AND BIAS CURRENT (DECREASE WITH AMP SIZE)

Source follower for CCD drives the off-chip load: **needs a big transistor**

Trapping sites under large area gate electrode of source follower determine 1/F noise for CCD S-F. Large geometry transistor has many sites: behave as continuum of trapping-detrapping

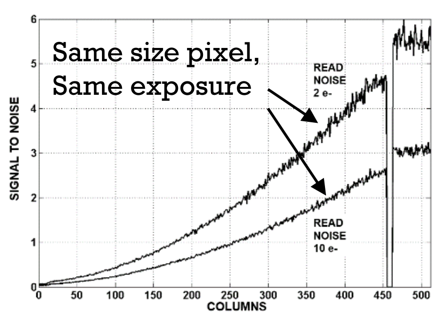
Source follower for CMOS is in each pixel and drives small on-chip load: **uses tiny transistor**

For CMOS, tiny S-F transistor has only small # trapping sites: lower noise & looks like discrete events (called RTS: Random Telegraph Signal)

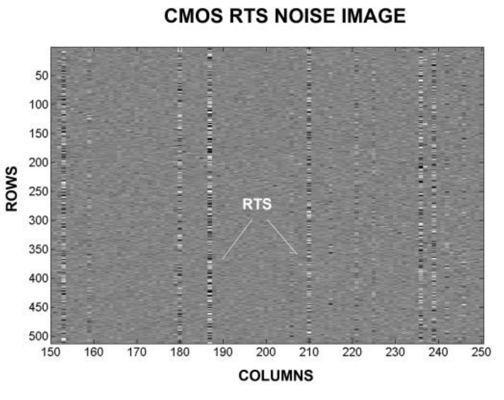


READ NOISE = 7.6 e⁻ rms

READ NOISE = 0.97 e⁻ rms

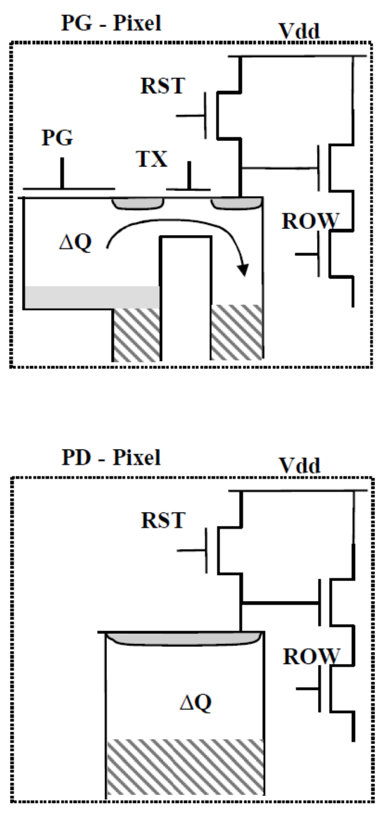


Same size pixel, Same exposure



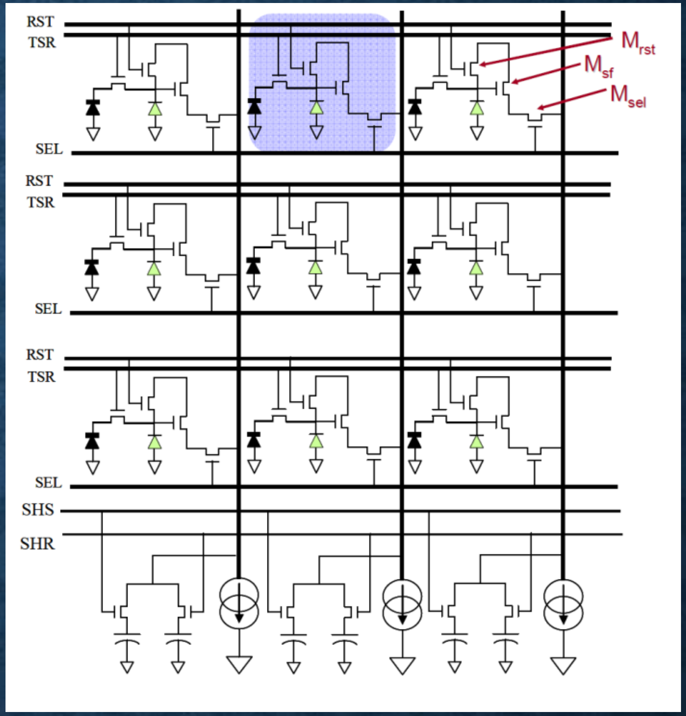
CMOS RTS NOISE IMAGE

COMMON CMOS PIXEL ARCHITECTURES



4 Transistor
DCDS possible
(noise compensation)
Image Lag
Lower fill factor

3 Transistor
No DCDS
No Image Lag
Higher fill factor



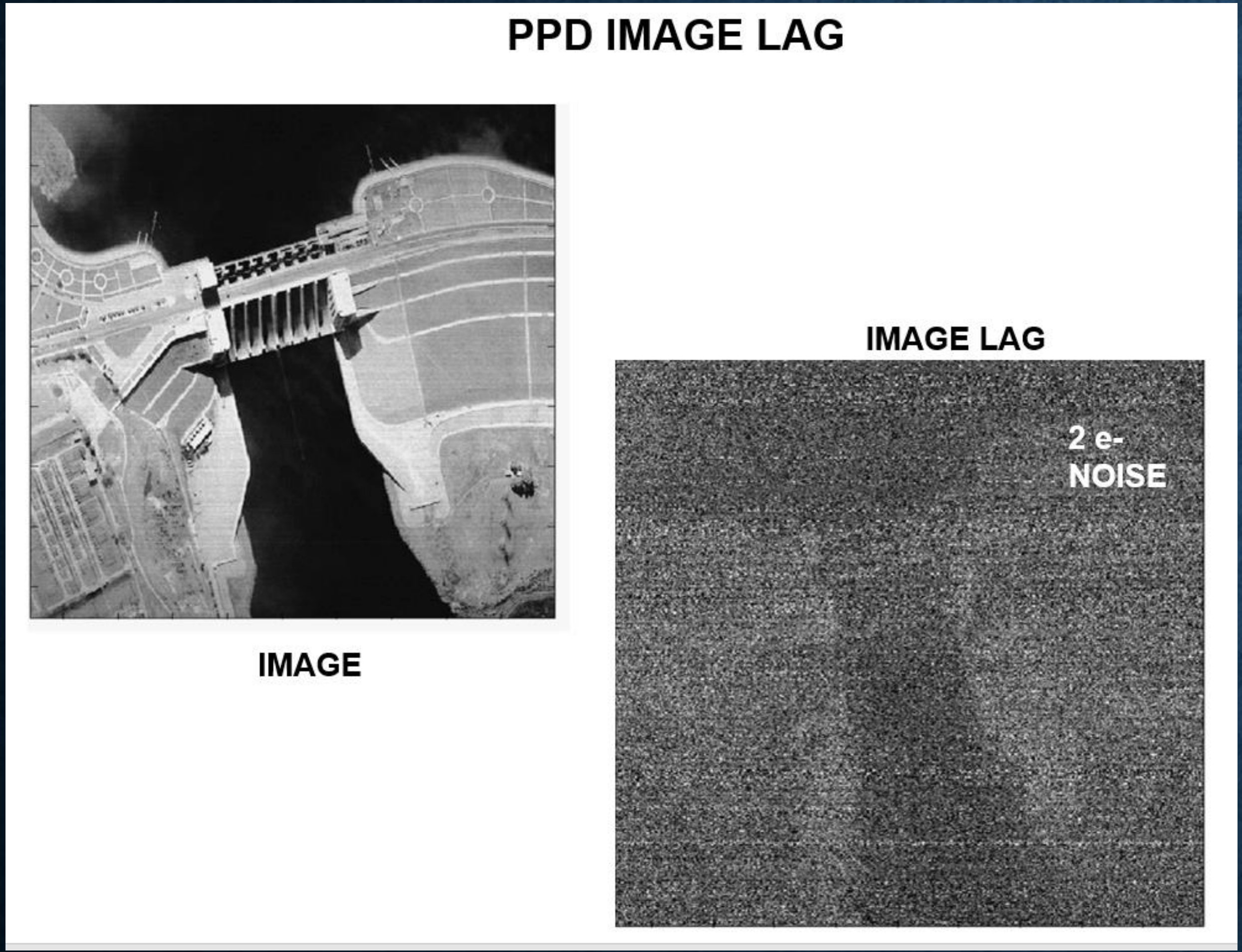
On Chip Binning not feasible with this array design

Amplifier / ADC per column is possible
Can get very fast frame readout rates vs CCD, ie > 1000 frames/sec
Can you store that much data?
(**16Mpix * 1000 f/s** = 16Gigapixels/sec * 16bits/pix = **32Gbytes/sec**)

How many pins do you want and how much power is OK?

Many other architectures / features possible
Depending on pixel/array design
(global snap shutter, A/D per pixel for HDR etc)

CMOS IMAGE LAG (NOT RBI!)



PPD IMAGE LAG

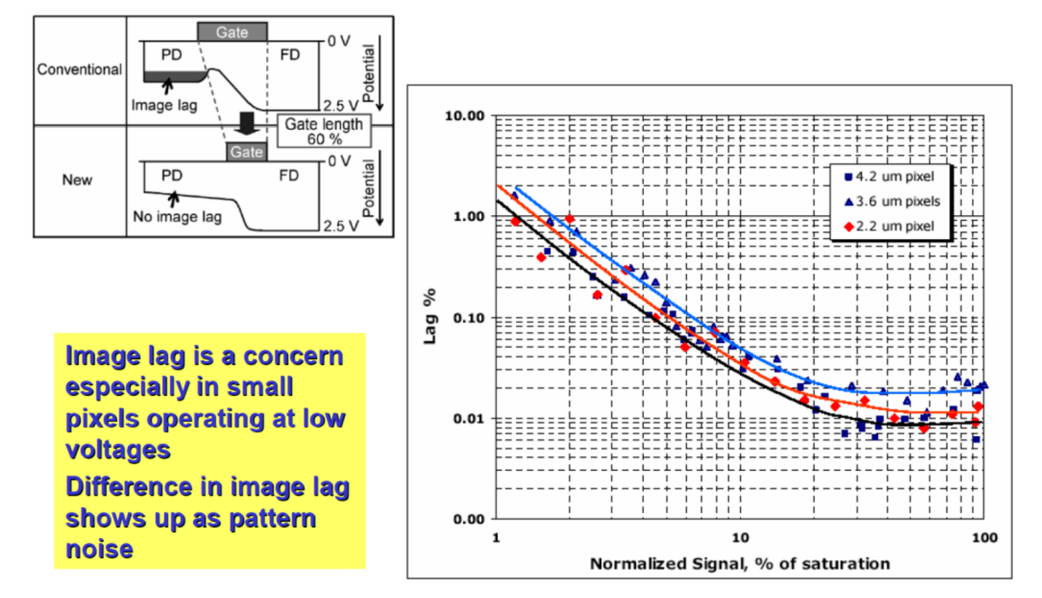
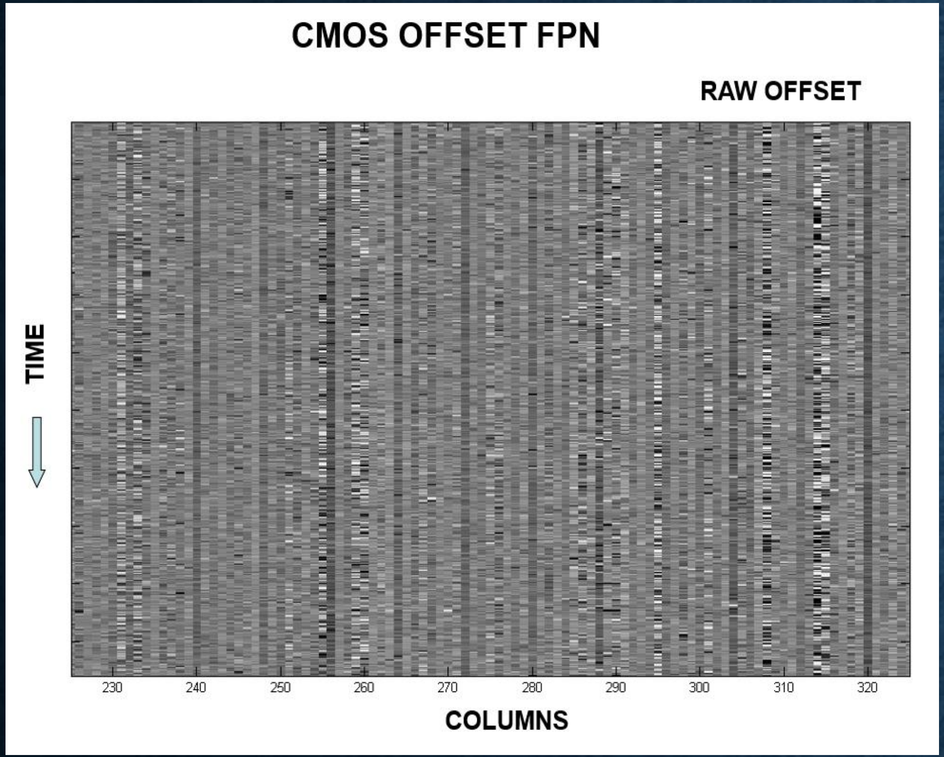


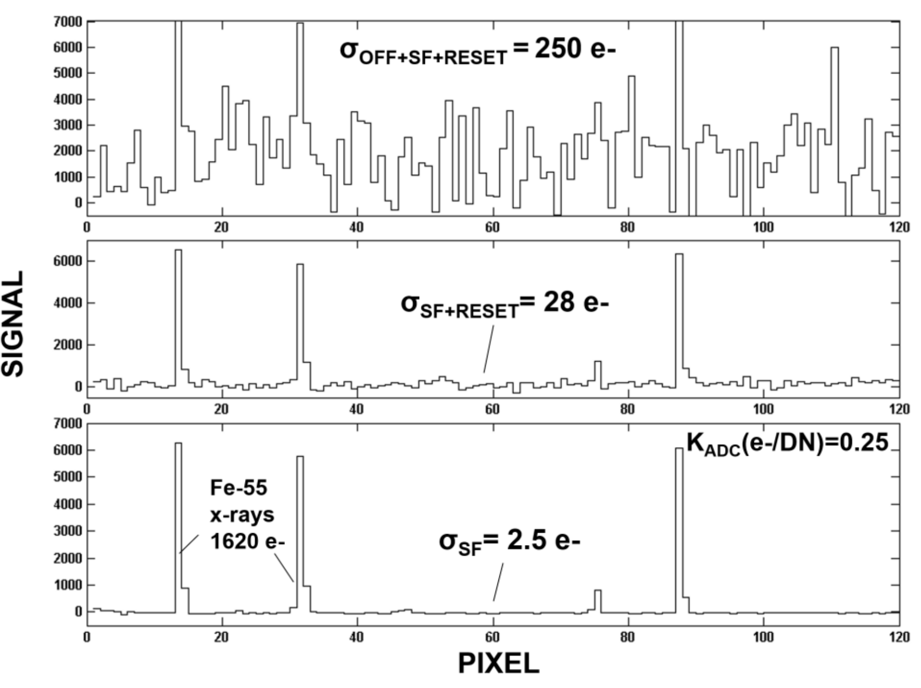
Image lag is a concern especially in small pixels operating at low voltages

Difference in image lag shows up as pattern noise

Reminds you of RBI but is different mechanism

CMOS OFFSET & RESET FPN



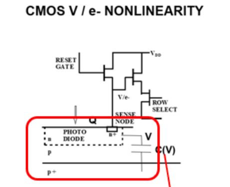


For many CMOS sensors, each pixel in a has its own amplifier
The offset value of each pixel amplifier is a little different resulting in pixel to pixel offset FPN.

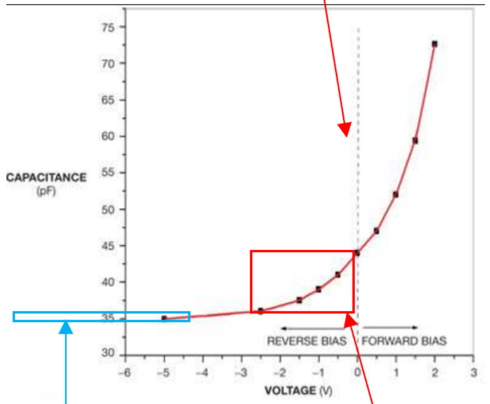
This can be removed on-chip depending on IC architecture
(DCDS, digital correlated double sampling)

CCD usually has 1 to 4 amplifiers only

CMOS: V/E NON-LINEARITY & FLAT FIELDING

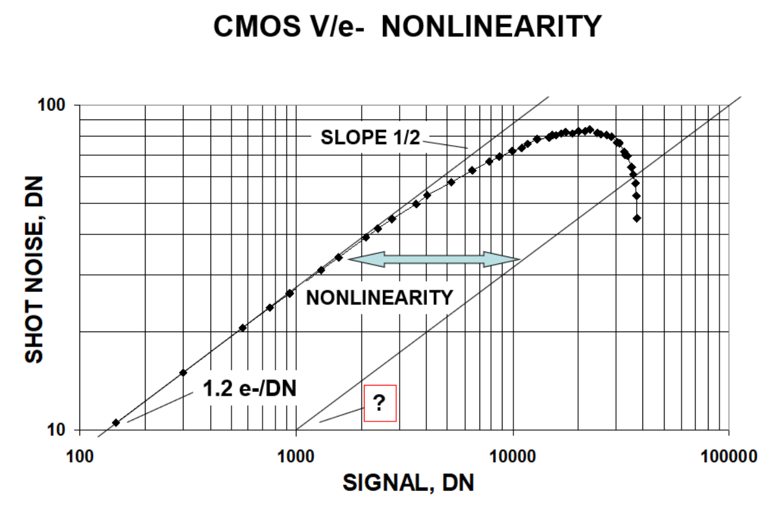


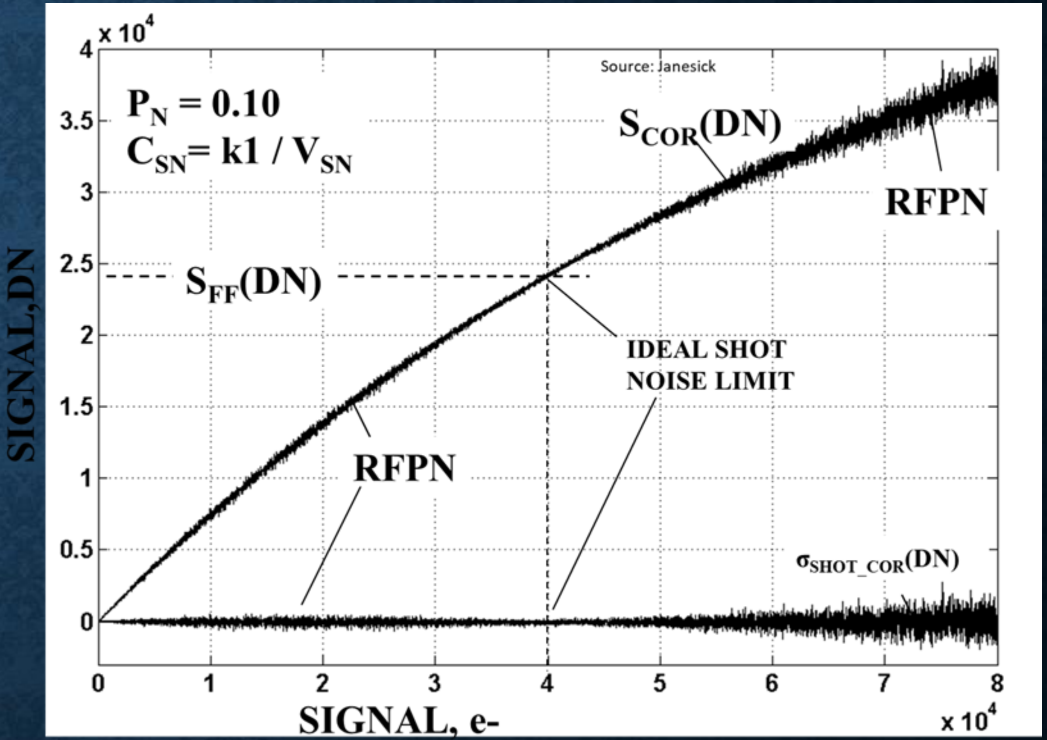
Reverse biased diode Capacitance vs Voltage (like sense node floating diffusion)



Typical CCD sense node voltage swings

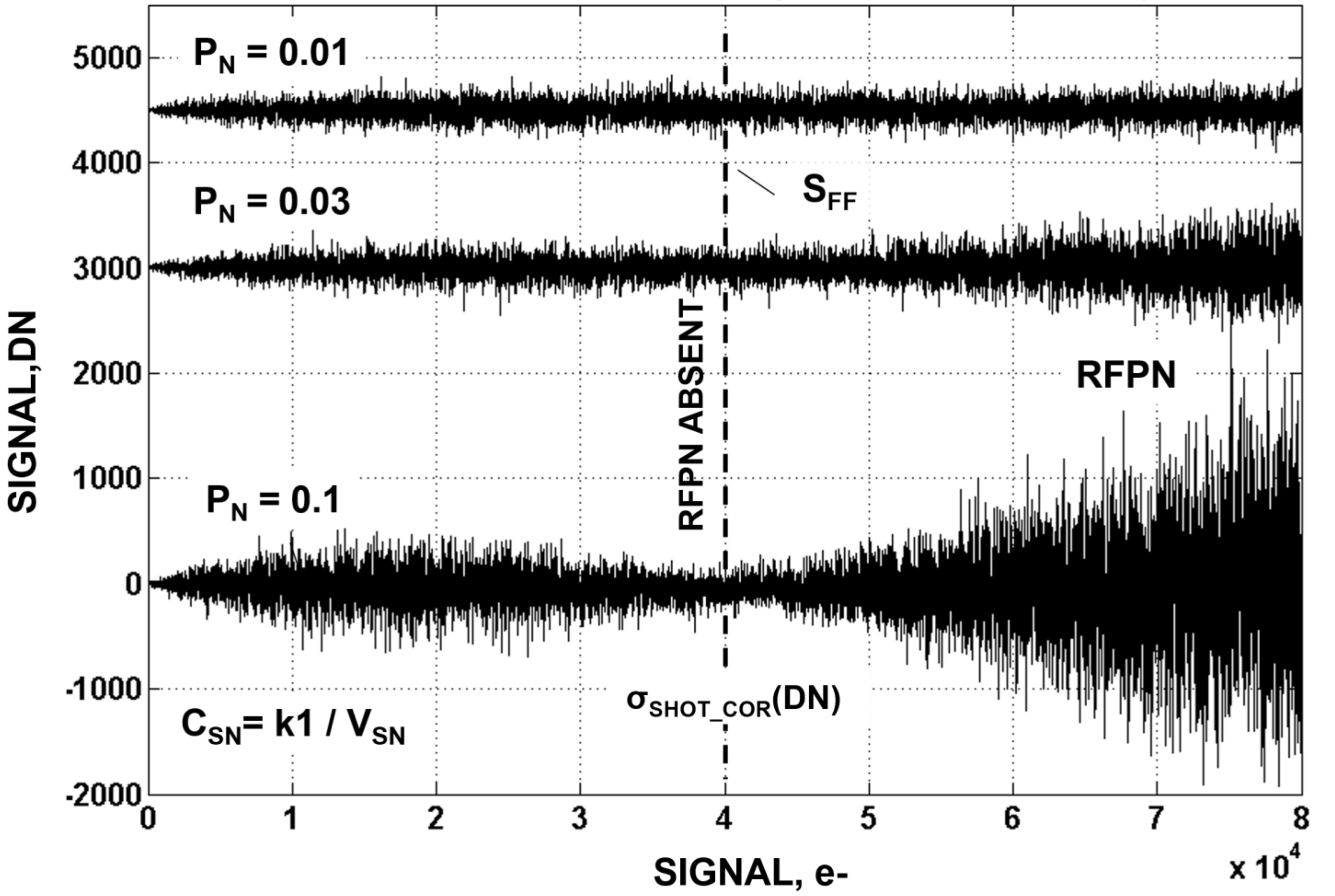
Typical CMOS sense node voltage swings





Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: REMNANT FPN



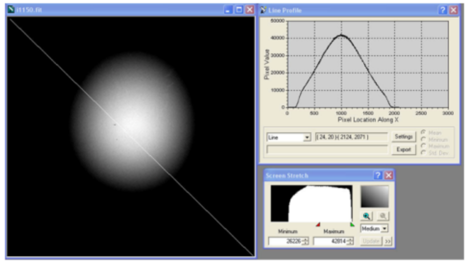
1%

IF PRNU is 1% or less flat fielding is effective in presence of V/e-nonlinearity

3%

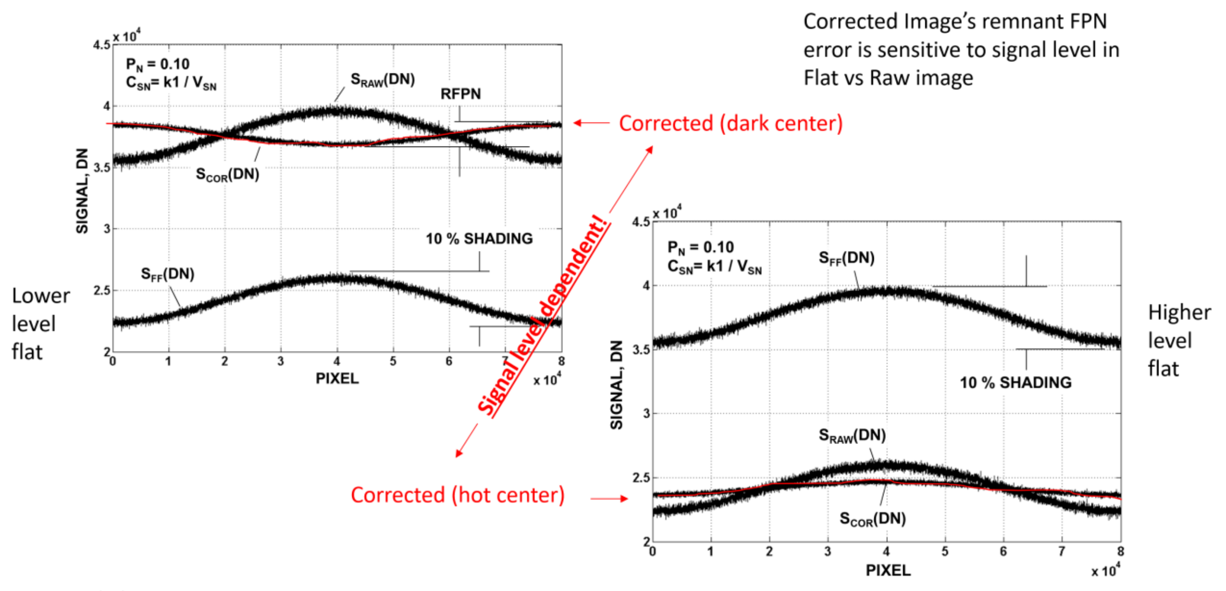
For larger values of PRNU (ie lens cos^4 rolloff), flat fielding may not be 100% effective

10%



Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: FLAT/SIGNAL DEPENDENT REMNANT FPN



Corrected Image's remnant FPN error is sensitive to signal level in Flat vs Raw image

Corrected (dark center)

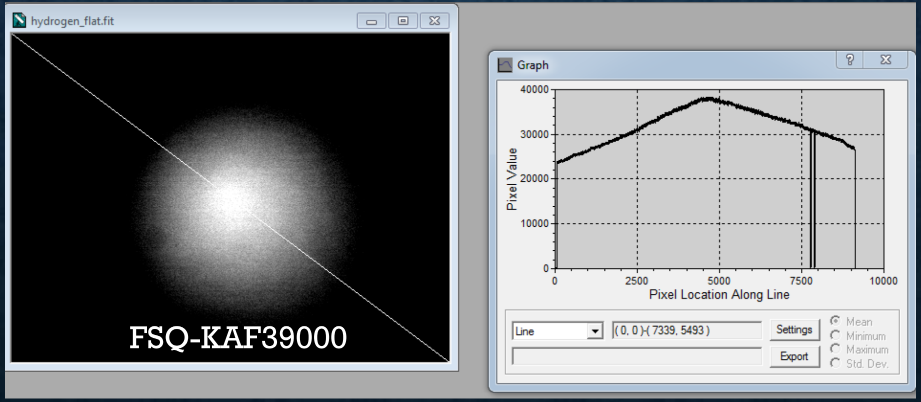
Signal level dependent!

Corrected (hot center)

Lower level flat

Higher level flat

Imperfect flat fielding is the net result



Line

(0, 0)-(7339, 5493)

● Mean
○ Minimum
○ Maximum
○ Std. Dev.

>10% Lens shading/rolloff is not unusual for wide FOV – big sensor combo

SUMMARY

CMOS often has lower read noise than CCD

- Source follower noise is lower because transistor geometry is smaller
- Lower noise with equal QE results in less time to given SNR target

CMOS Sensors can be read at very high speed

- One or two Amplifiers & A/D per column is feasible for ultra fast frame rates (> 1000 frames/sec)
- Very difficult to store the high bandwidth data (32GByte/sec = 1000 frames sec of a 16 megapixel sensor with 16 bits/pixel)

Some CMOS pixel architectures suffer from image lag

- Reminds you of RBI but is a different mechanism
- Can be especially bad in high frame rate video applications

CMOS noise sources behave differently than CCD

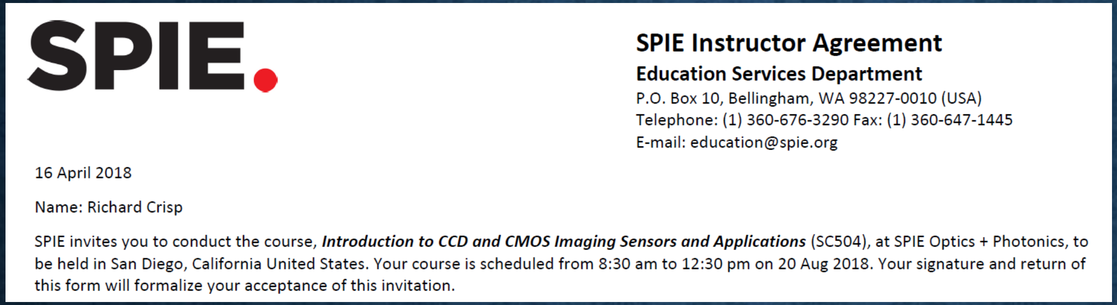
- Each pixel has its own amplifier with its own offset and noise characteristics
  - Reset Noise
  - Offset FPN
    - Reset and Offset FPN can be corrected on-chip, depending on architecture
- RTS noise (ultimate noise floor)

CMOS nonlinearities can be more severe than CCD

- V/e- more severe vs CCD and that causes FPN to not be fully removed by flat fielding
- Can cause visible artifacts with as little as 10% lens intensity rolloff & high signal levels

HALF DAY CLASSES
ATTEND SPIE OPTICS & PHOTONICS
SAN DIEGO: AUG 19-23, 2018

CCD & CMOS
Half day class



SPIE Instructor Agreement
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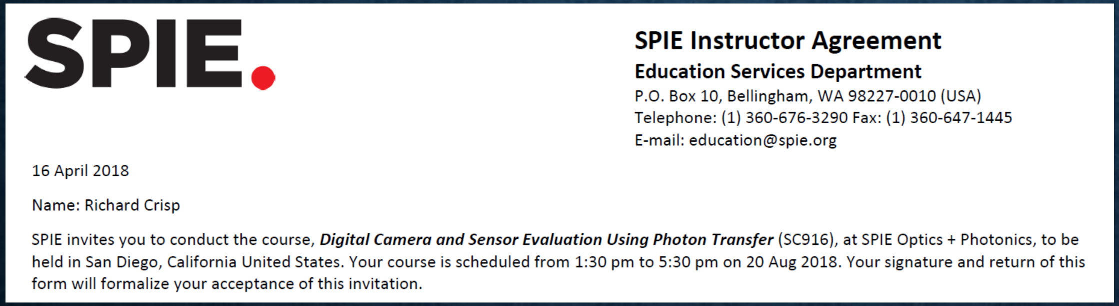
E-mail: education@spie.org

16 April 2018

Name: Richard Crisp

SPIE invites you to conduct the course, ***Introduction to CCD and CMOS Imaging Sensors and Applications*** (SC504), at SPIE Optics + Photonics, to be held in San Diego, California United States. Your course is scheduled from 8:30 am to 12:30 pm on 20 Aug 2018. Your signature and return of this form will formalize your acceptance of this invitation.

Photon Transfer
Half day class



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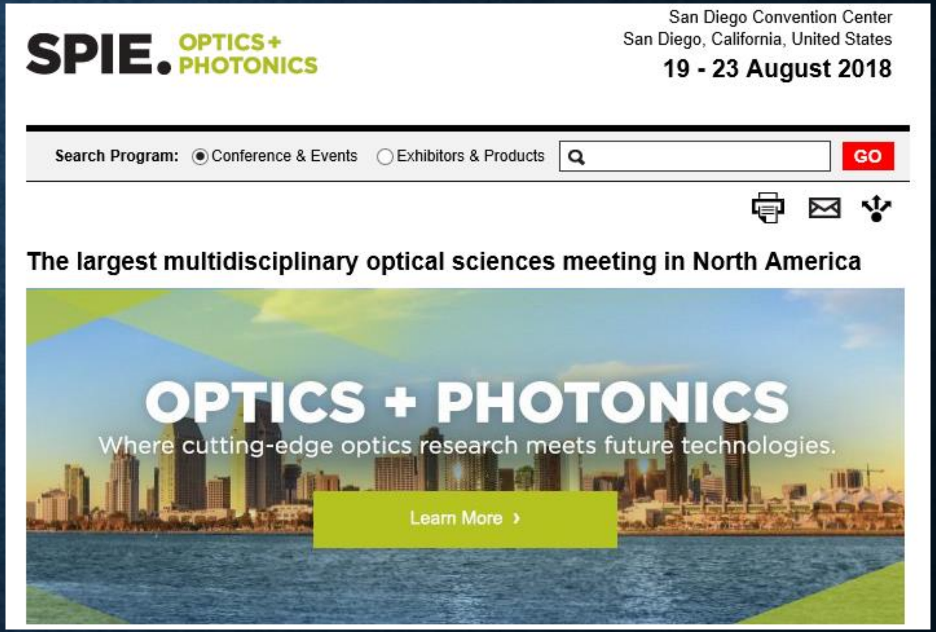
16 April 2018

Name: Richard Crisp

SPIE invites you to conduct the course, ***Digital Camera and Sensor Evaluation Using Photon Transfer*** (SC916), at SPIE Optics + Photonics, to be held in San Diego, California United States. Your course is scheduled from 1:30 pm to 5:30 pm on 20 Aug 2018. Your signature and return of this form will formalize your acceptance of this invitation.



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