Image Lag in CMOS

Crisp

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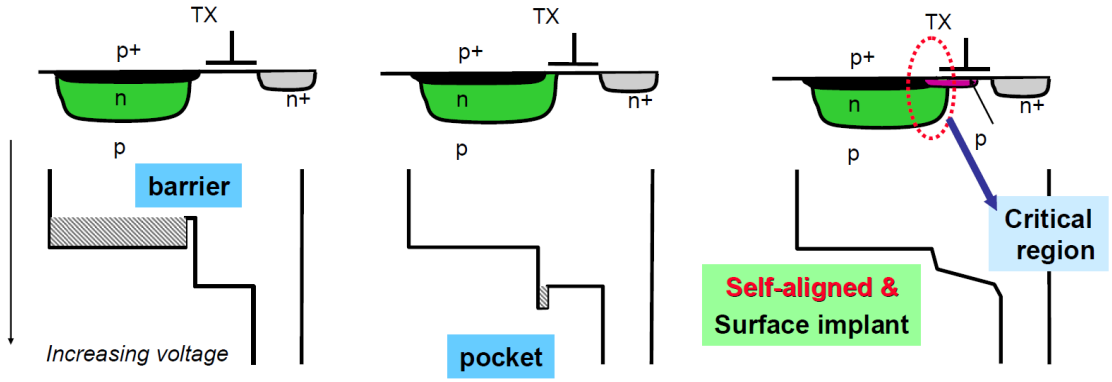
DIFFICULTIES IN PPD PIXEL



- Low voltage is a big problem – transfer, pinning, and depletion width compromised
- Surface p^+ must be deep enough to fully passivate surface traps
- TX is a strange FET – what V_T to use? Surface FET ok?
- Electric field between TX and p^+ needs to be reduced (to prevent GIDL)
- Floating diffusion doping needs to be tailored to prevent pockets in the FD side
- Horizontal drift field needed to prevent back-flow
- **Excellent process control**

IMAGE LAG

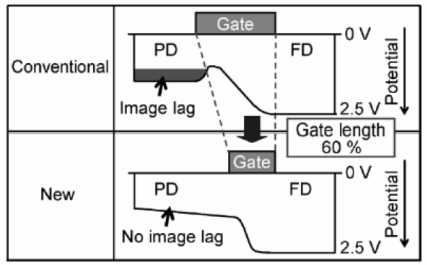
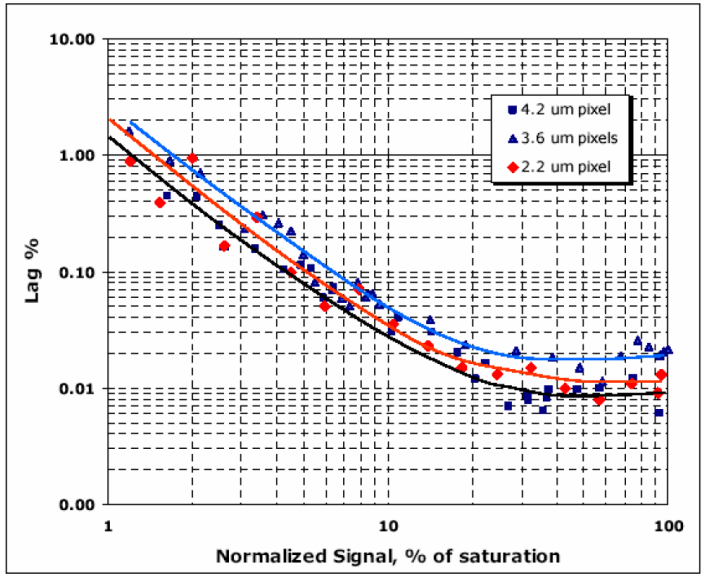
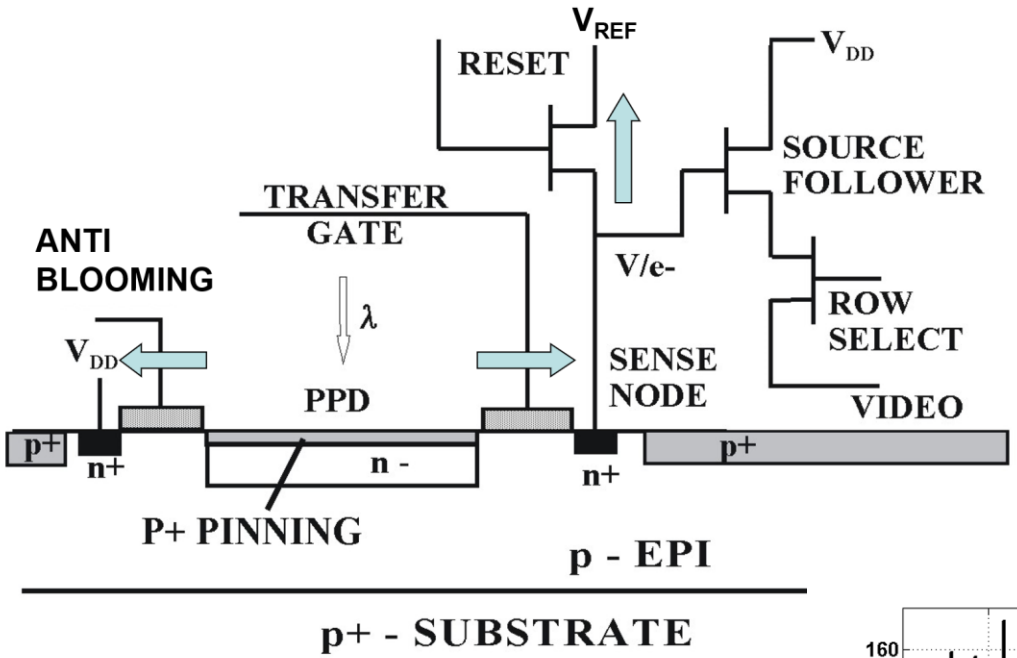


Image lag is a concern especially in small pixels operating at low voltages

Difference in image lag shows up as pattern noise



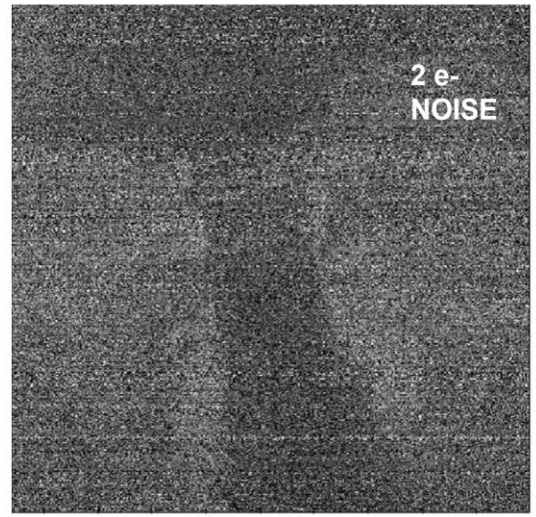
5 T PPD CHARGE TRANSFER



PPD IMAGE LAG

IMAGE

IMAGE LAG



CMOS IMAGE LAG