


CMOS IMAGE SENSORS

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CMOS IMAGE SENSOR: MAJOR PERFORMANCE DIFFERENCES VS CCD

CCD VS CMOS: JAGUAR VS LEOPARD



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Jaguar

Species [Share](#)

The jaguar, is a wild cat species and the only extant member of the genus Panthera native to the Americas. The jaguar's present range extends from Southwestern United States and Mexico across much of Central America and south to Paraguay and northern Argentina. Though there are single cats now living within the western United States, the species has lar... [+](#)

[W](#) [Wikipedia](#)

Scientific name: Panthera onca


Weight: 123.46 pound (56 kg) – 211.64 pound (96 kg)

Lifespan: 12 years – 15 years (In wild)

Height: 24.80 inch (63 cm) – 29.92 inch (76 cm)

Body length: 47.24 inch (120 cm) – 76.77 inch (195 cm) (From nose to the base of the tail)

Territory size: 9.65 sq miles (25 km²) – 15.44 sq miles (40 km²) (Female)



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Leopard

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The leopard is one of the five species in the genus Panthera, a member of the Felidae. The leopard occurs in a wide range in sub-Saharan Africa and parts of Asia and is listed as Vulnerable on the IUCN Red List because leopard populations are threatened by habitat loss and fragmentation, and are declining in large parts of the global range. In Hong Kong, Singap... [+](#)

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Scientific name: Panthera pardus

Weight: 50.71 pound (23 kg) – 132.28 pound (60 kg) (Female) · 66.14 pound (30 kg) – 200.62 pound (91 kg) (Male)

Speed: 36.04 mph (58 km/h) (Running)

Lifespan: 12 years – 17 years on average

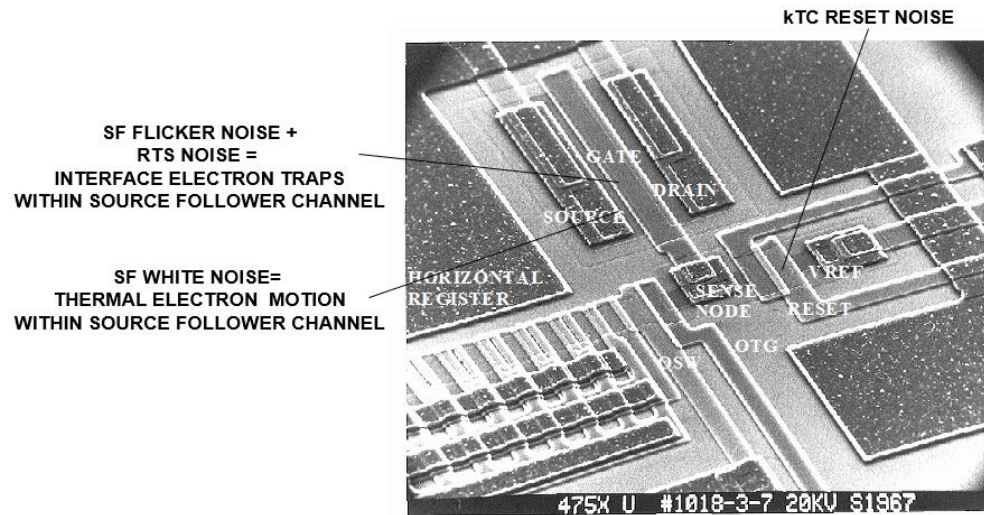
Height: 17.72 inch (45 cm) – 31.50 inch (80 cm)

Gestation period: 90 days – 105 days

“similar but different”

CMOS: OFTEN LOWER READ NOISE THAN CCD

OUTPUT AMPLIFIER NOISE SOURCES



SF FLICKER AND WHITE NOISE DEPENDENT ON MOSFET SIZE AND BIAS CURRENT (DECREASE WITH AMP SIZE)

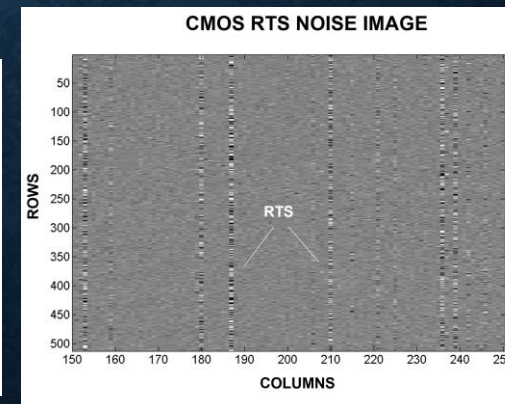
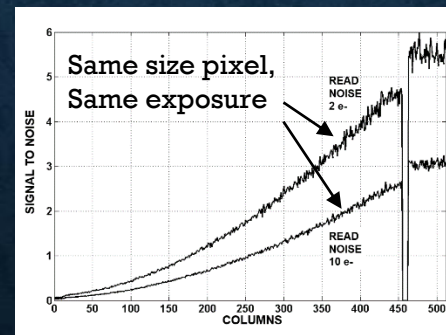
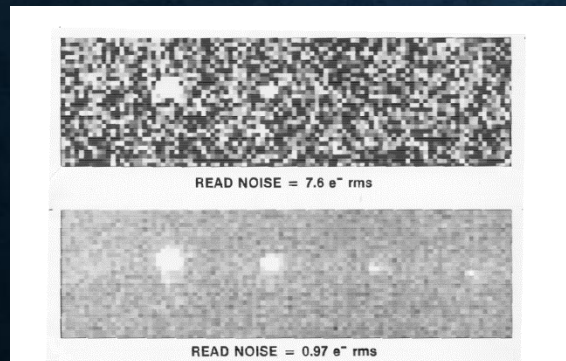
Source follower for CCD drives the off-chip load: needs a big transistor

Trapping sites under large area gate electrode of source follower determine $1/F$ noise for CCD S-F. Large geometry transistor has many sites: behave as continuum of trapping-detrapping

Source follower for CMOS is in each pixel and drives small on-chip load: uses tiny transistor

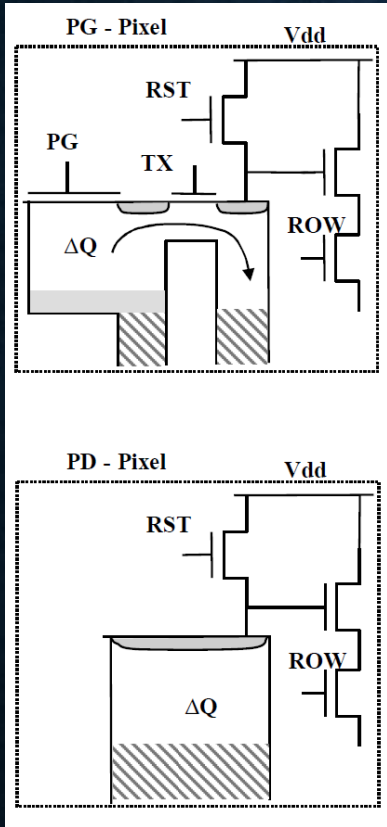
For CMOS, tiny S-F transistor has only small # trapping sites: lower noise & looks like discrete events (called RTS: Random Telegraph Signal)

ECAIC 2018 Crisp



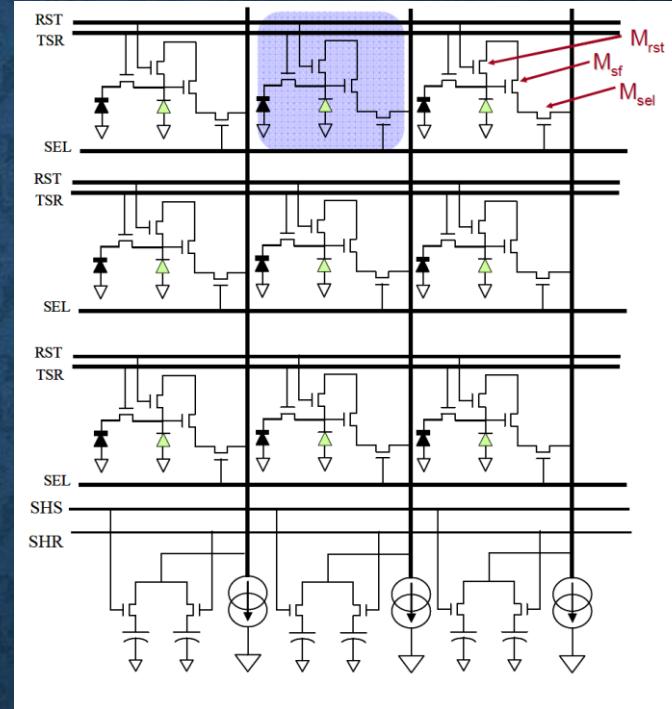
5/20/2019

COMMON CMOS PIXEL ARCHITECTURES



4 Transistor
DCDS possible
(noise compensation)
Image Lag
Lower fill factor

3 Transistor
No DCDS
No Image Lag
Higher fill factor



On Chip Binning not feasible
with this array design

Amplifier / ADC per
column is possible
Can get very fast
frame readout rates
vs CCD, ie > 1000
frames/sec
Can you store that
much data?
(16Mpix * 1000 f/s =
16Gigapixels/sec *
16bits/pix =
32Gbytes/sec)

**How many pins do
you want and how
much power is OK?**

Many other architectures / features possible
Depending on pixel/array design
(global snap shutter, A/D per pixel for HDR etc)

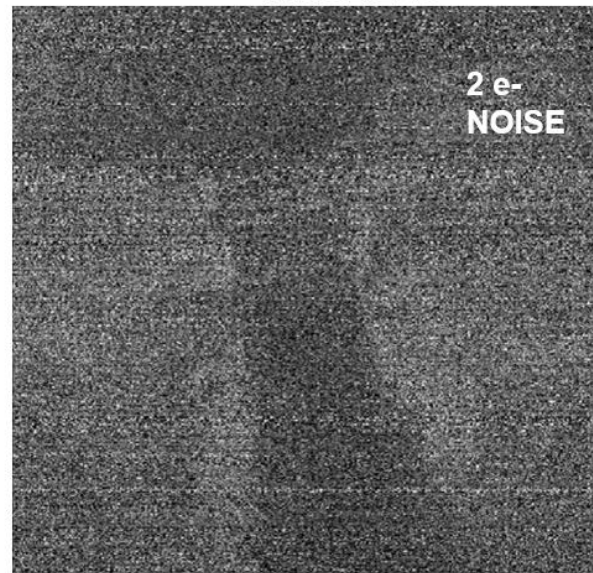
CMOS IMAGE LAG (NOT RBI!)

PPD IMAGE LAG



IMAGE

IMAGE LAG



2 e-
NOISE

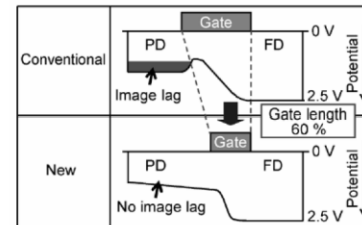
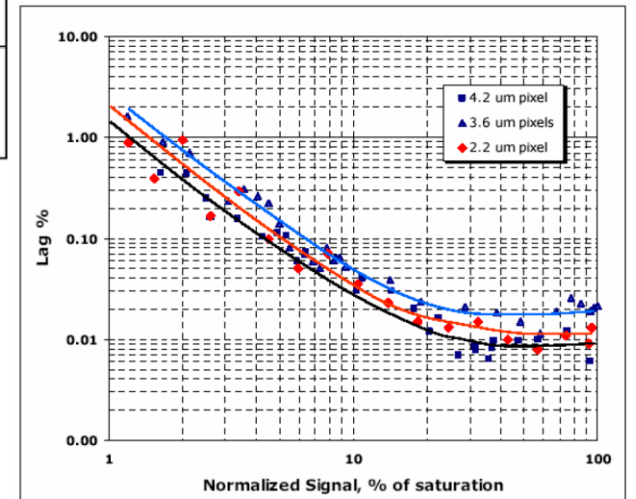
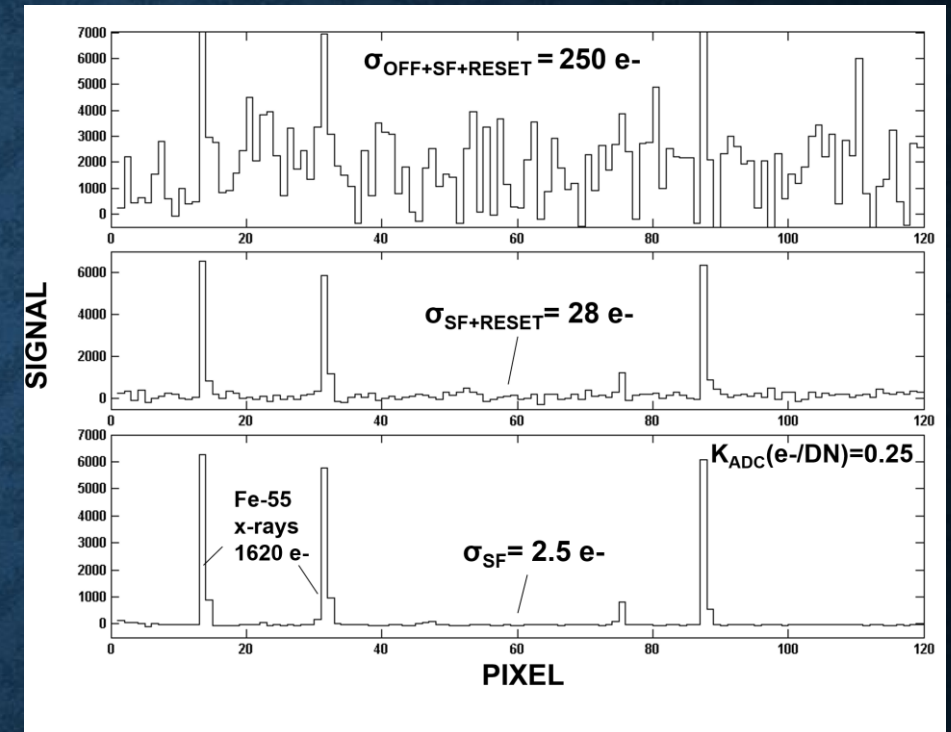
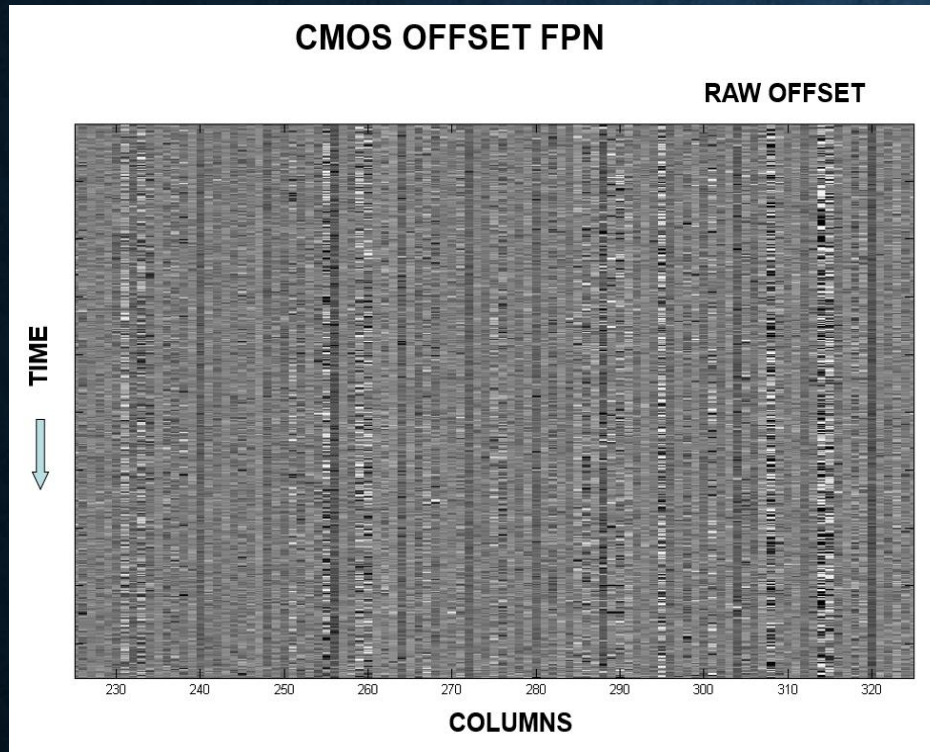


Image lag is a concern especially in small pixels operating at low voltages
Difference in image lag shows up as pattern noise



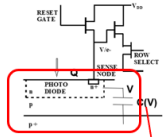
CMOS OFFSET & RESET FPN



For many CMOS sensors, each pixel in a has its own amplifier
The offset value of each pixel amplifier is a little different resulting in pixel to pixel offset FPN.

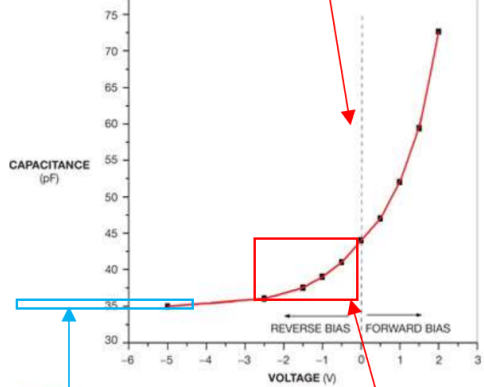
This can be removed on-chip depending on IC architecture
(DCDS, digital correlated double sampling)

CCD usually has 1 to 4 amplifiers only



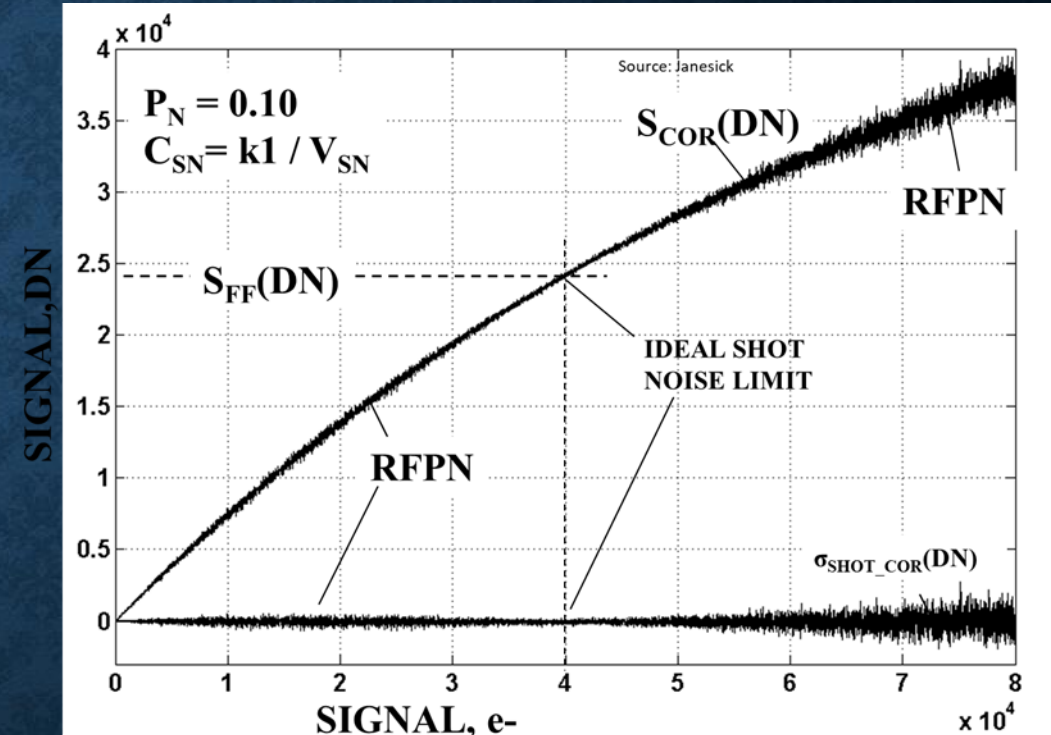
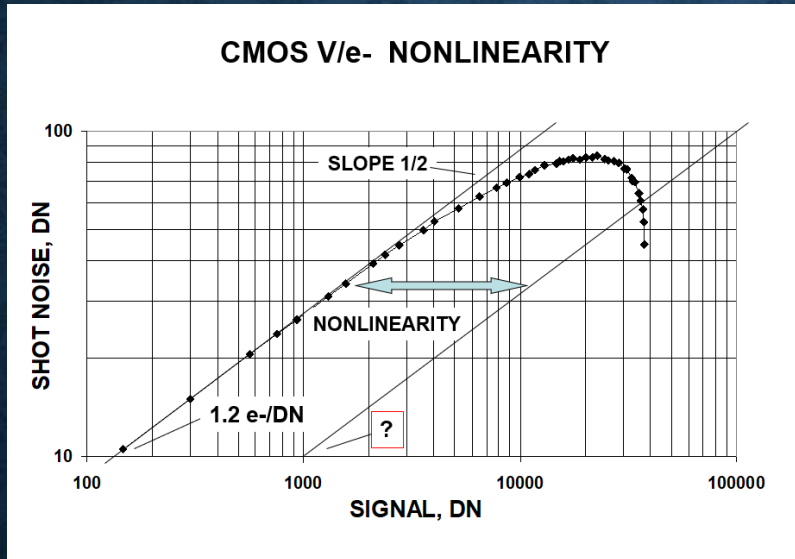
CMOS: V/E NON-LINEARITY & FLAT FIELDING

Reverse biased diode Capacitance vs Voltage (like sense node floating diffusion)



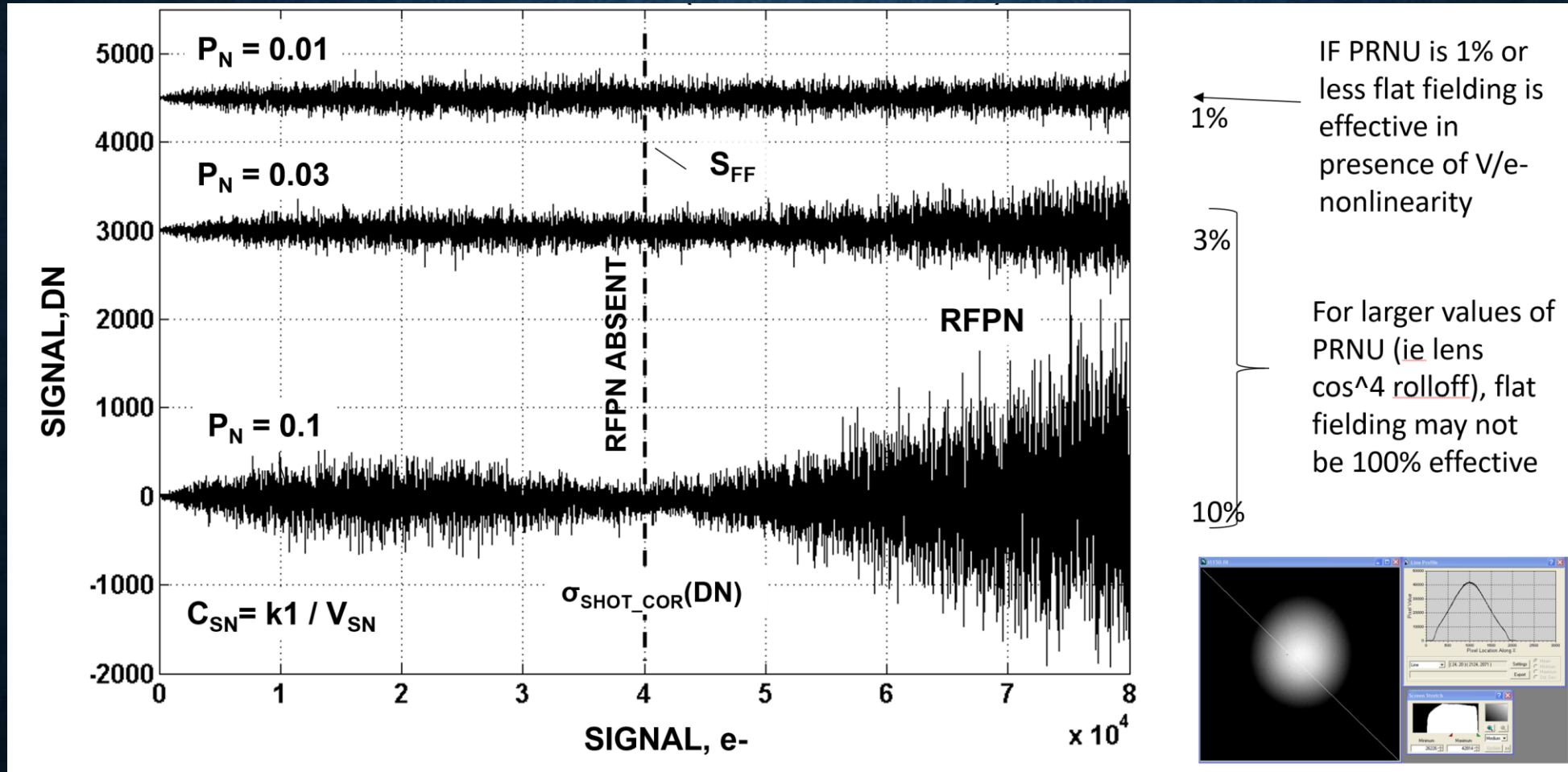
Typical CCD sense node voltage swings

Typical CMOS sense node voltage swings



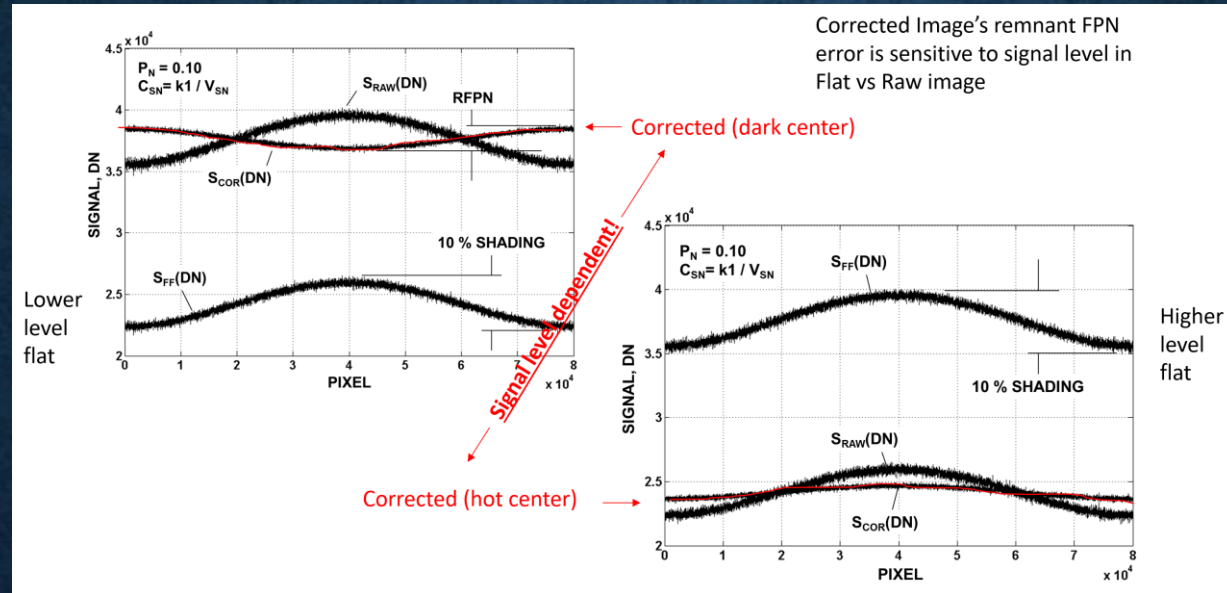
Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: REMNANT FPN

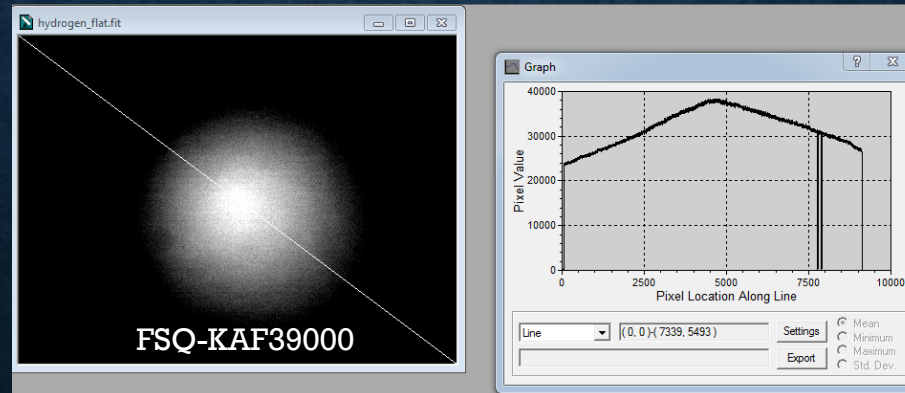


Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: FLAT/SIGNAL DEPENDENT REMNANT FPN



Imperfect flat fielding is the net result



>10% Lens shading/rolloff is not unusual for wide FOV – big sensor combo

SUMMARY

CMOS often has lower read noise than CCD

- Source follower noise is lower because transistor geometry is smaller
- Lower noise with equal QE results in less time to given SNR target

CMOS Sensors can be read at very high speed

- One or two Amplifiers & A/D per column is feasible for ultra fast frame rates (> 1000 frames/sec)
- Very difficult to store the high bandwidth data (32GByte/sec = 1000 frames sec of a 16 megapixel sensor with 16 bits/pixel)

Some CMOS pixel architectures suffer from image lag

- Reminds you of RBI but is a different mechanism
- Can be especially bad in high frame rate video applications

CMOS noise sources behave differently than CCD

- Each pixel has its own amplifier with its own offset and noise characteristics
 - Reset Noise
 - Offset FPN
 - Reset and Offset FPN can be corrected on-chip, depending on architecture
- RTS noise (ultimate noise floor)

CMOS nonlinearities can be more severe than CCD

- V/e - more severe vs CCD and that causes FPN to not be fully removed by flat fielding
- Can cause visible artifacts with as little as 10% lens intensity rolloff & high signal levels

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CCD & CMOS
Half day class

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E-mail: education@spie.org

16 April 2018

Name: Richard Crisp

SPIE invites you to conduct the course, *Introduction to CCD and CMOS Imaging Sensors and Applications* (SC504), at SPIE Optics + Photonics, to be held in San Diego, California United States. Your course is scheduled from 8:30 am to 12:30 pm on 20 Aug 2018. Your signature and return of this form will formalize your acceptance of this invitation.

Photon Transfer
Half day class

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E-mail: education@spie.org

16 April 2018

Name: Richard Crisp

SPIE invites you to conduct the course, *Digital Camera and Sensor Evaluation Using Photon Transfer* (SC916), at SPIE Optics + Photonics, to be held in San Diego, California United States. Your course is scheduled from 1:30 pm to 5:30 pm on 20 Aug 2018. Your signature and return of this form will formalize your acceptance of this invitation.

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