CMOS IMAGE SENSORS

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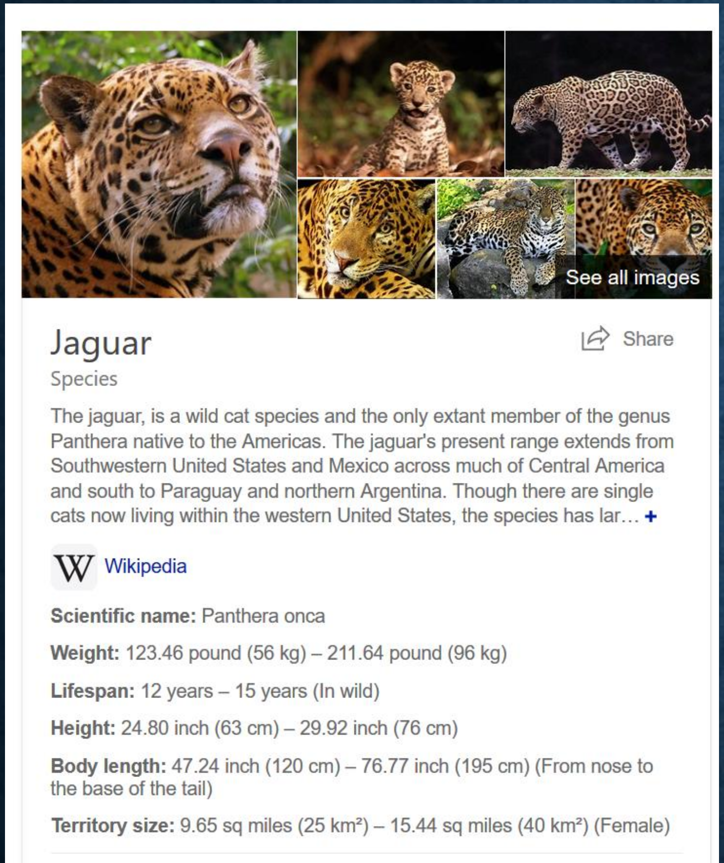
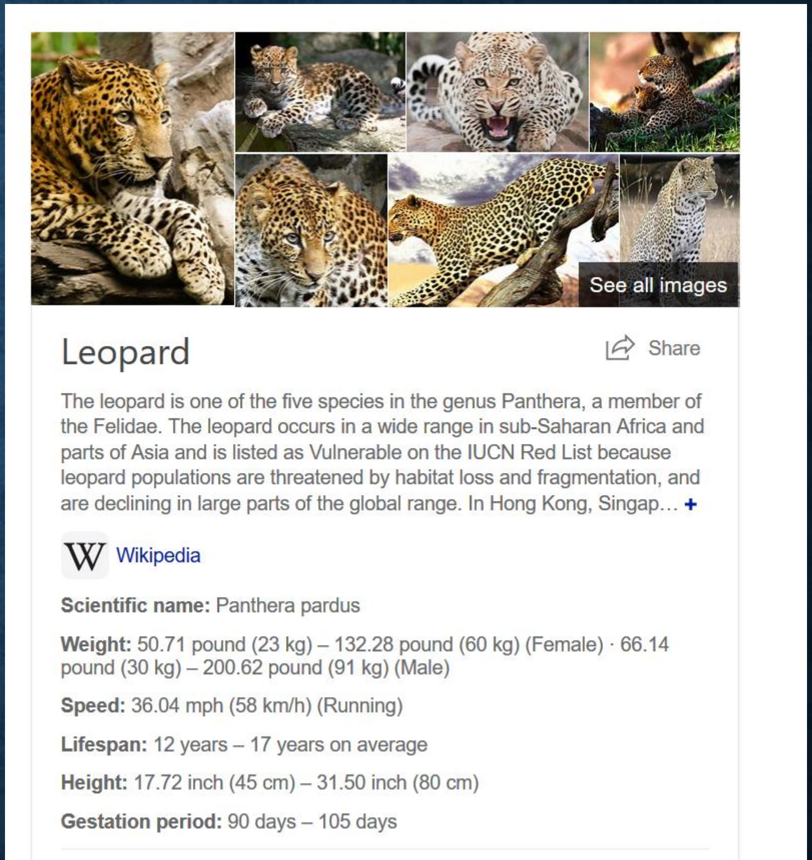
CMOS IMAGE SENSOR:
MAJOR PERFORMANCE DIFFERENCES VS CCD

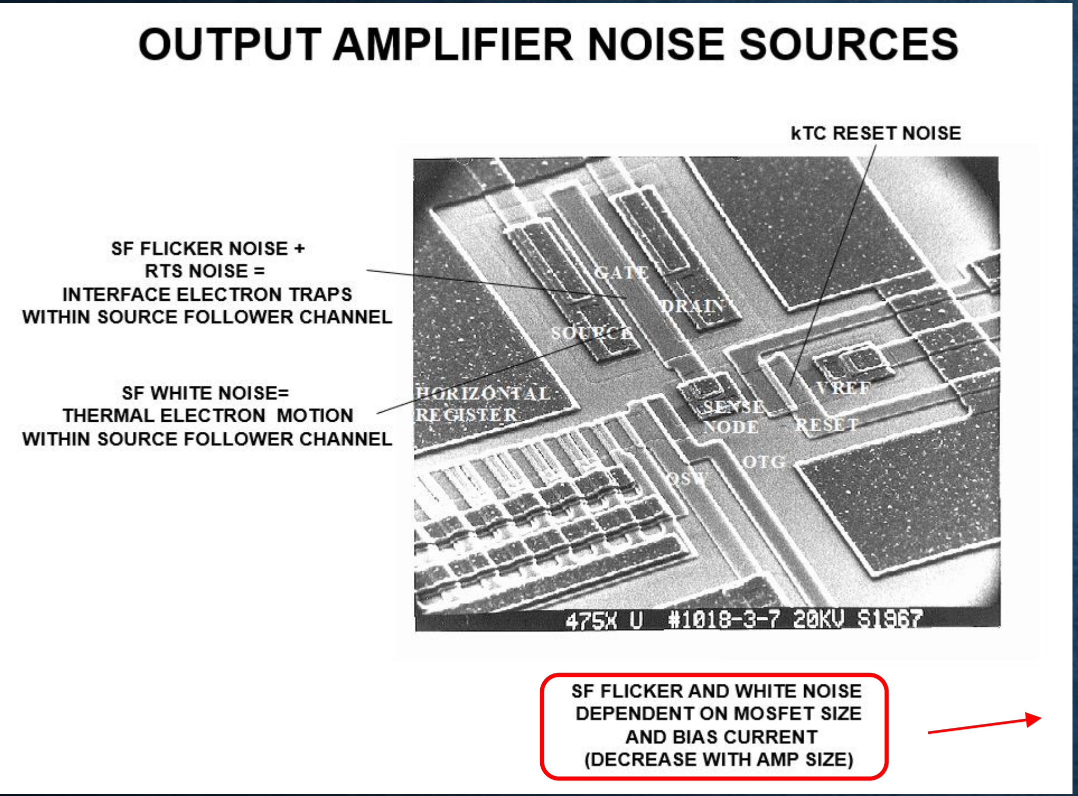
CCD VS CMOS:
JAGUAR VS LEOPARD





“similar but different”

CMOS: OFTEN LOWER READ NOISE THAN CCD

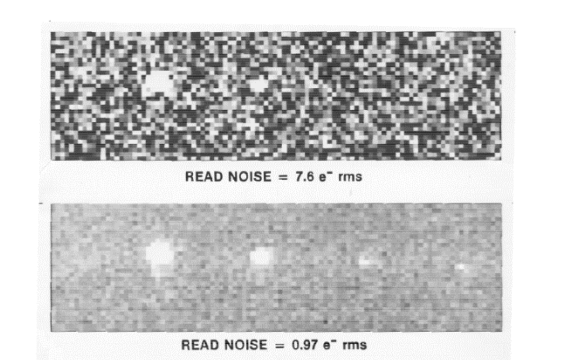


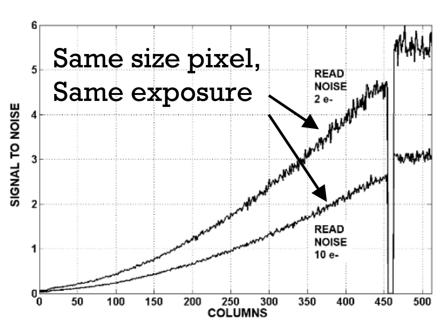
Source follower for CCD drives the off-chip load: **needs a big transistor**

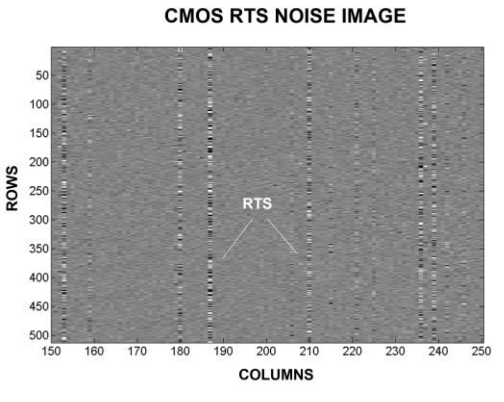
Trapping sites under large area gate electrode of source follower determine 1/F noise for CCD S-F. Large geometry transistor has many sites: behave as continuum of trapping-detrapping

Source follower for CMOS is in each pixel and drives small on-chip load: **uses tiny transistor**

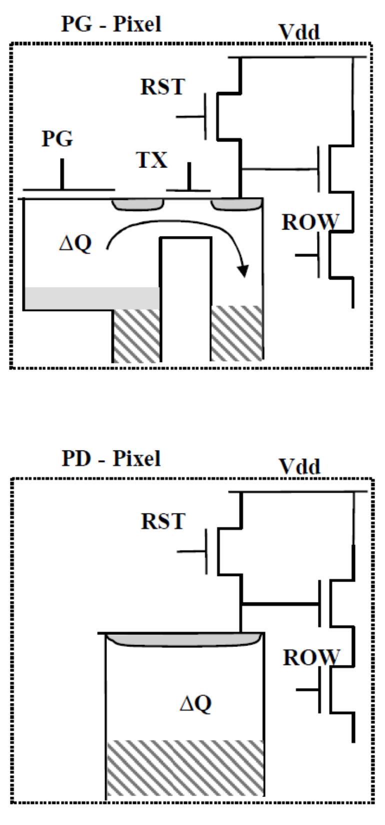
For CMOS, tiny S-F transistor has only small # trapping sites: lower noise & looks like discrete events (called RTS: Random Telegraph Signal)





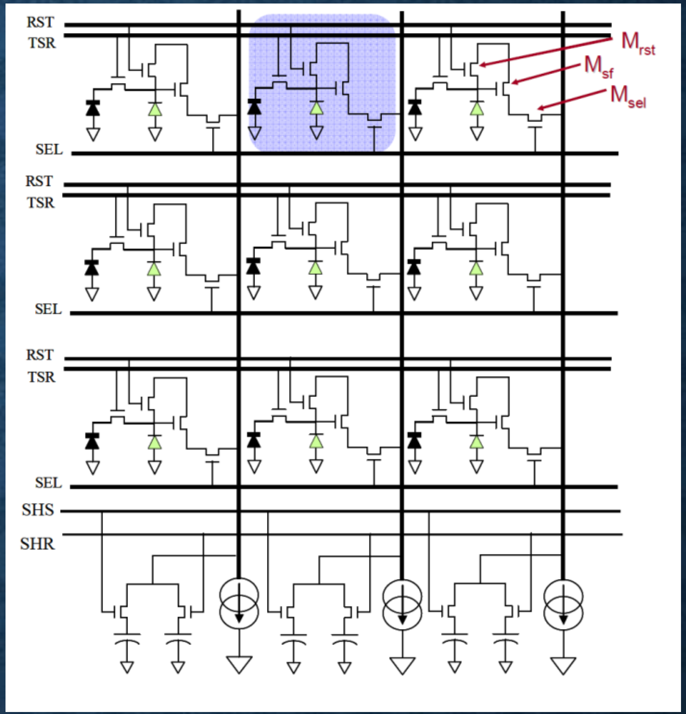


COMMON CMOS PIXEL ARCHITECTURES



4 Transistor
DCDS possible
(noise compensation)
Image Lag
Lower fill factor

3 Transistor
No DCDS
No Image Lag
Higher fill factor



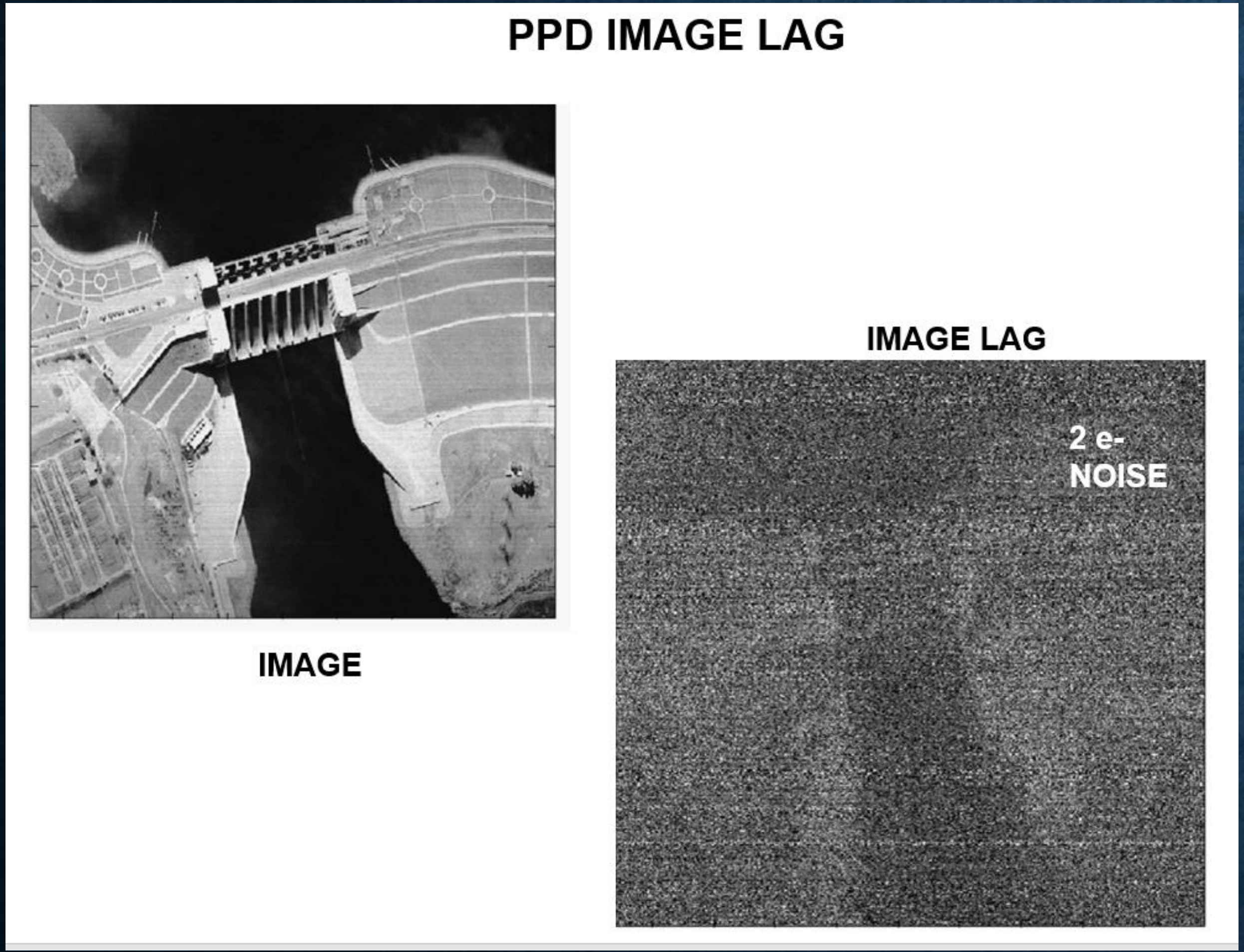
On Chip Binning not feasible with this array design

Amplifier / ADC per column is possible
Can get very fast frame readout rates vs CCD, ie > 1000 frames/sec
Can you store that much data?
(**16Mpix * 1000 f/s** = 16Gigapixels/sec * 16bits/pix = **32Gbytes/sec**)

How many pins do you want and how much power is OK?

Many other architectures / features possible
Depending on pixel/array design
(global snap shutter, A/D per pixel for HDR etc)

CMOS IMAGE LAG (NOT RBI!)



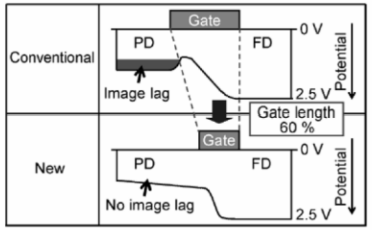
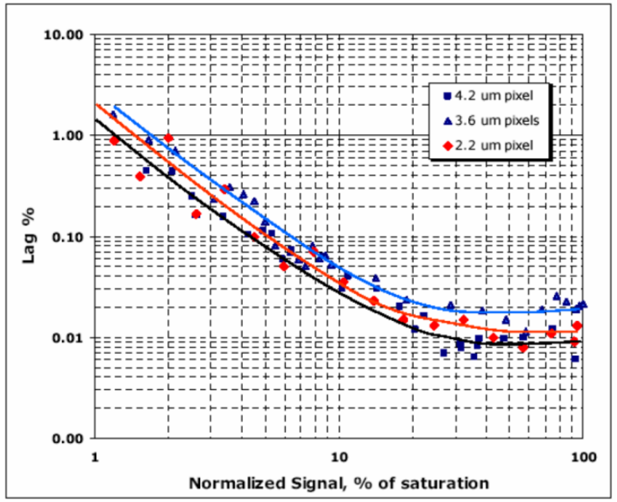


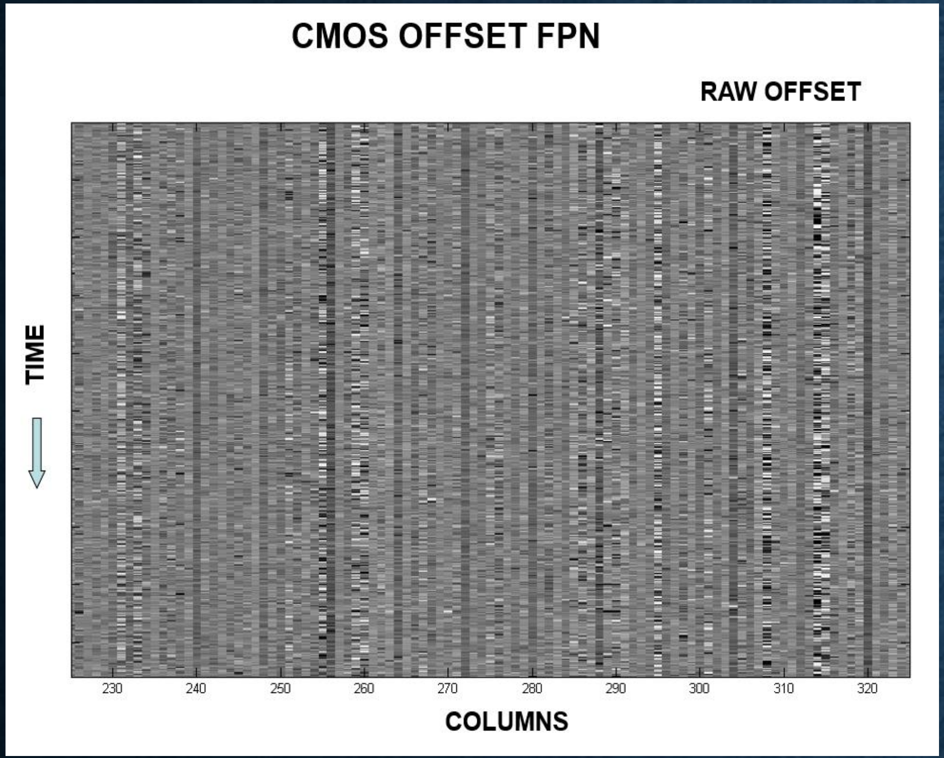
Image lag is a concern especially in small pixels operating at low voltages

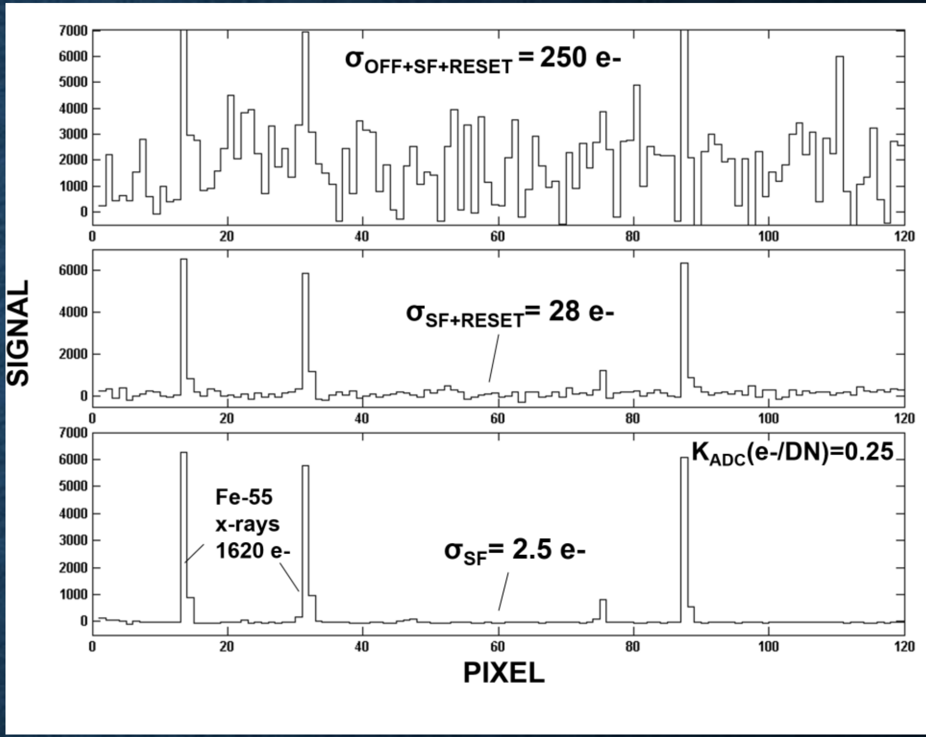
Difference in image lag shows up as pattern noise



Reminds you of RBI but is different mechanism

CMOS OFFSET & RESET FPN



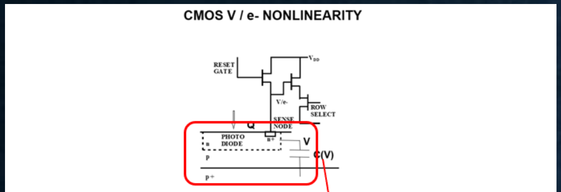


For many CMOS sensors, each pixel in a has its own amplifier
The offset value of each pixel amplifier is a little different resulting in pixel to pixel offset FPN.

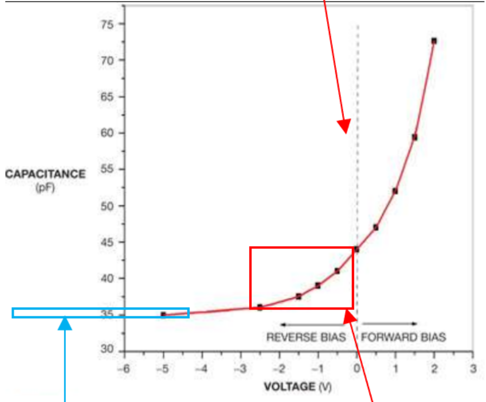
This can be removed on-chip depending on IC architecture
(DCDS, digital correlated double sampling)

CCD usually has 1 to 4 amplifiers only

CMOS: V/E NON-LINEARITY & FLAT FIELDING

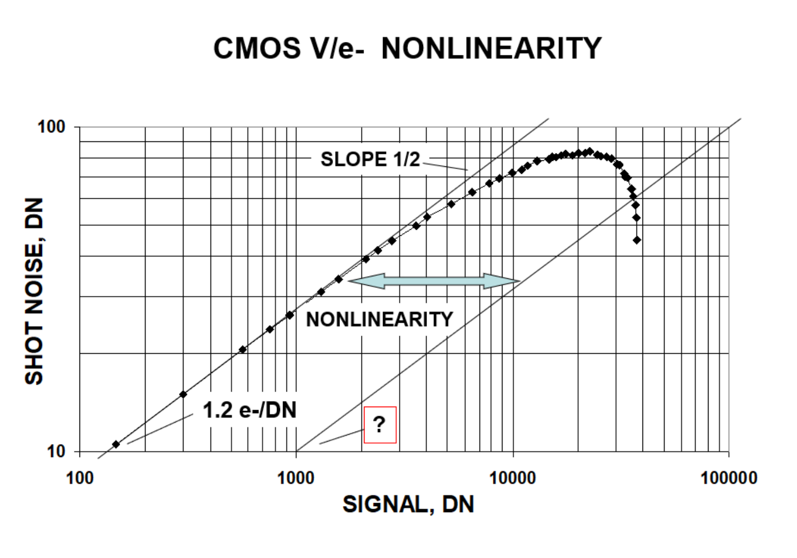


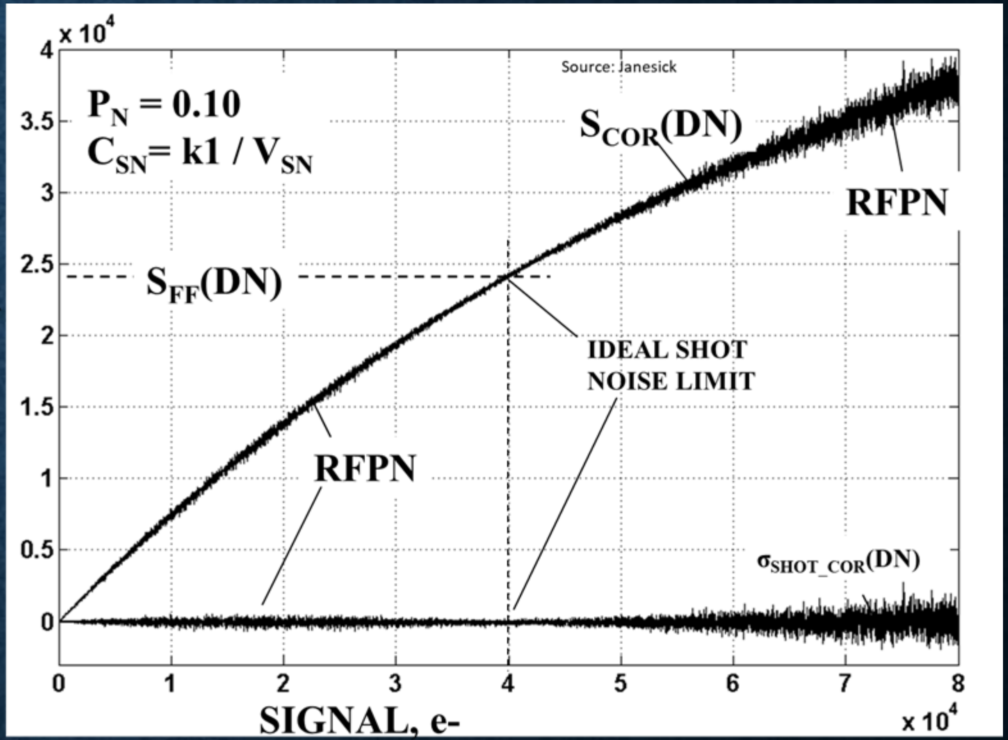
Reverse biased diode Capacitance vs Voltage (like sense node floating diffusion)



Typical CCD sense node voltage swings

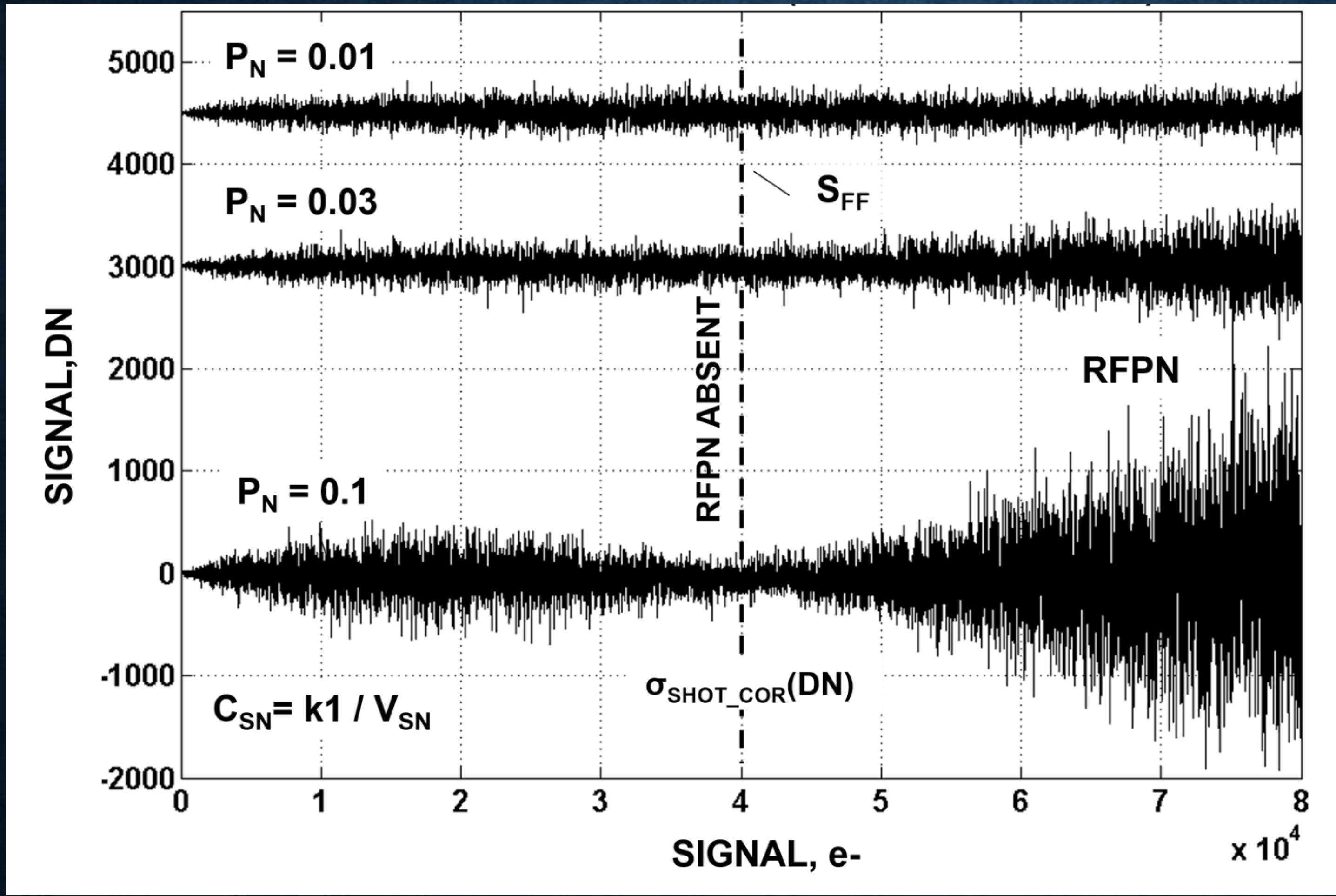
Typical CMOS sense node voltage swings





Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: REMNANT FPN



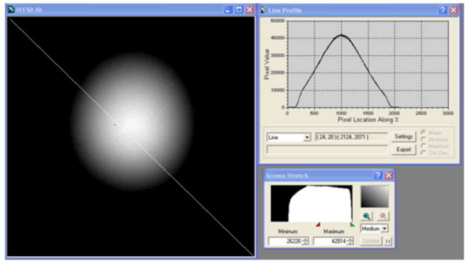
1%

IF PRNU is 1% or less flat fielding is effective in presence of V/e-nonlinearity

3%

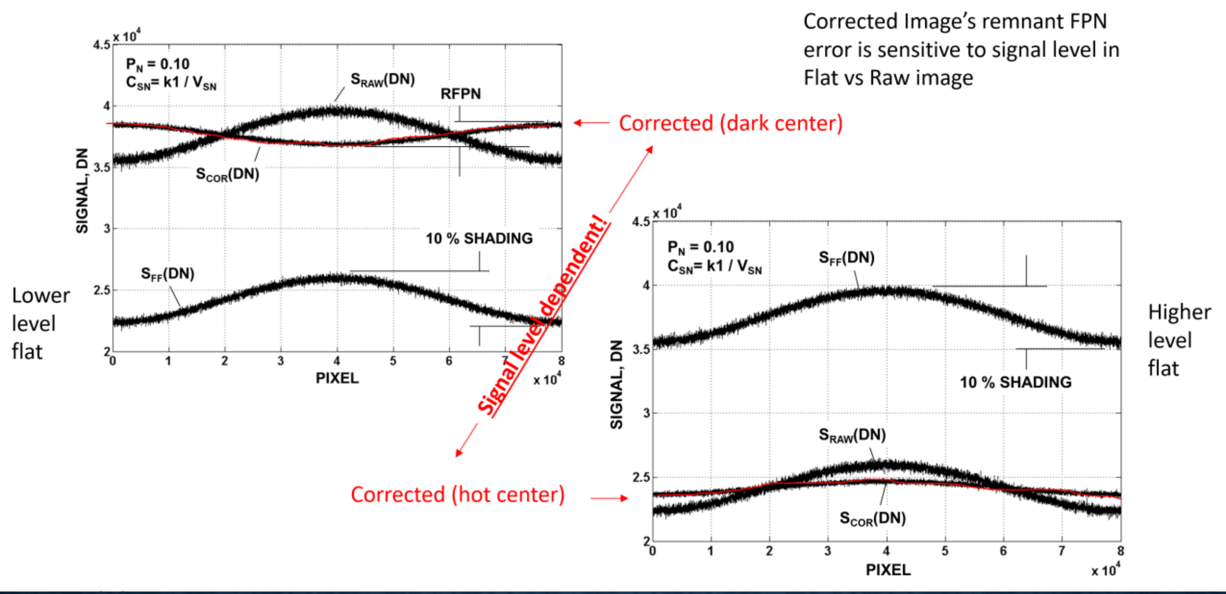
For larger values of PRNU (ie lens cos^4 rolloff), flat fielding may not be 100% effective

10%

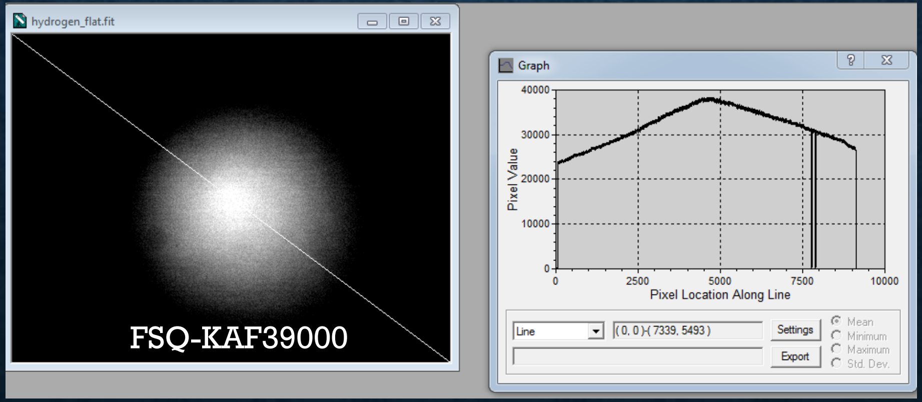


Photon Transfer Plots (Friday Workshop)

CMOS: V/E NON-LINEARITY: FLAT/SIGNAL DEPENDENT REMNANT FPN



Imperfect flat fielding is the net result



>10% Lens shading/rolloff is not unusual for wide FOV – big sensor combo

SUMMARY

CMOS often has lower read noise than CCD

- Source follower noise is lower because transistor geometry is smaller
- Lower noise with equal QE results in less time to given SNR target

CMOS Sensors can be read at very high speed

- One or two Amplifiers & A/D per column is feasible for ultra fast frame rates (> 1000 frames/sec)
- Very difficult to store the high bandwidth data (32GByte/sec = 1000 frames sec of a 16 megapixel sensor with 16 bits/pixel)

Some CMOS pixel architectures suffer from image lag

- Reminds you of RBI but is a different mechanism
- Can be especially bad in high frame rate video applications

CMOS noise sources behave differently than CCD

- Each pixel has its own amplifier with its own offset and noise characteristics
    - Reset Noise
    - Offset FPN
        - Reset and Offset FPN can be corrected on-chip, depending on architecture
- RTS noise (ultimate noise floor)

CMOS nonlinearities can be more severe than CCD

- V/e- more severe vs CCD and that causes FPN to not be fully removed by flat fielding
- Can cause visible artifacts with as little as 10% lens intensity rolloff & high signal levels

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16 April 2018

Name: Richard Crisp

SPIE invites you to conduct the course, ***Introduction to CCD and CMOS Imaging Sensors and Applications*** (SC504), at SPIE Optics + Photonics, to be held in San Diego, California United States. Your course is scheduled from 8:30 am to 12:30 pm on 20 Aug 2018. Your signature and return of this form will formalize your acceptance of this invitation.

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E-mail: education@spie.org

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