January 18th 2013

DIMM-in-a-Package and Bond Via Array POP Technologies for Mobile Memory

Richard Crisp (Chief Technologist)

Invensas Solutions for Ultrabooks and Tablets

Invensas with Dell and the XPS-12 (with DIMM-in-a-Package Memory)
Running Windows 8 at CES 2013, Las Vegas.

Invensas xFD

Who is Invensas?

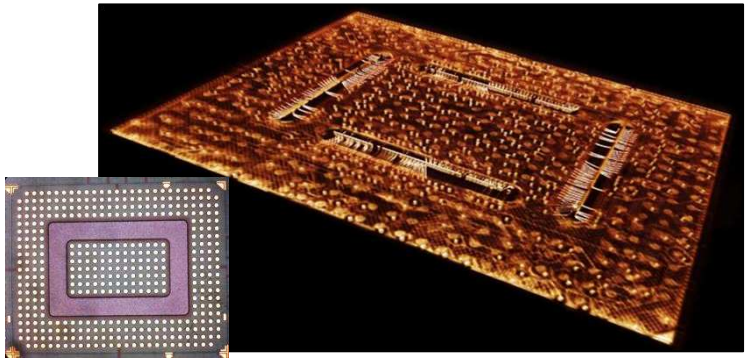
- ***Formation:*** Founded in 2011 as a wholly owned subsidiary of Tessera Technologies, Inc. (Nasdaq:TSRA)
- ***Goal***: Develop and commercialize breakthrough semiconductor interconnect solutions and IP in Mobile, Storage and Cons. Electronics.
- ***Core Focus***: "Interconnectology": adv. interconnect, semiconductor packaging, memory circuitry, modules, 3D TSV architecture.
- ***Company***: 50+ Employees (1/3 PhD). ***Headquarters***: San Jose, CA.
- ***IP***: ~1000 patents and applications.

Invensas Product Development Prototyping Capabilities

Invensas, has advanced prototyping capabilities from Wirebond, Flip-chip and 3D-TSV: Circuit Level to Package to Board and System Level

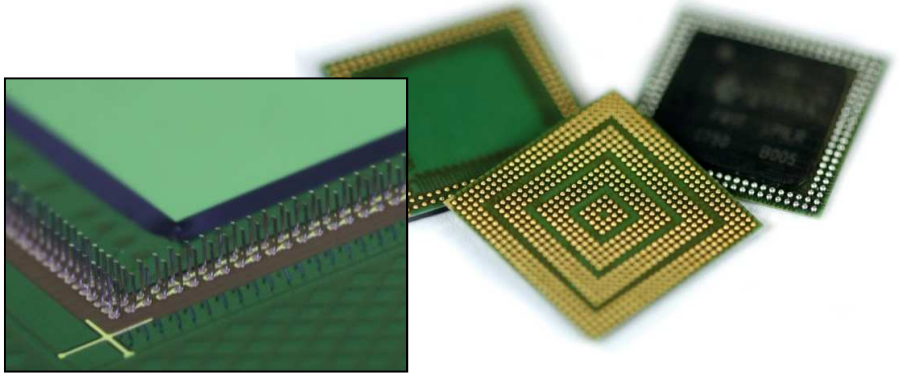
Invensas Technology Platforms

MEMORY (xFD):



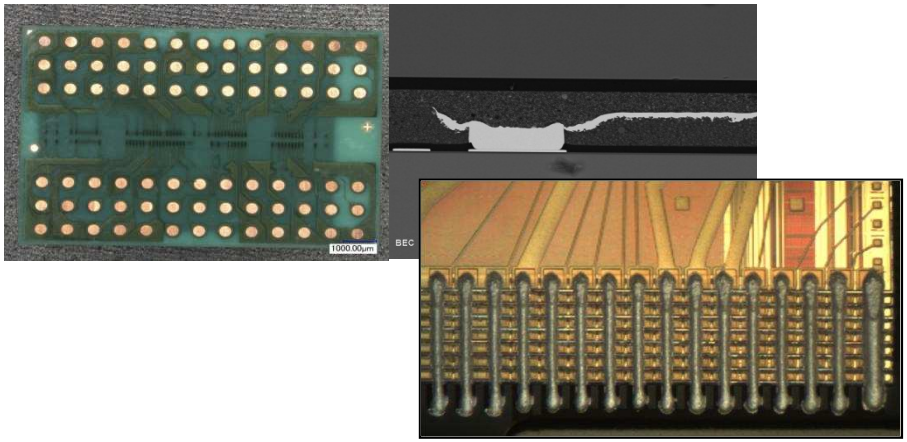
- DIAP for Ultrabooks & Tablets.
- xFD for Servers and Datacenters.

MOBILE (BVA):



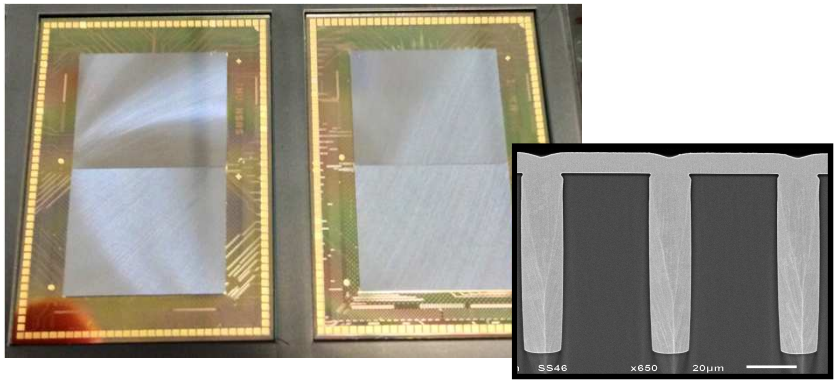
- Bond Via Array for Ultra Smartphones
- Cu-Pillar PoP for Smartphones/Tablets

WAFER LEVEL PACKAGING:



- Fan-Out Wafer Level Packaging
- Stacked WLP for Flash Memory/SSD

3D-IC:



- Fine-Pitch TSV Interposers
- 3D Memories
- 3D Capacitors

Ongoing Investment in R&D: Adding Continual Value

Our ongoing investment in R&D sustains and grows our packaging royalty base

3D IC

2.5D Interposer

Low Cost DRAM CSP

Fine Pitch PoP for Mobile Apps

xFD for Stacked DRAM

Long-term R&D investments plus partnership

Near-term R&D investments

Recently commercialized

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DIMM-in-a-PACKAGE technology

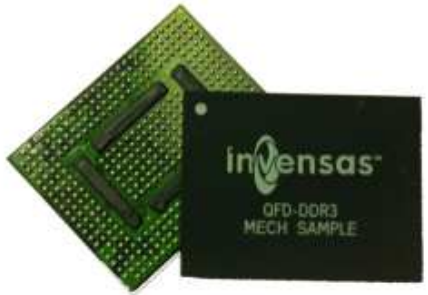
Key Project Management Advantages

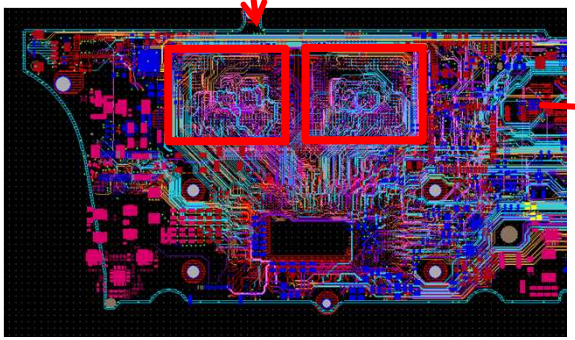
- Design Flexibility
  - One low-cost Type 3 PCB design can support a broad range configuration options: 2 die/channel to 16 die / channel
- Design Resource Management
  - One PCB design instead of multiple designs to staff for SKU mix
- PCB Logistics
  - Standard Type 3 PCB in 5 days versus 3 weeks for Type 4 HDI PCBs
  - Lower Manufacturing Cost
  - Type 3 PCB vs Type 4 PCB

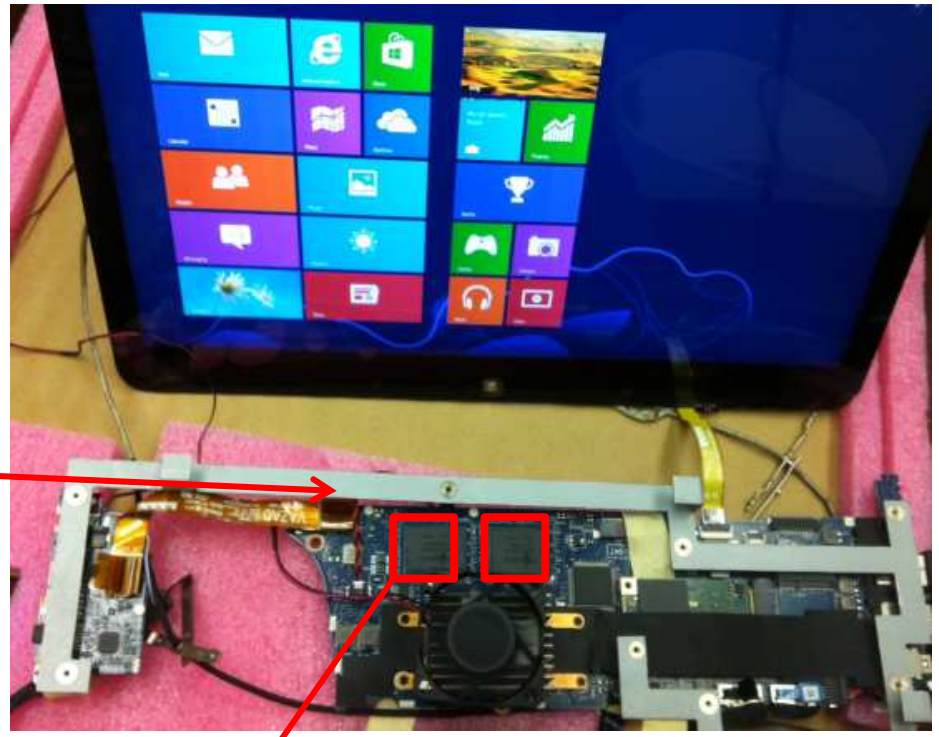
Key Benefits of DIMM-in-a-PACKAGE module technology

- Full DIMM functionality in a single package including I2C interface
- Designed for low-cost solder-down use: no HDI motherboards required
- Common ball-map for DDR3, DDR4 and LPDDR3 multi-die DRAM packages
  - Standardized footprint/ball-map for channel-wide solder-down memory: ie "DIMM connector" for solder-down memory
- Broad range of device configuration options from single PCB design
  - DDR3 and LPDDR3 co-support at PCB level
- Single-sided or clamshell system use
- Best thermal characteristics of multi-die packages
- Manufactured using existing wirebond FBGA lines: streamlined process flow

First Ultrabook System Using DIAP Now Running Win8







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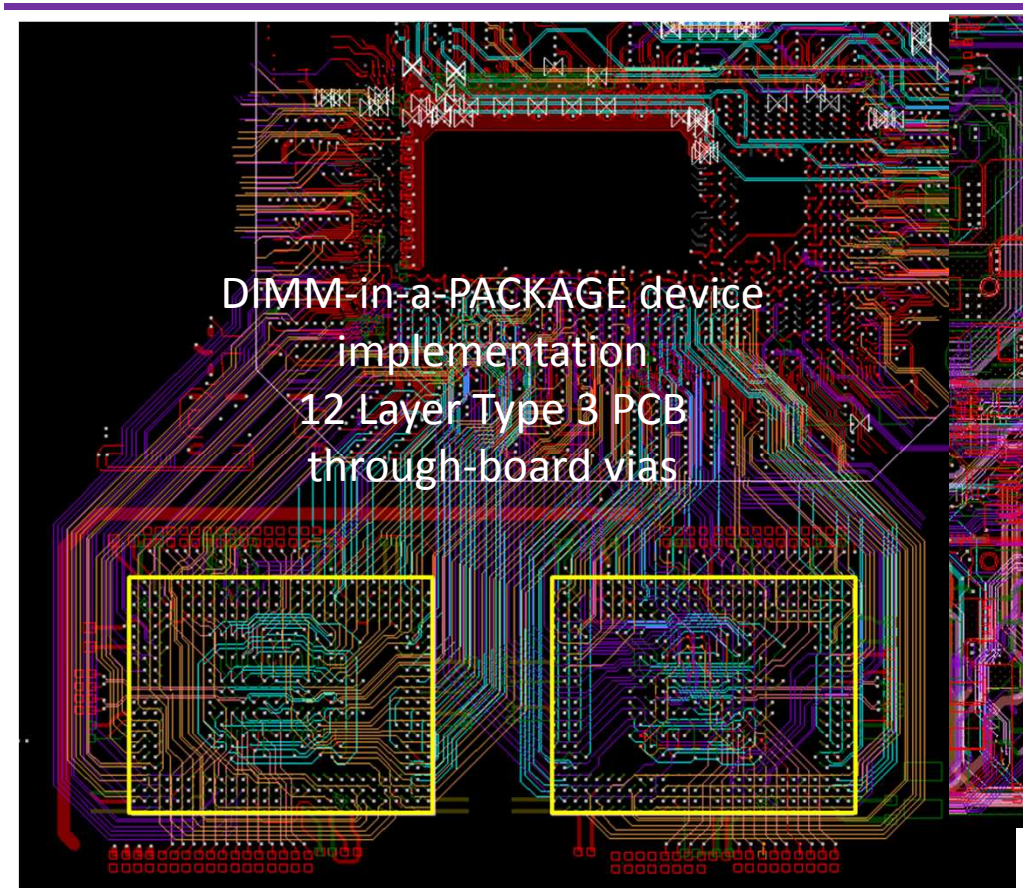
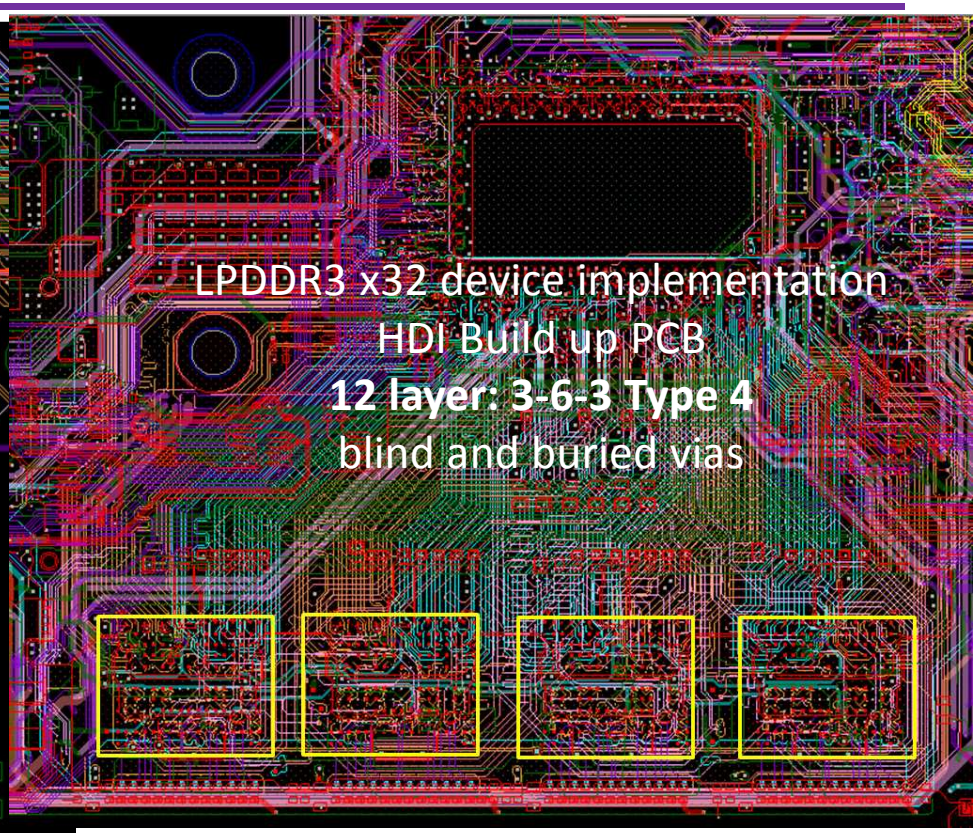
2013: Routed Haswell CPU/memory area comparison





Single Side Assy Configuration options:
2 LPDDR3 (x32) per channel (1 rank)
4 LPDDR3 (x32) per channel (2 rank)
4 LPDDR3 (x16) per channel (1 rank)
4 DDR3 (x16) per channel (1 rank)
8 DDR3 (x8) per channel (1 rank)

Single Side Assy Configuration options:
2 LPDDR3 (x32) per channel (1 rank)
4 LPDDR3 (x32) per channel (2 rank)

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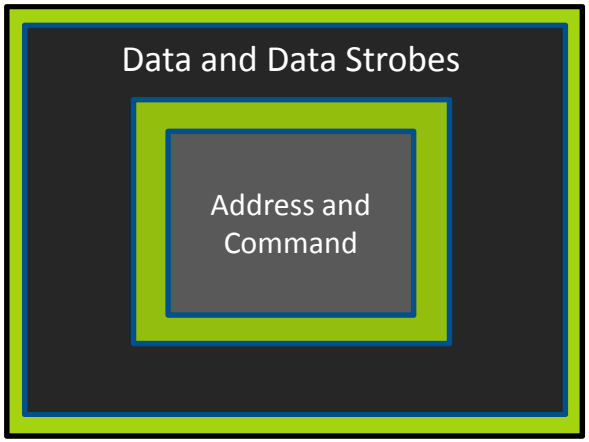
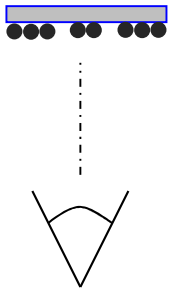
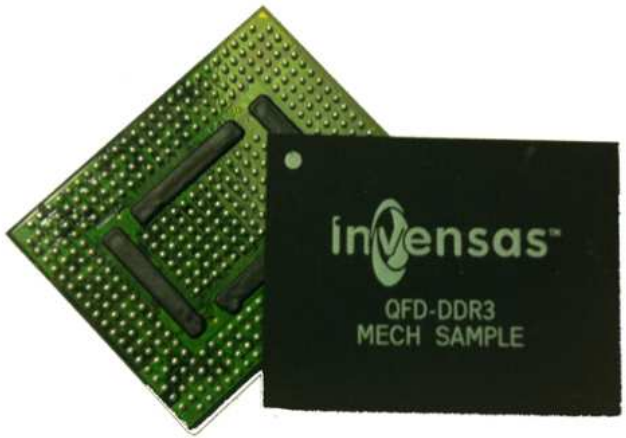
DIMM-in-a-PACKAGE Memory Device: Family Members

DIMM-in-a-PACKAGE Module: Ball Map Plan



Ball Map plan





407 BGA
17.5 x 22.5 mm
0.8 x 0.8 mm ball pitch

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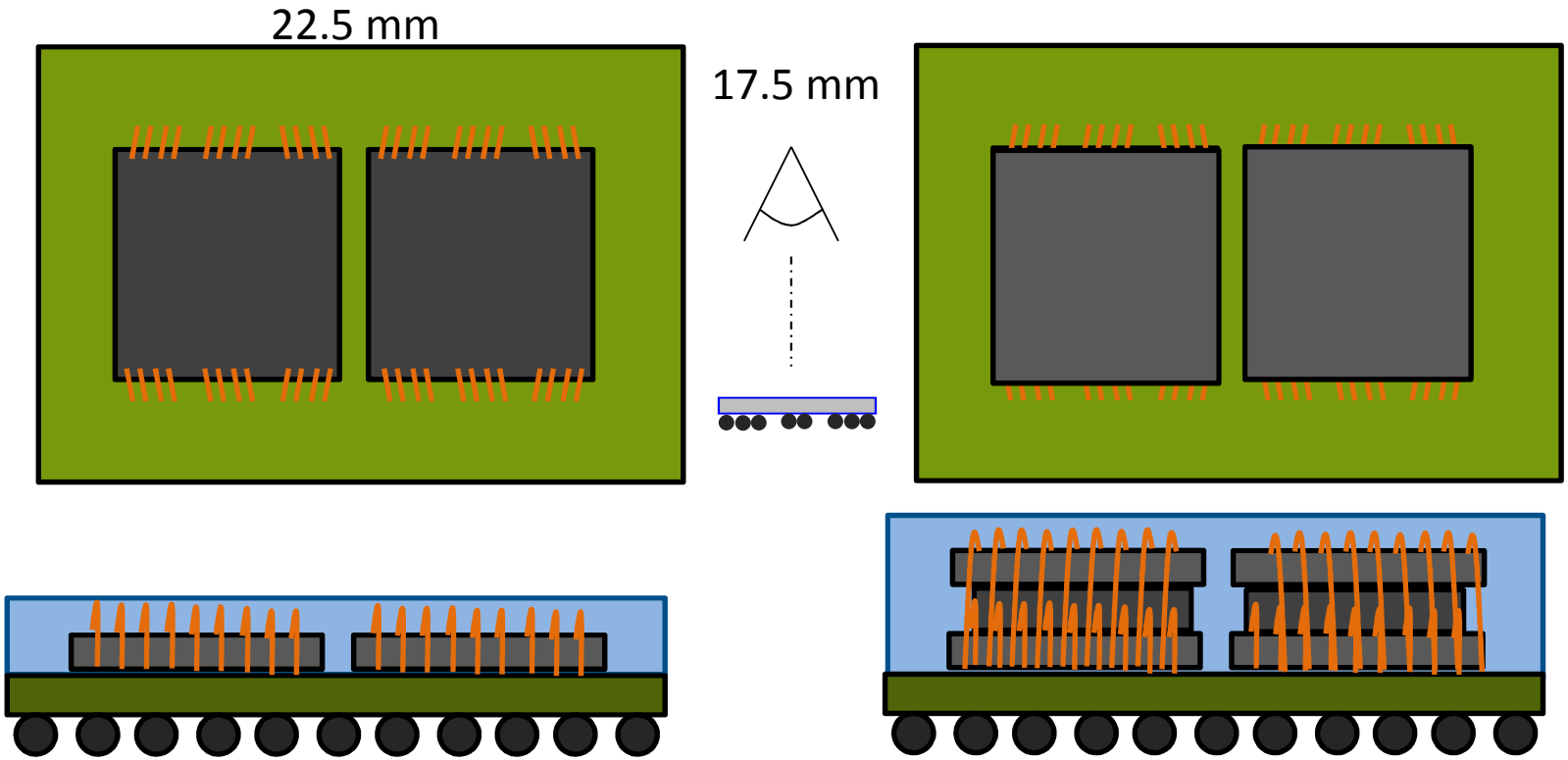
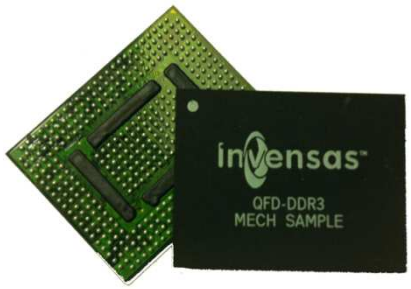
2 Die and 4 Die Structures: DIMM-in-a-PACKAGE Module



Dual Face Up

Quad Face Up Spacer



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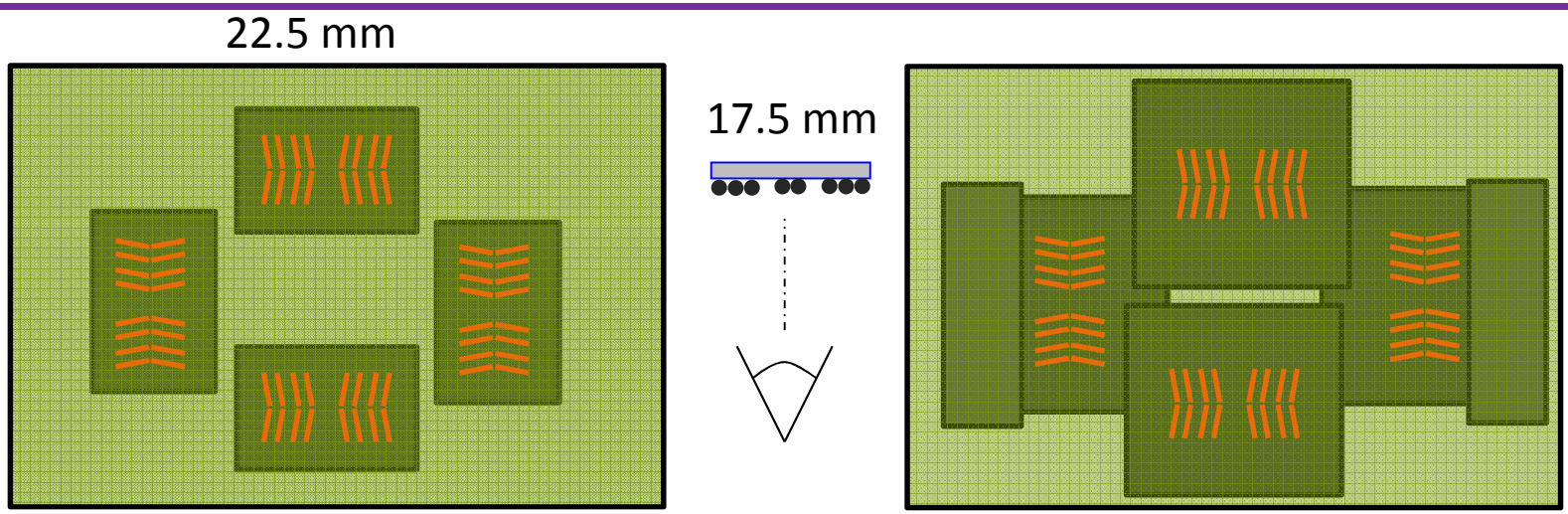
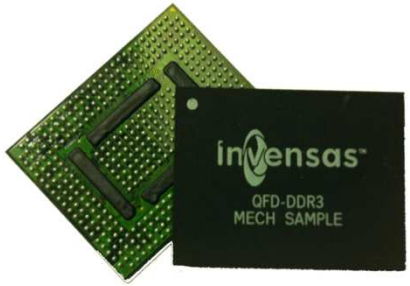
4 Die Structures: DIMM-in-a-PACKAGE Module



Quad Face Down Planar
(small die)

Quad Face Down Stack
(large die)



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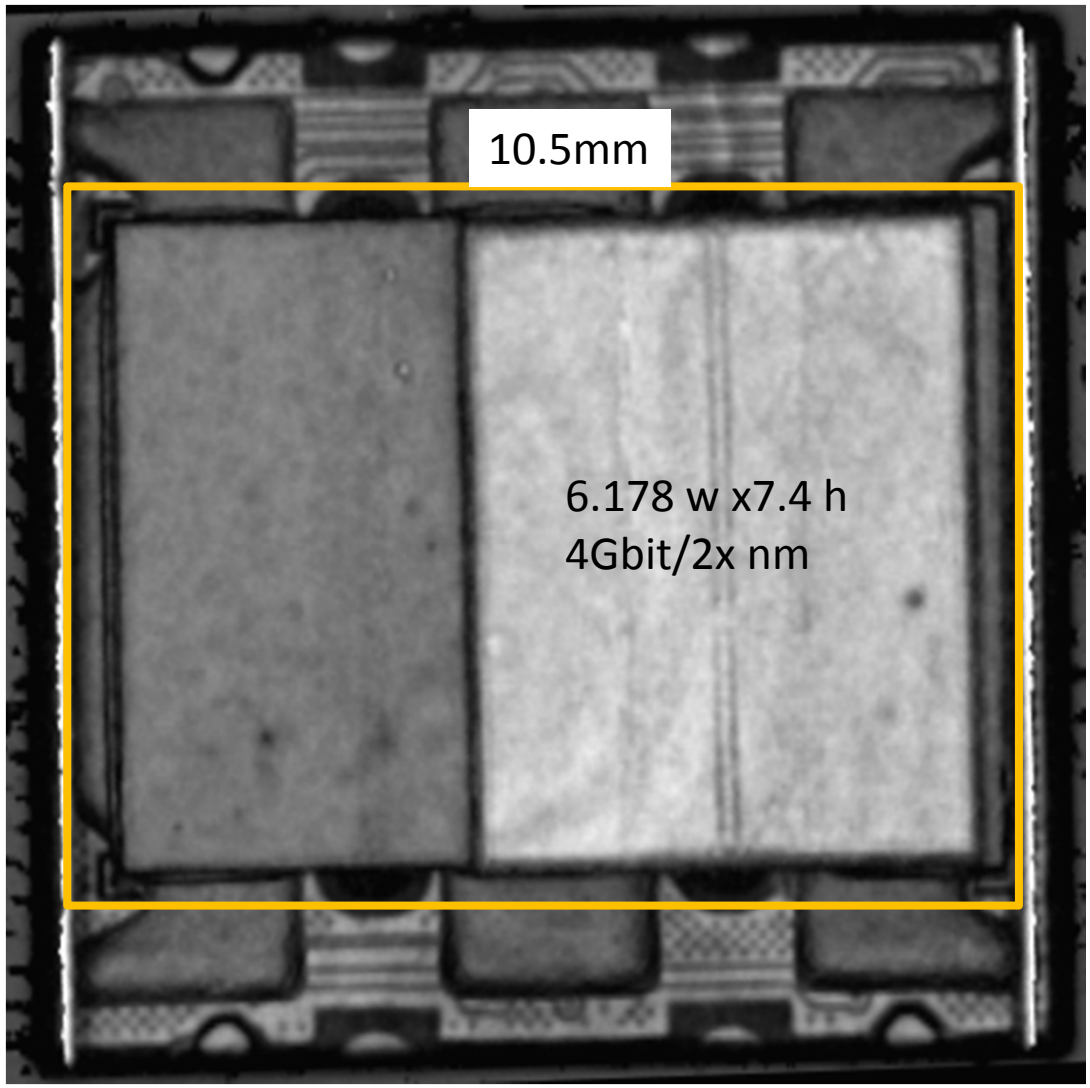
Shrinking the DFD -> µDFD



8 mm

Reduce encapsulation to 0.25mm on four sides

Reduce ball pitch to 0.5 x 0.8 mm

Add three rows (24 extra balls) for enhanced PI/SI

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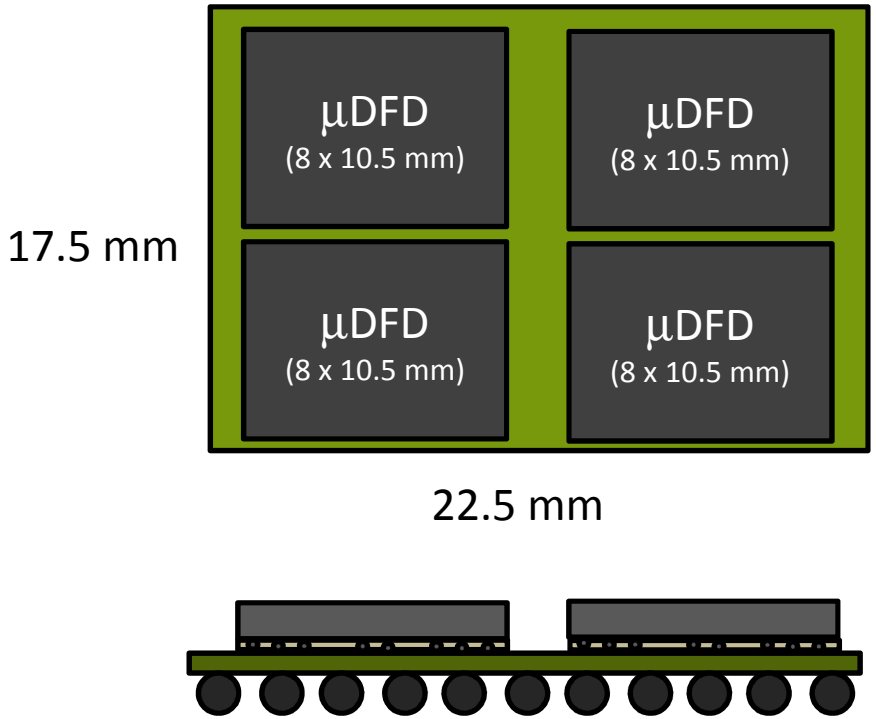
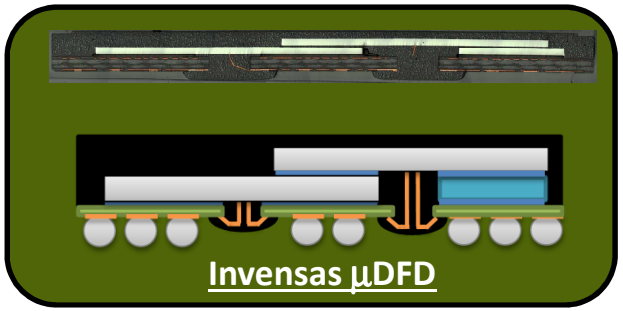
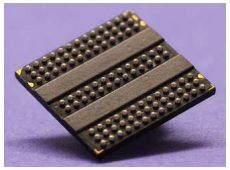
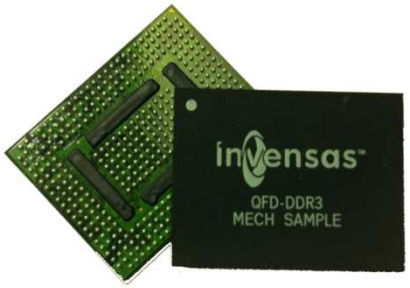
8 Die DIMM-in-a-PACKAGE Module







Eight Die Interposer using µDFD



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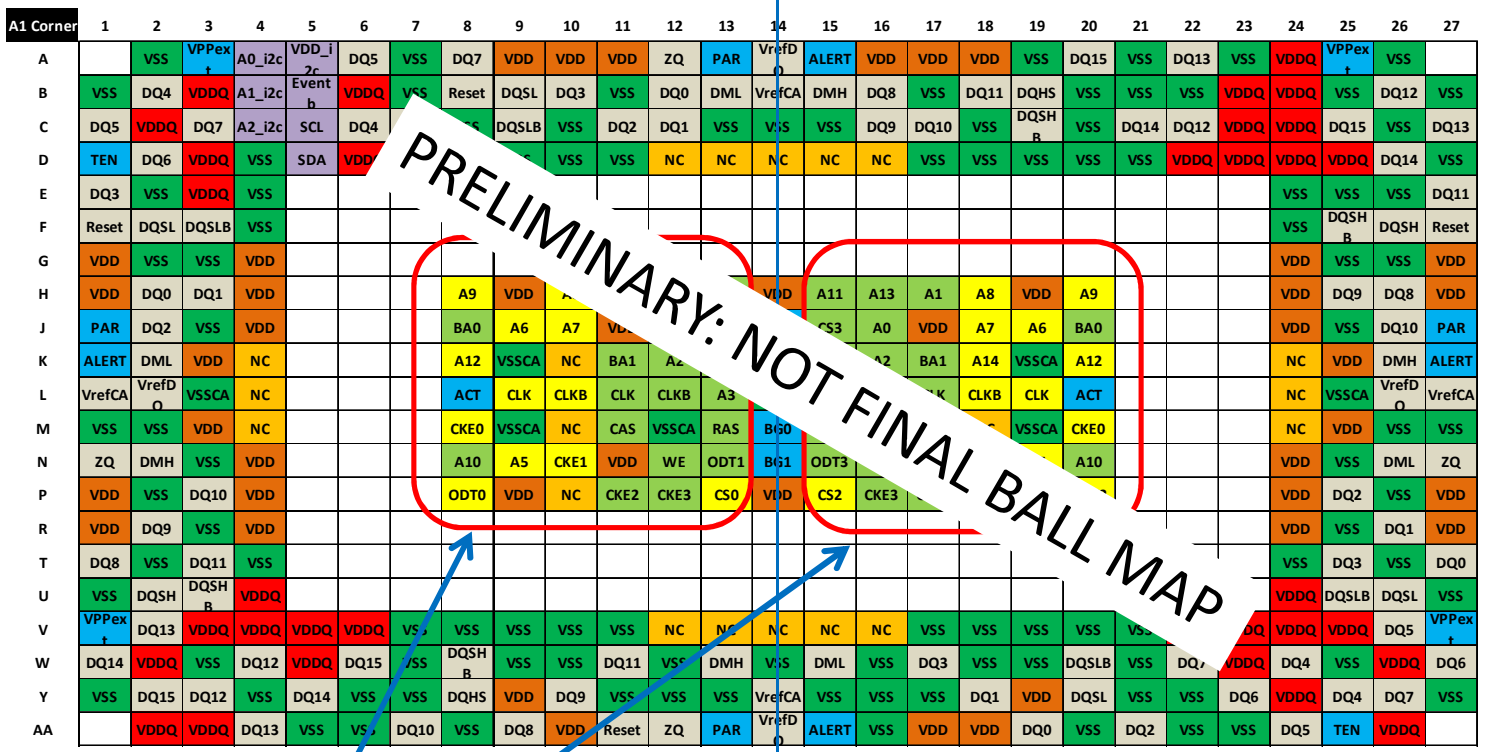
System-Level co-support of LPDDR3 and DDR3

Example Ball Map Features

Axis of Signal Symmetry

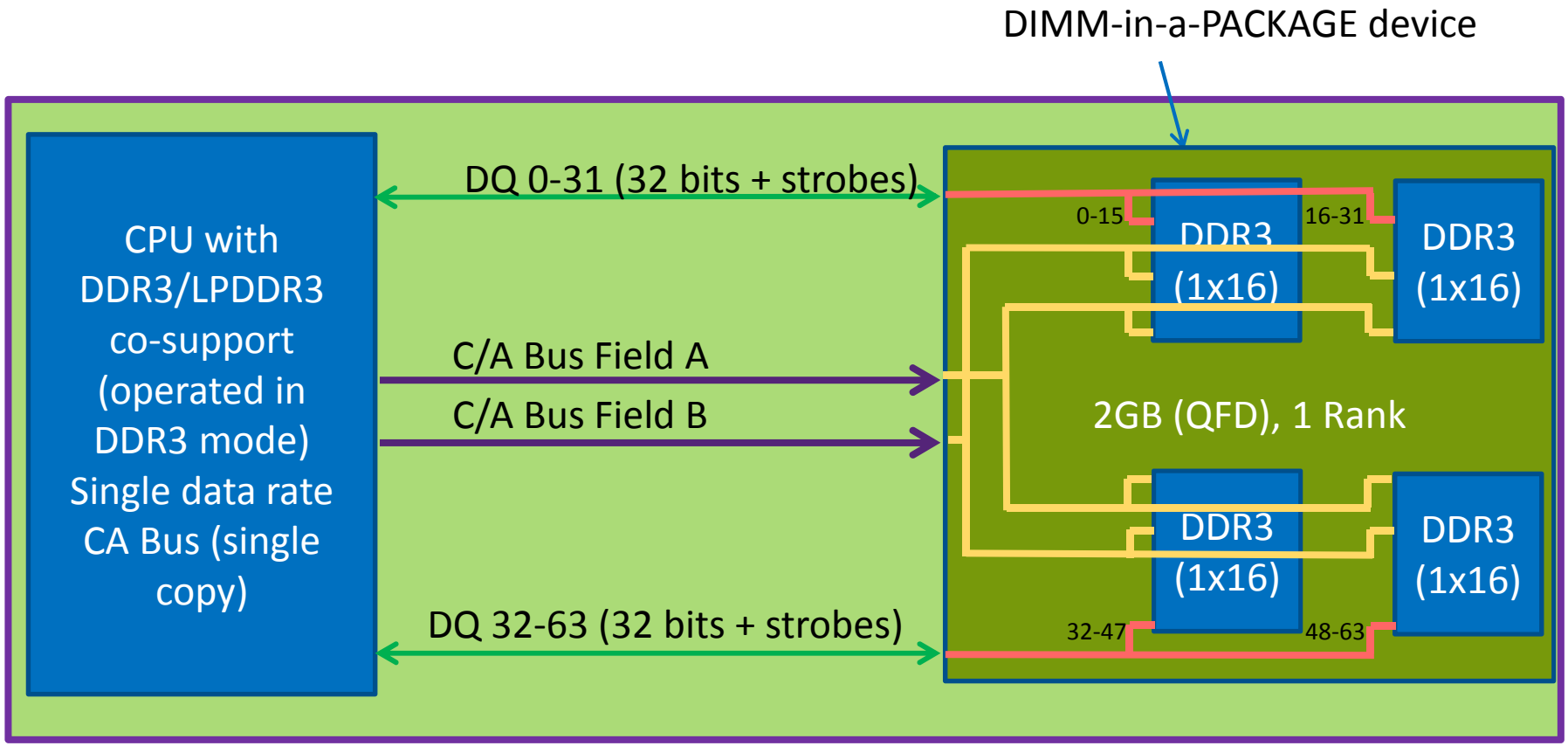
All signals: 0.8 x 0.8mm pitch
For simple PCB routing



Redundant set of
Command Address Signals

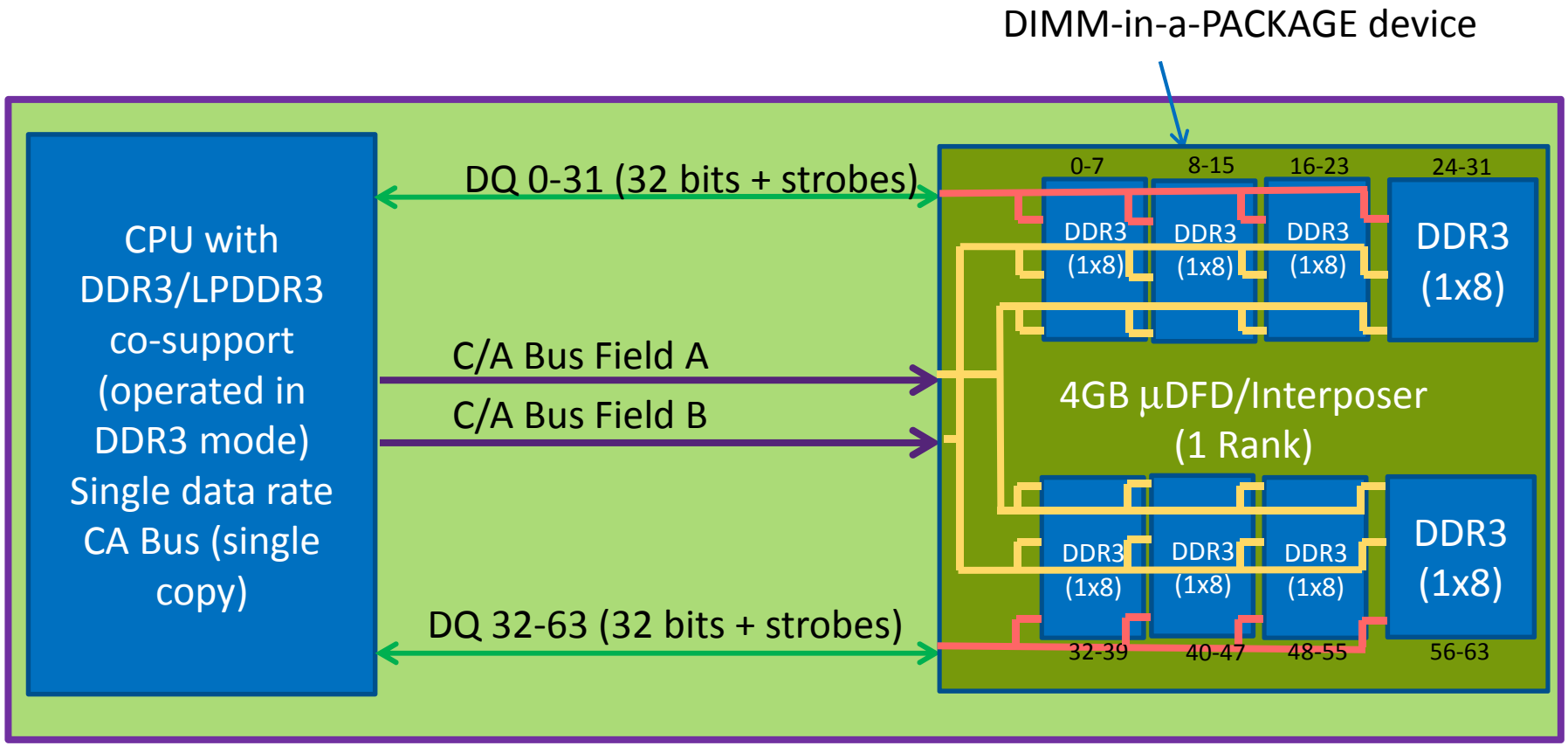
Simplifies substrate and PCB routing
Provides dual x32 or single x64 operation
PCB-level Co-support for LPDDR3/DDRx

Single Sided Deployment: configuration options



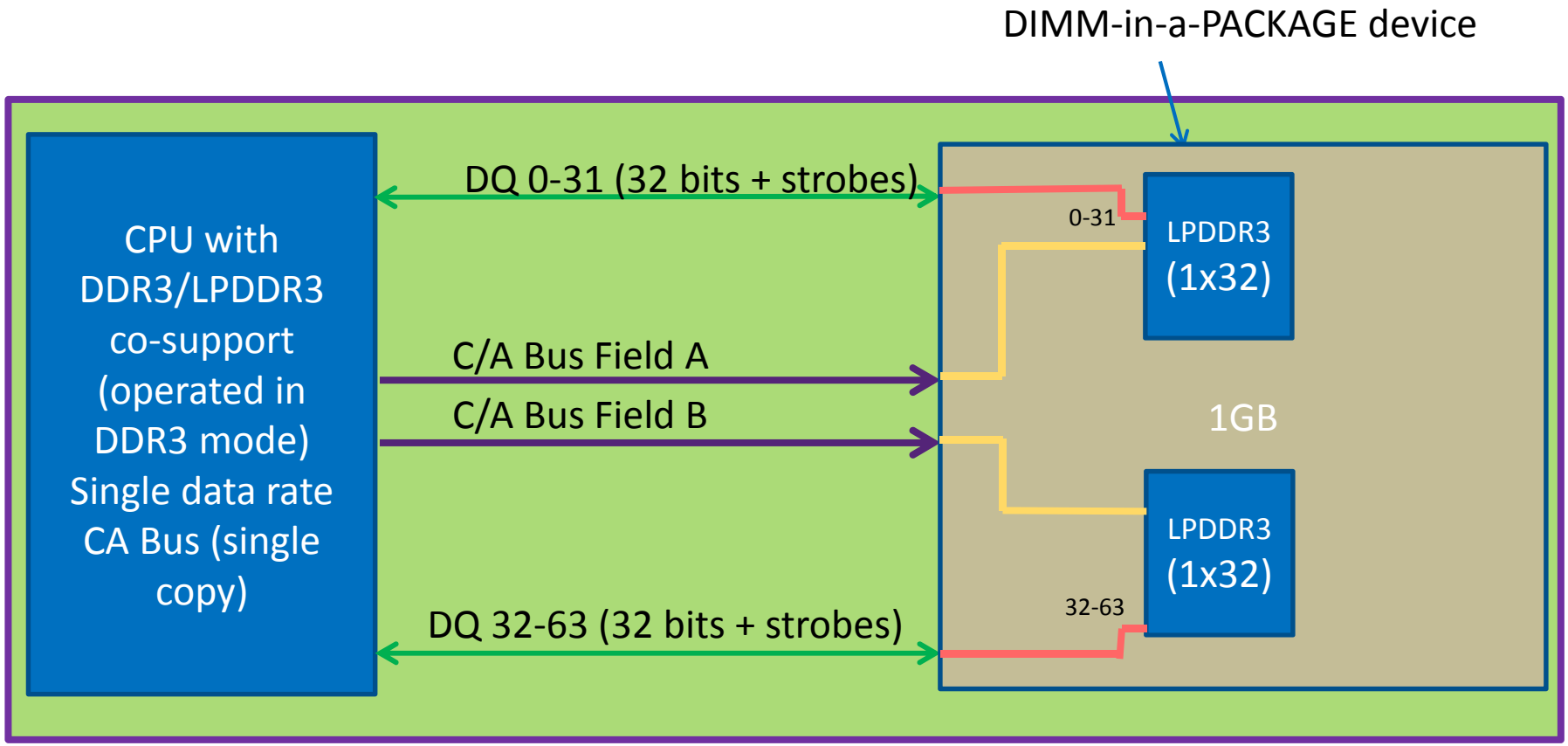
One of two identical memory channels shown

Single Sided Deployment: configuration options



One of two identical memory channels shown

Single Sided Deployment: configuration options



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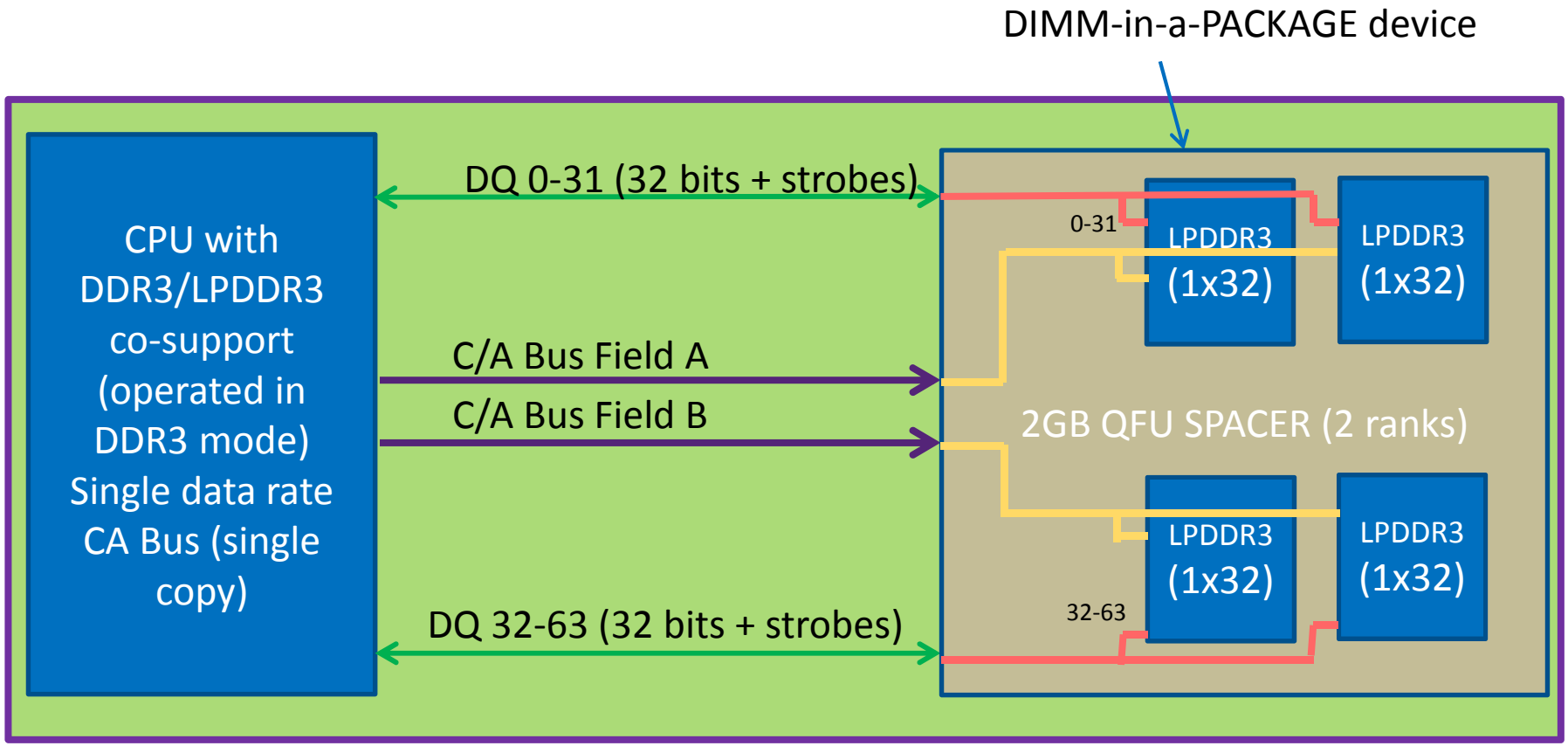
Single Sided Deployment: configuration options



One of two identical memory channels shown

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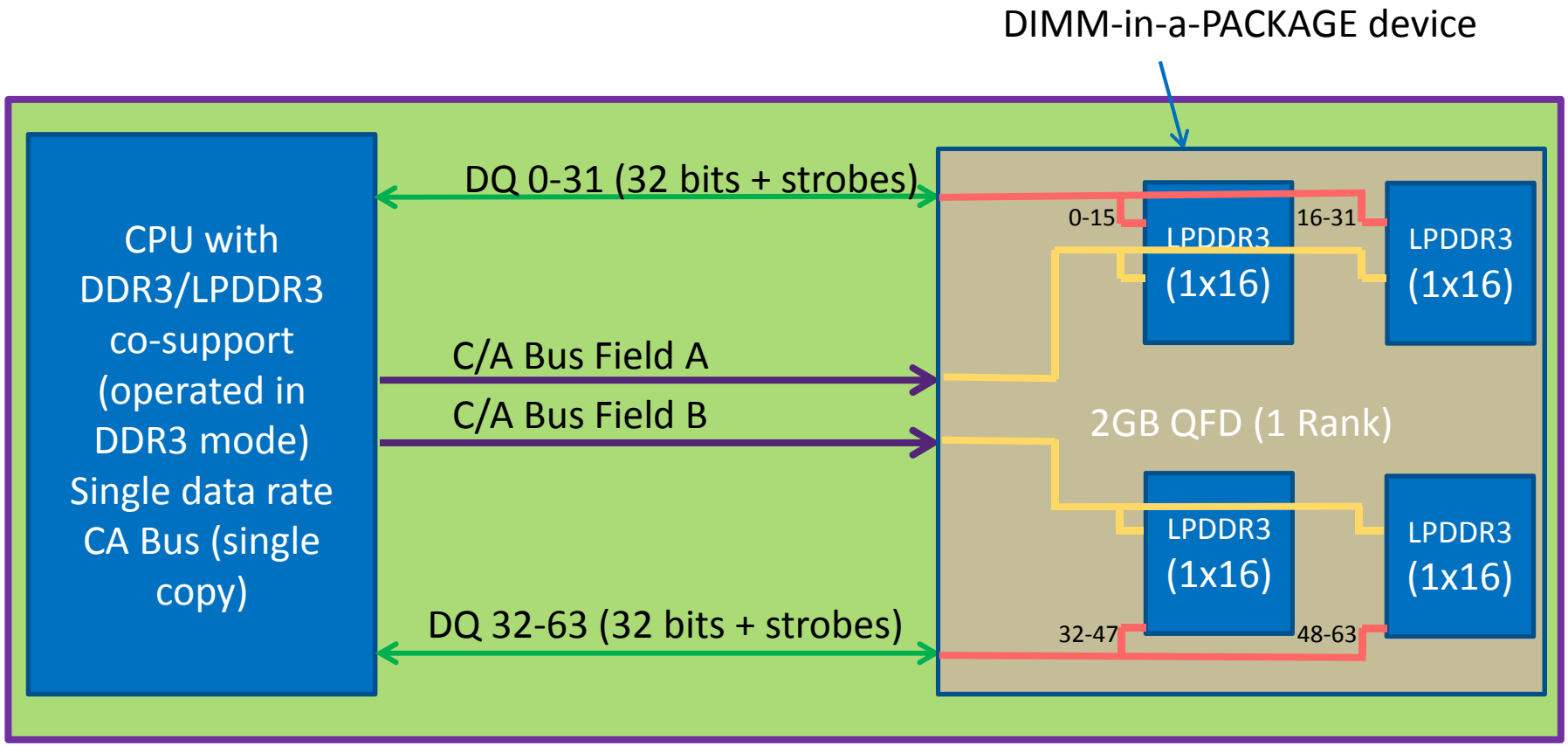
Single Sided Deployment: configuration options



One of two identical memory channels shown

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Supported Configurations: Per Channel (Single-Sided Assy)

Number of Die / structure	# ranks	2Gbit				4Gbit			
		LPDDR3		DDR3		LPDDR3		DDR3	
		x16	x32	x8	x16	x16	x32	x8	x16
2 Die, DFU	1 Rank		yes				yes		
4 Die, QFU (Spacer)	2 Ranks		yes				yes		
4 Die, QFD	1 Rank	yes			yes	yes			yes
8 Die, (µDFD/Interposer)	1 Rank			yes				yes	

	2Gbit	4Gbit
2 Die, DFU	0.5GB LPDDR3	1GB LPDDR3
4 Die, QFU (Spacer)	1GB LPDDR3	2GB LPDDR3
4 Die, QFD	1GB LPDDR3, DDR3	2GB LPDDR3, DDR3
8 Die, (mDFD/Interposer)	2GB DDR3	4GB DDR3

ALL CONFIGURATIONS POSSIBLE ON TYPE 3 PCB

Supported Configurations: Per Channel (Clamshell Assy)

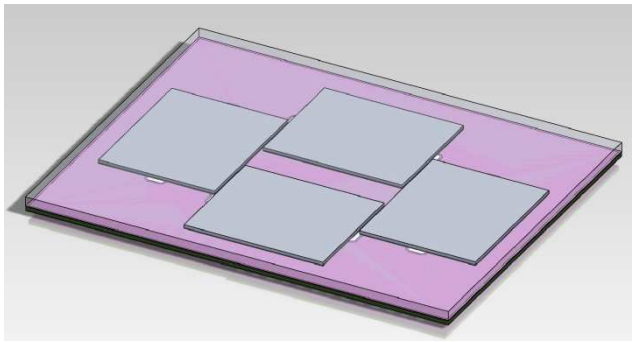
Number of Die / structure	# ranks	2Gbit				4Gbit			
		LPDDR3		DDR3		LPDDR3		DDR3	
		x16	x32	x8	x16	x16	x32	x8	x16
4 Die, DFU	2 Ranks		yes				yes		
8 Die, QFD	2 Ranks	yes			yes	yes			yes
16 Die, (µDFD/Interposer)	2 Ranks			yes				yes	

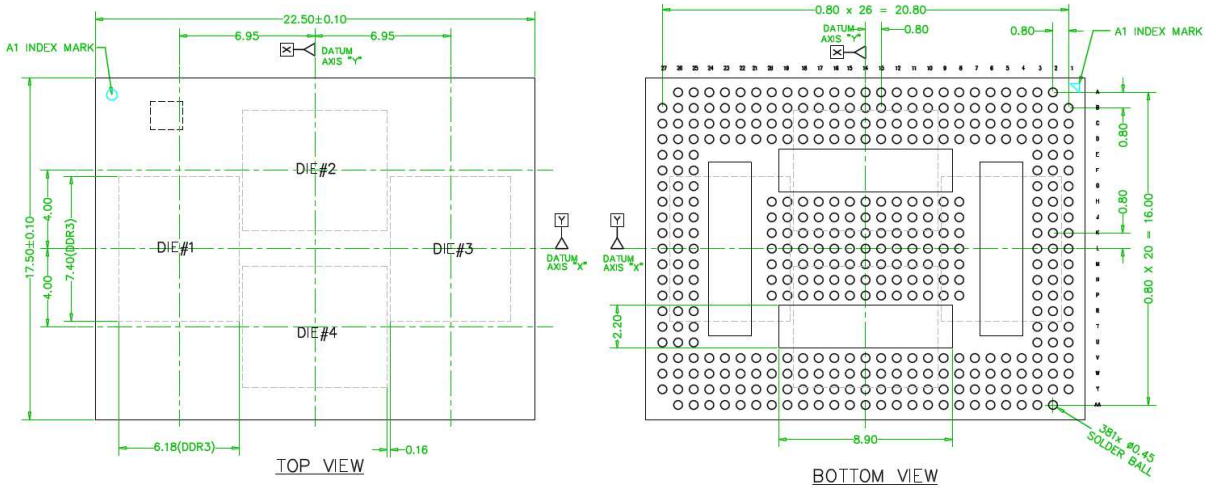
	2Gbit	4Gbit
2 Die, DFU (one side pop)	0.5GB LPDDR3	1GB LPDDR3
4 Die, DFU	1GB LPDDR3	2GB LPDDR3
8 Die, QFD	2GB LPDDR3, DDR3	4GB LPDDR3, DDR3
16 Die, (µDFD/Interposer)	4GB DDR3	8GB DDR3

ALL CONFIGURATIONS POSSIBLE ON TYPE 3 PCB

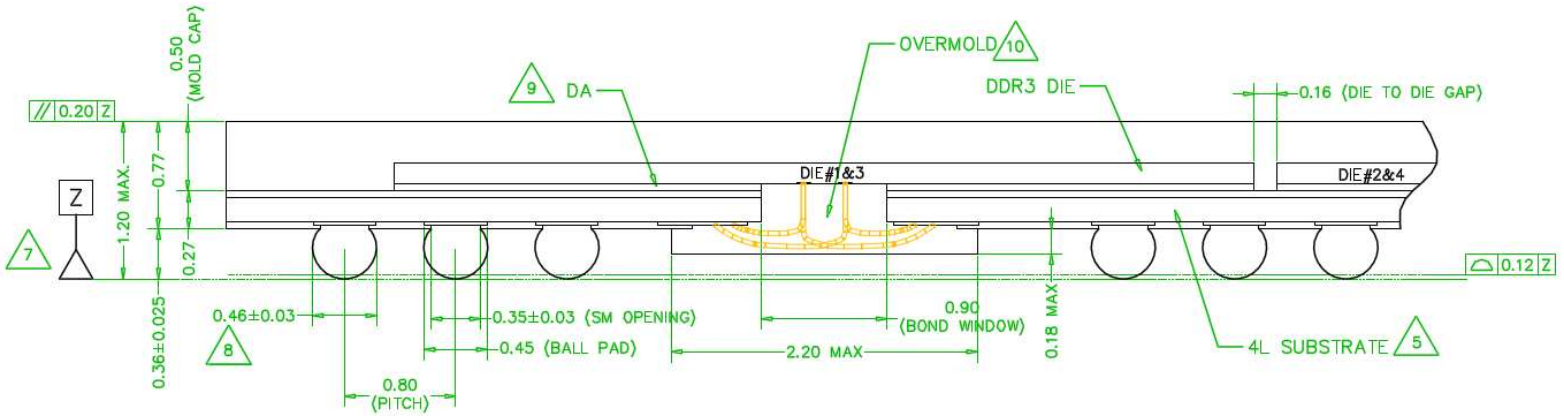
Thermal

Planar QFD Configuration

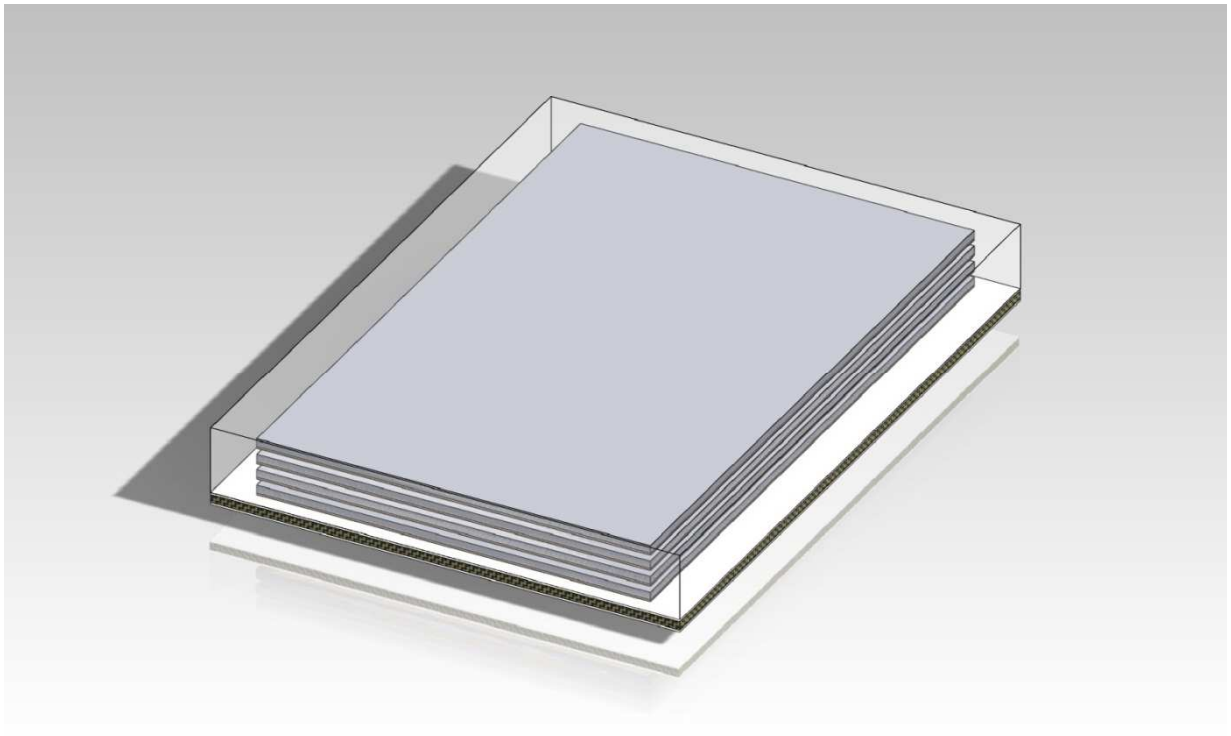




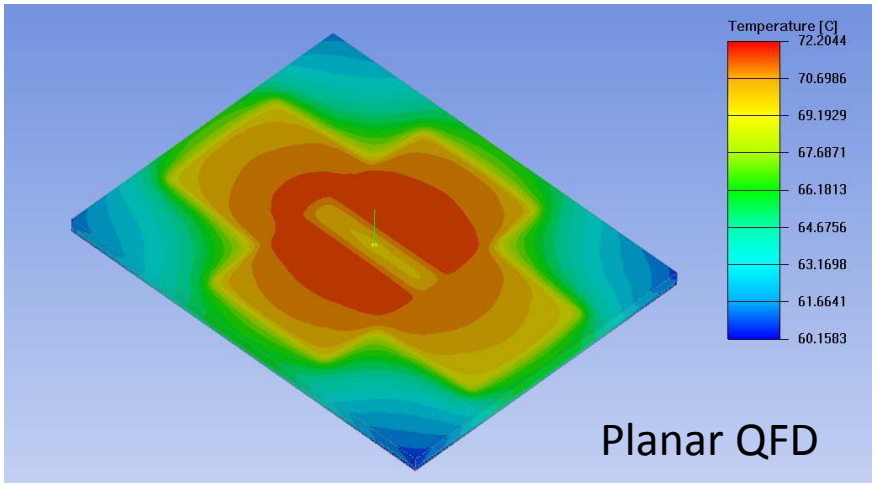
PACKAGE SECTION DETAIL



JEDEC Standard QDP Configuration

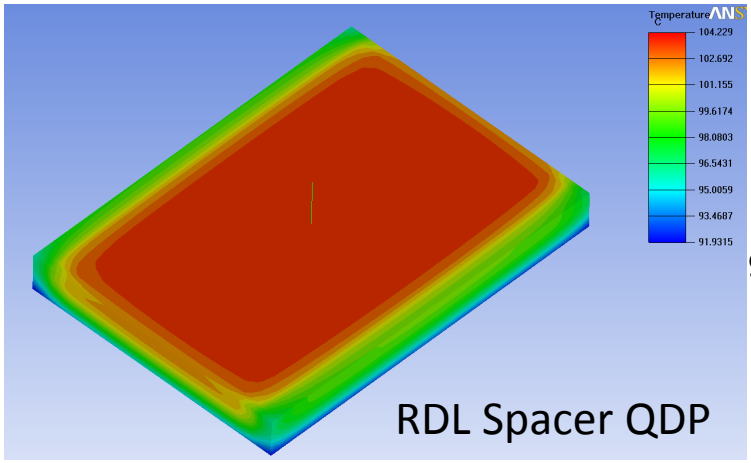


Planar QFD vs JEDEC Std QDP thermal modeling results



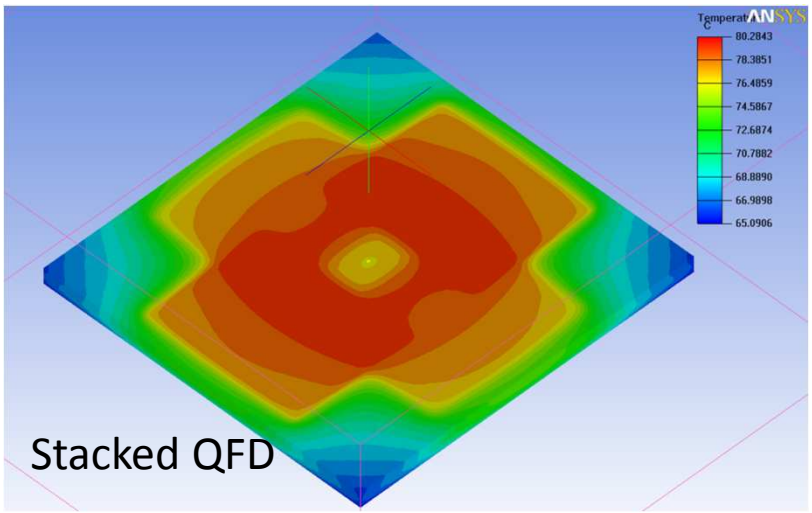
72.2C

60.2C



104C

91.9C

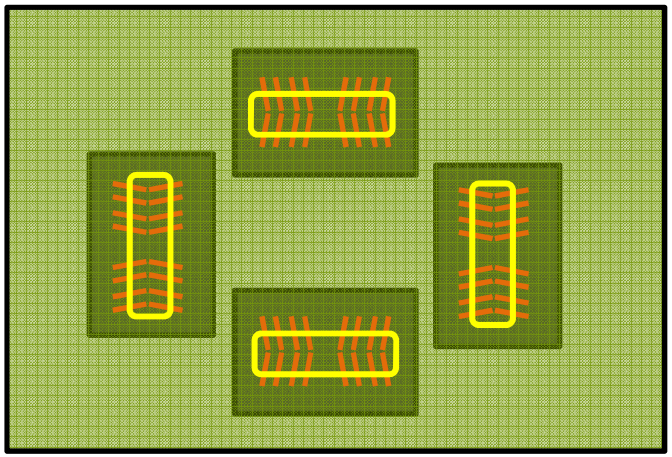


80C

65C

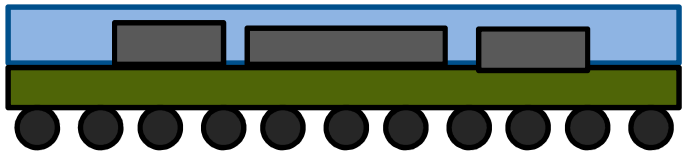
Manufacturing

Structures compared

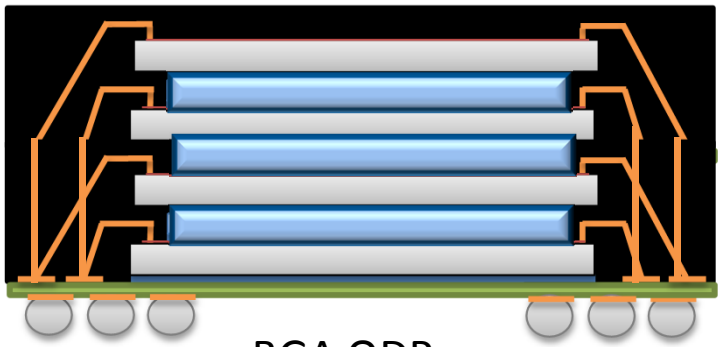


WIREBONDED THROUGH WINDOW IN SUBSTRATE

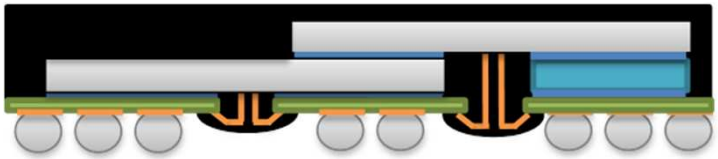
BGA DDP



Invensas QFD

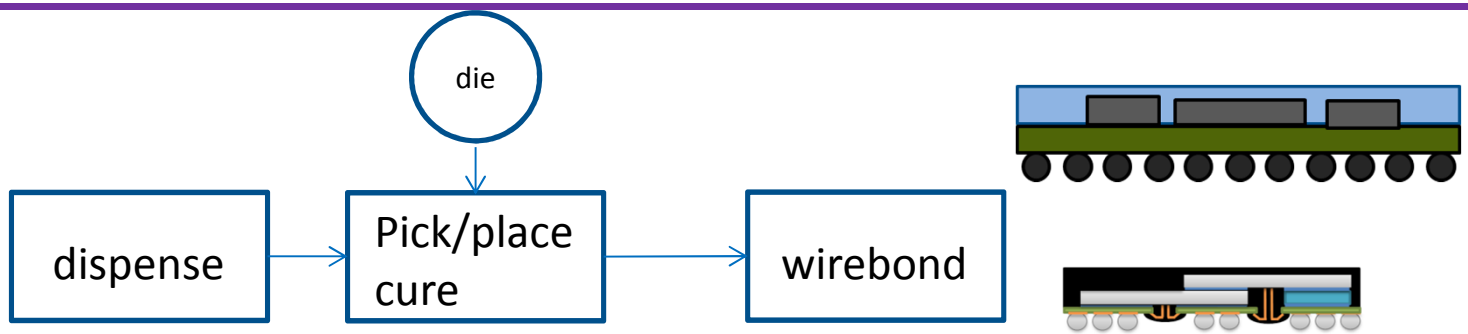


BGA QDP

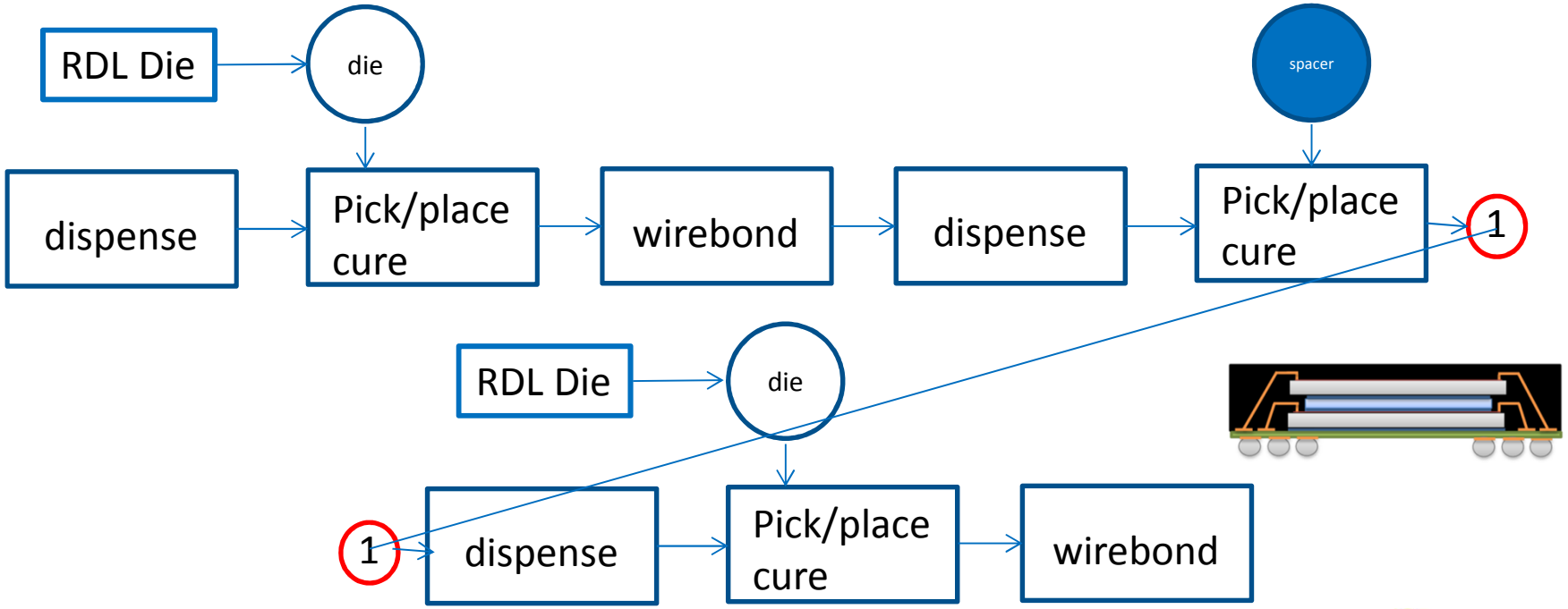


Invensas DFD

Process flows: QFD and JEDEC DDP



Planar QFD flow (same as single die package!)



Twindie DDP flow

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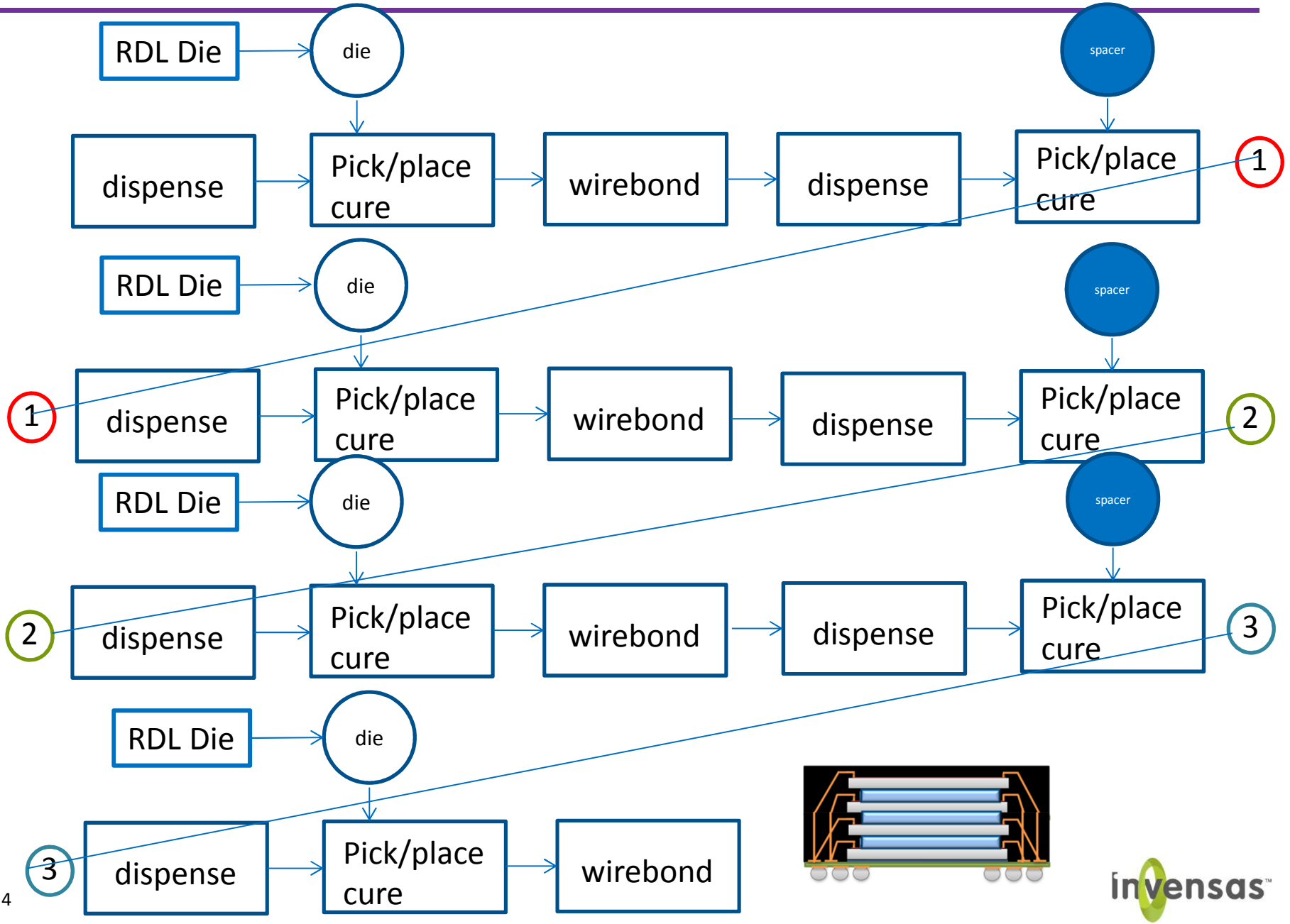
Process flows: JEDEC QDP



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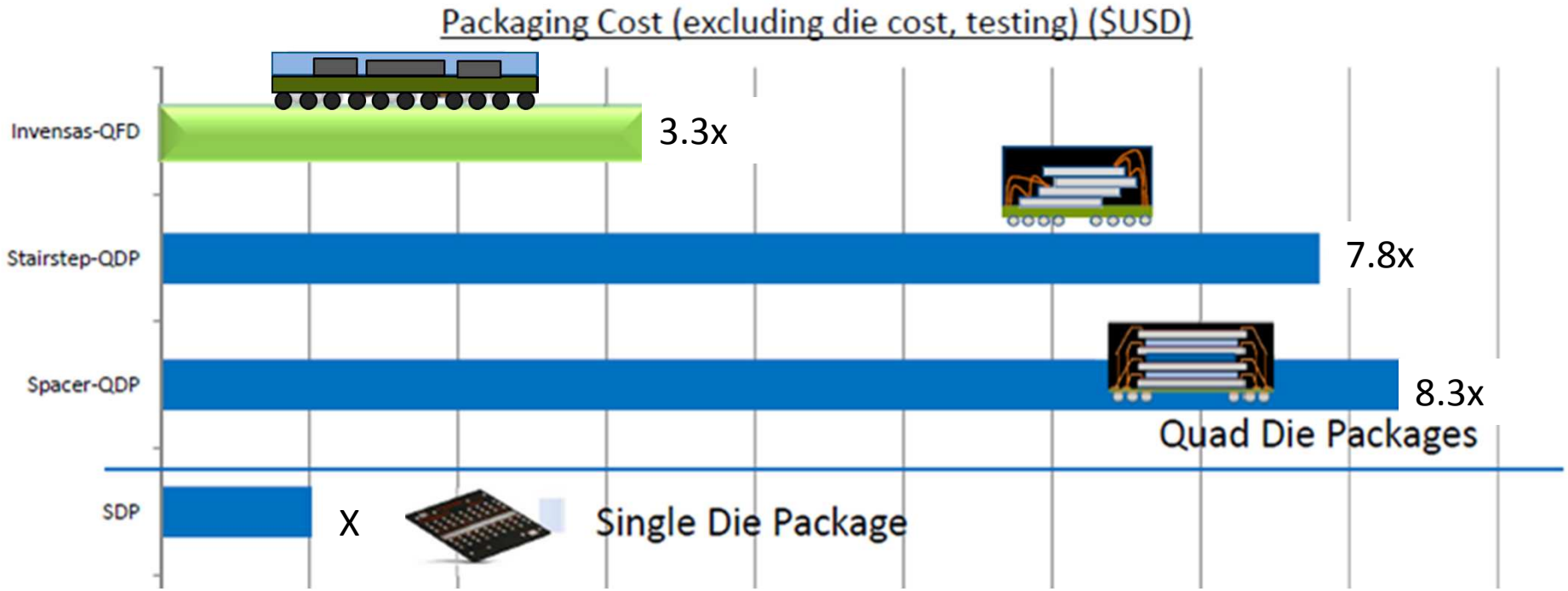
Quad Die Packaging Cost Comparison



Invensas QFD is cheaper per die than SDP!

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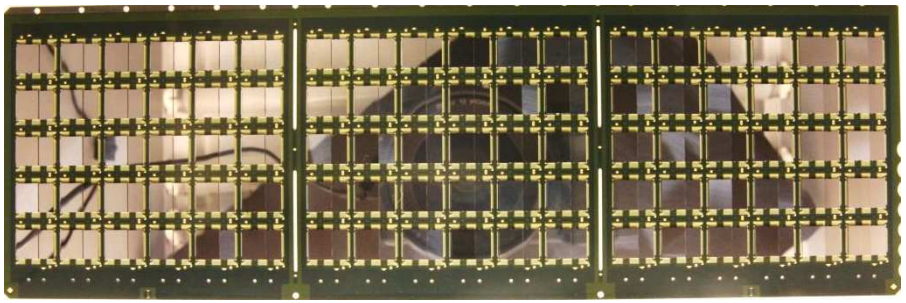
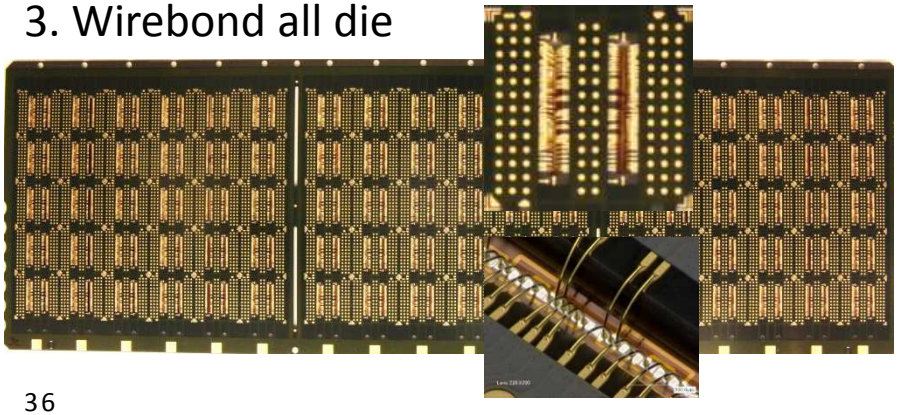
DFD / QFD Manufacturing

1. Start with the PCB substrate strip

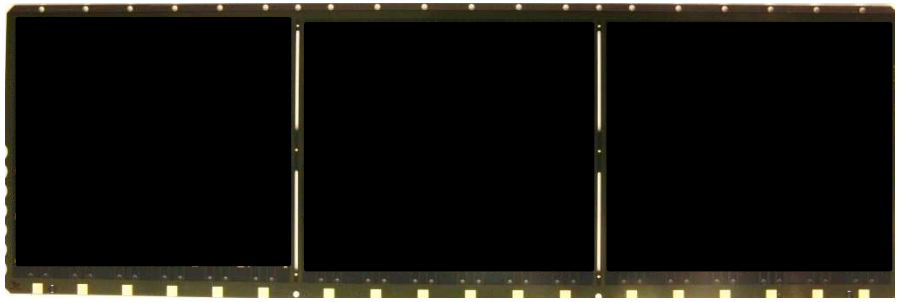
2. Die Attach all die



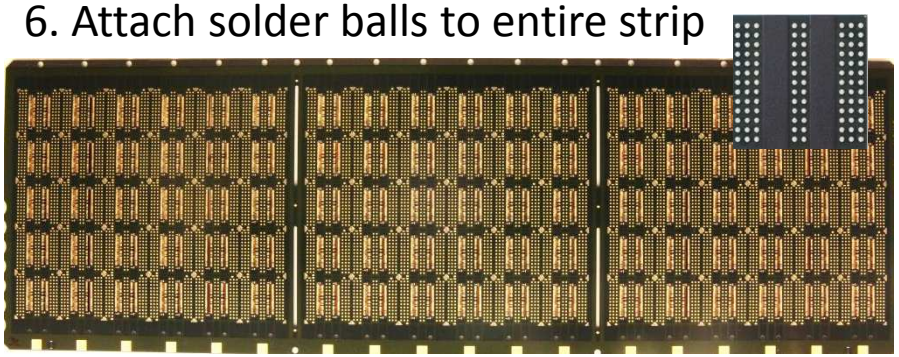
3. Wirebond all die



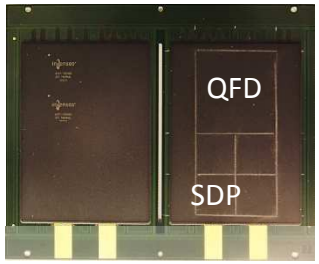
4. Mold entire strip



6. Attach solder balls to entire strip



7. Singulate



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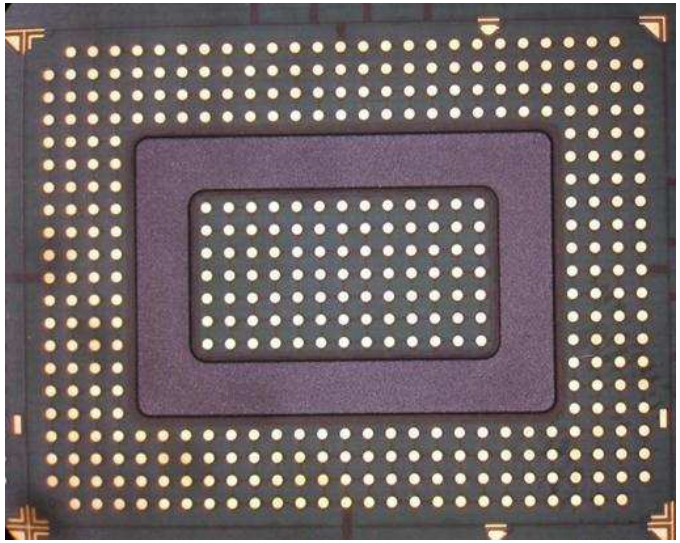
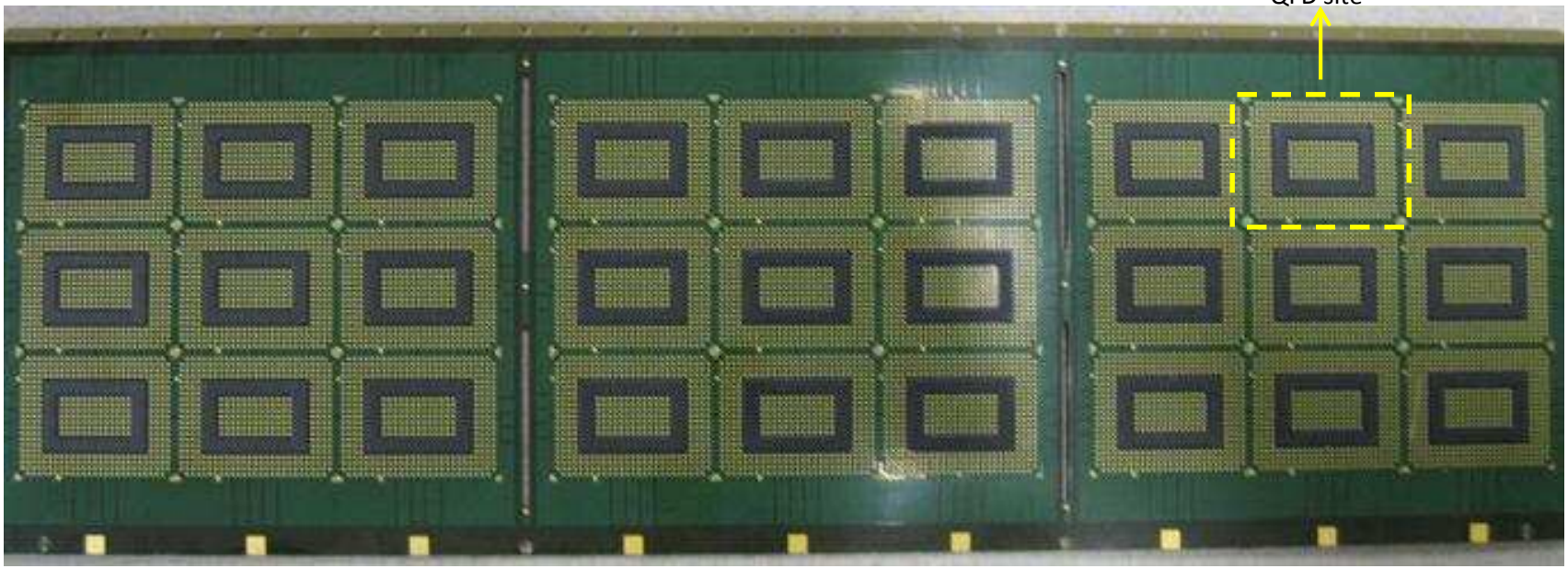
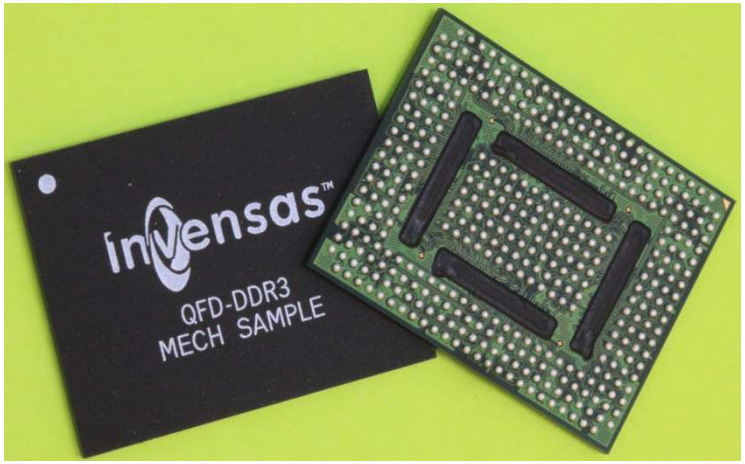
DFD / QFD Manufacturing

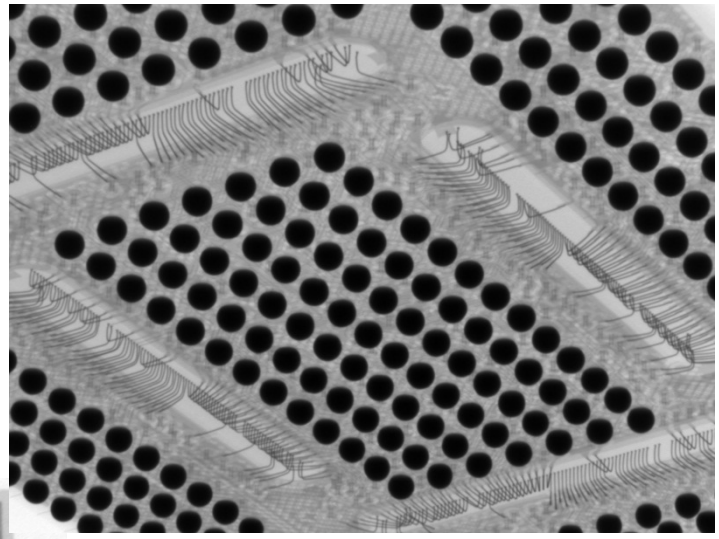


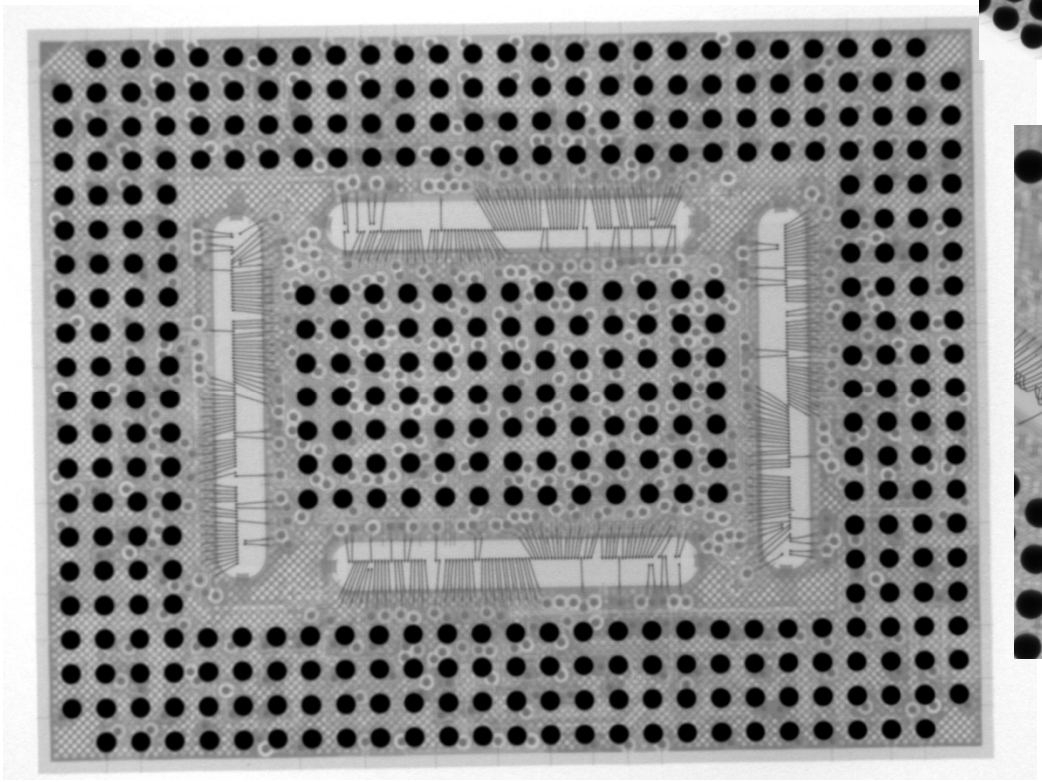


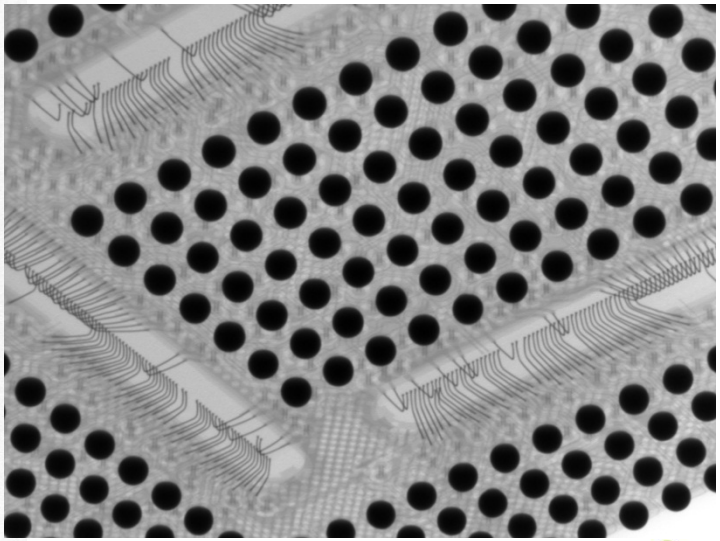
QFD assembly strip

Optical and 2D X-Ray images









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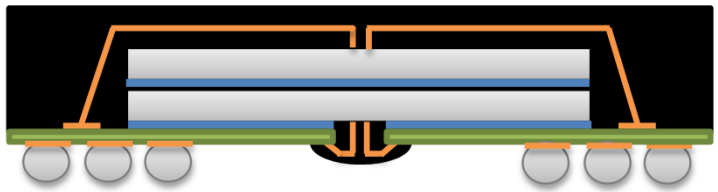
DFD for DIMMs and RDIMMs

Key Difficulties with Dual Die DRAM Package Structures

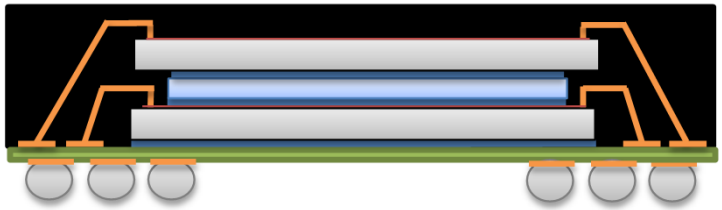
Dominated
by Gold Cost



Opposing-Face DDP

Asymmetric signal and power delivery
Thermal
Thickness
Cost

Dominated
by RDL Cost

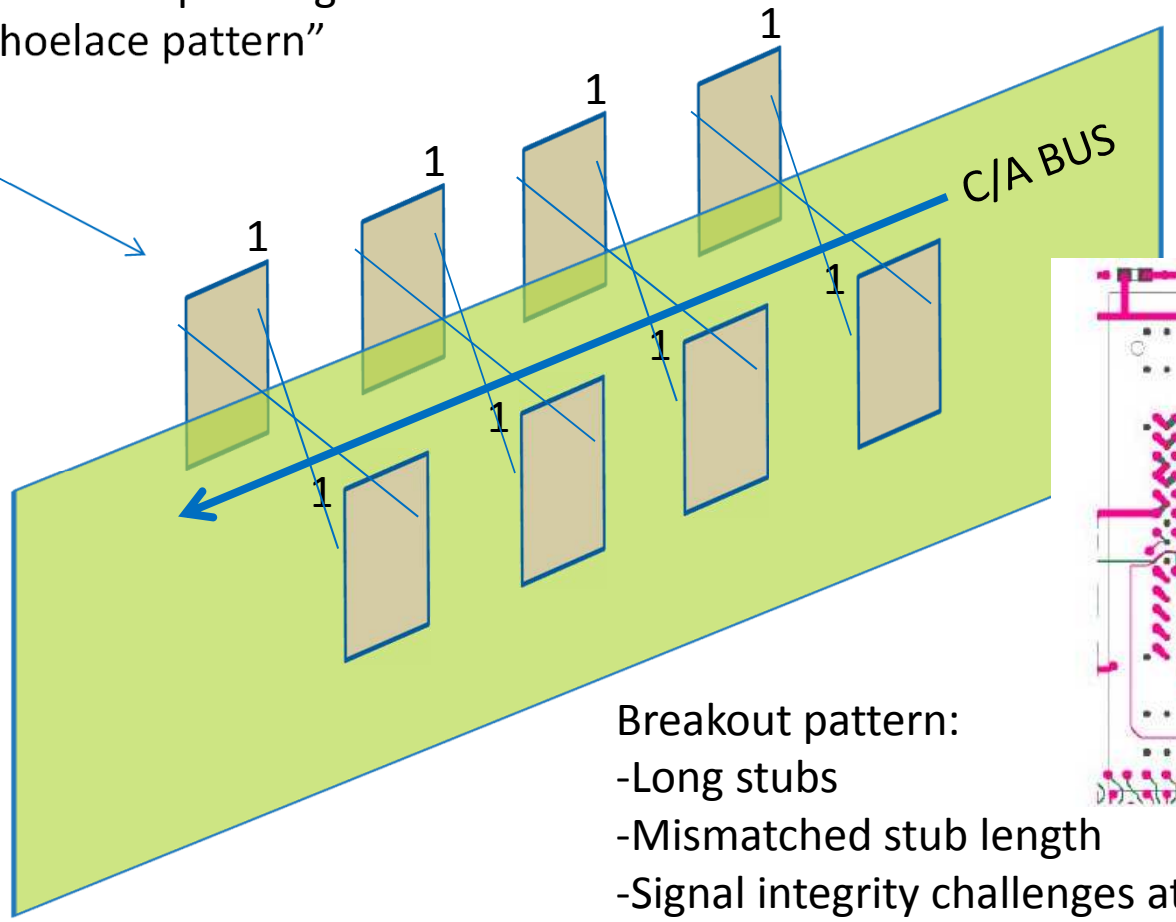


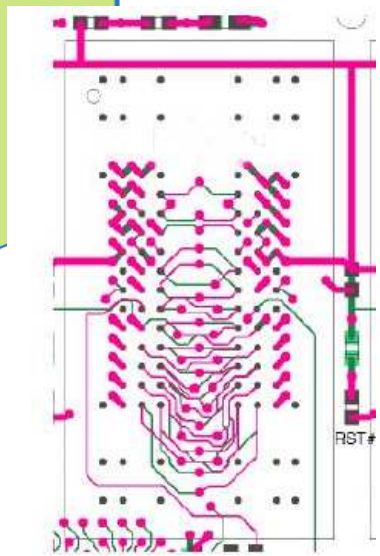
Face-Up DDP with RDL

Power and Signal Delivery via RDL
Thermal
Thickness
Cost

PCB Layout difficulties with standard DDPs

Must interconnect same-named bussed signal to corresponding leads using “shoelace pattern”





Breakout pattern:
-Long stubs
-Mismatched stub length
-Signal integrity challenges at high frequency

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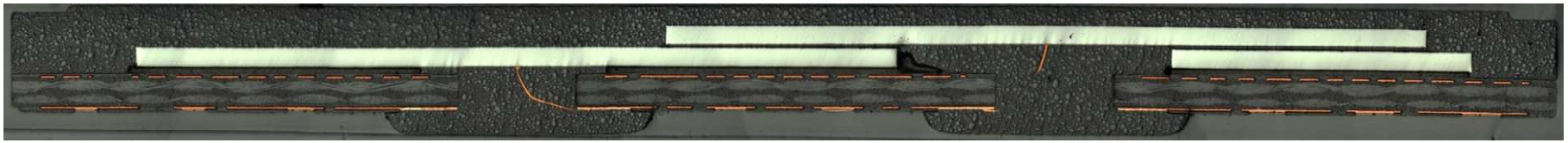
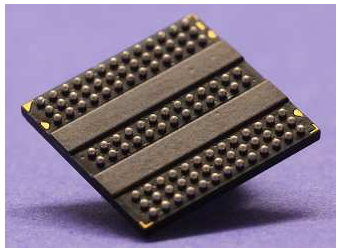
Newly Developed Package: Invensas Dual Face Down: DFD™

Invensas Dual Face Down

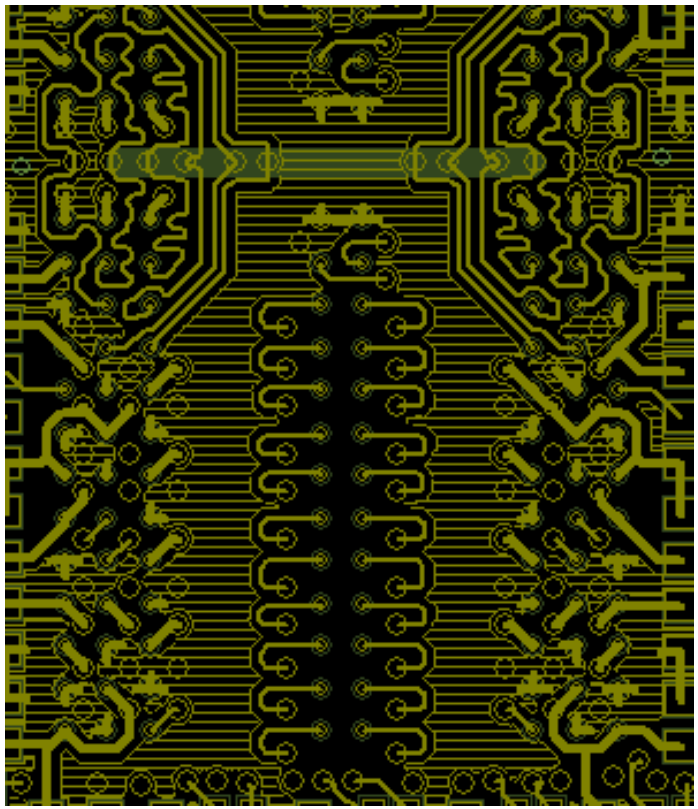
Symmetric performance: similar to Single Die Package
Best thermals
Thinnest structure (no topside wire loops)
Lowest manufacturing cost



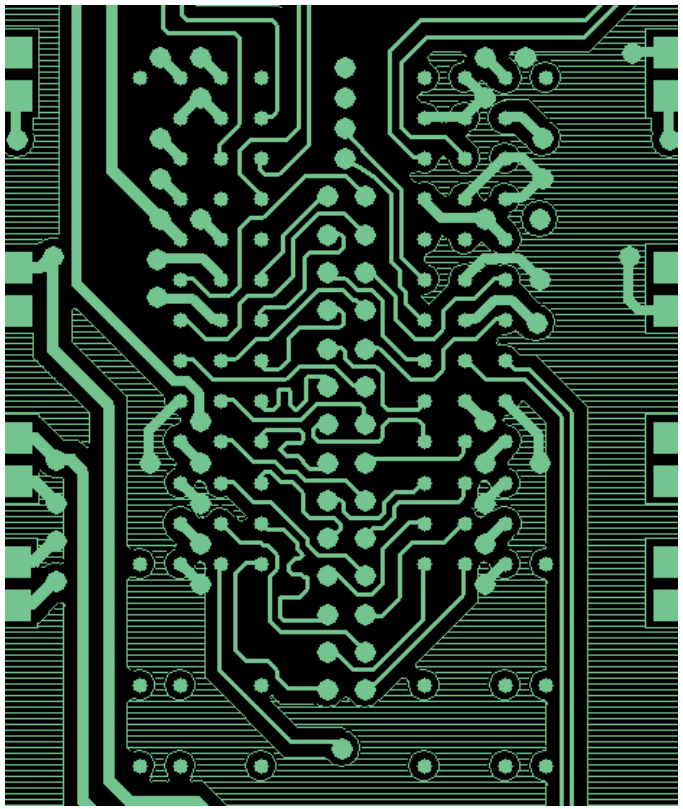


Simplified Breakout Using DFD

Invensas DFD



Standard BGA



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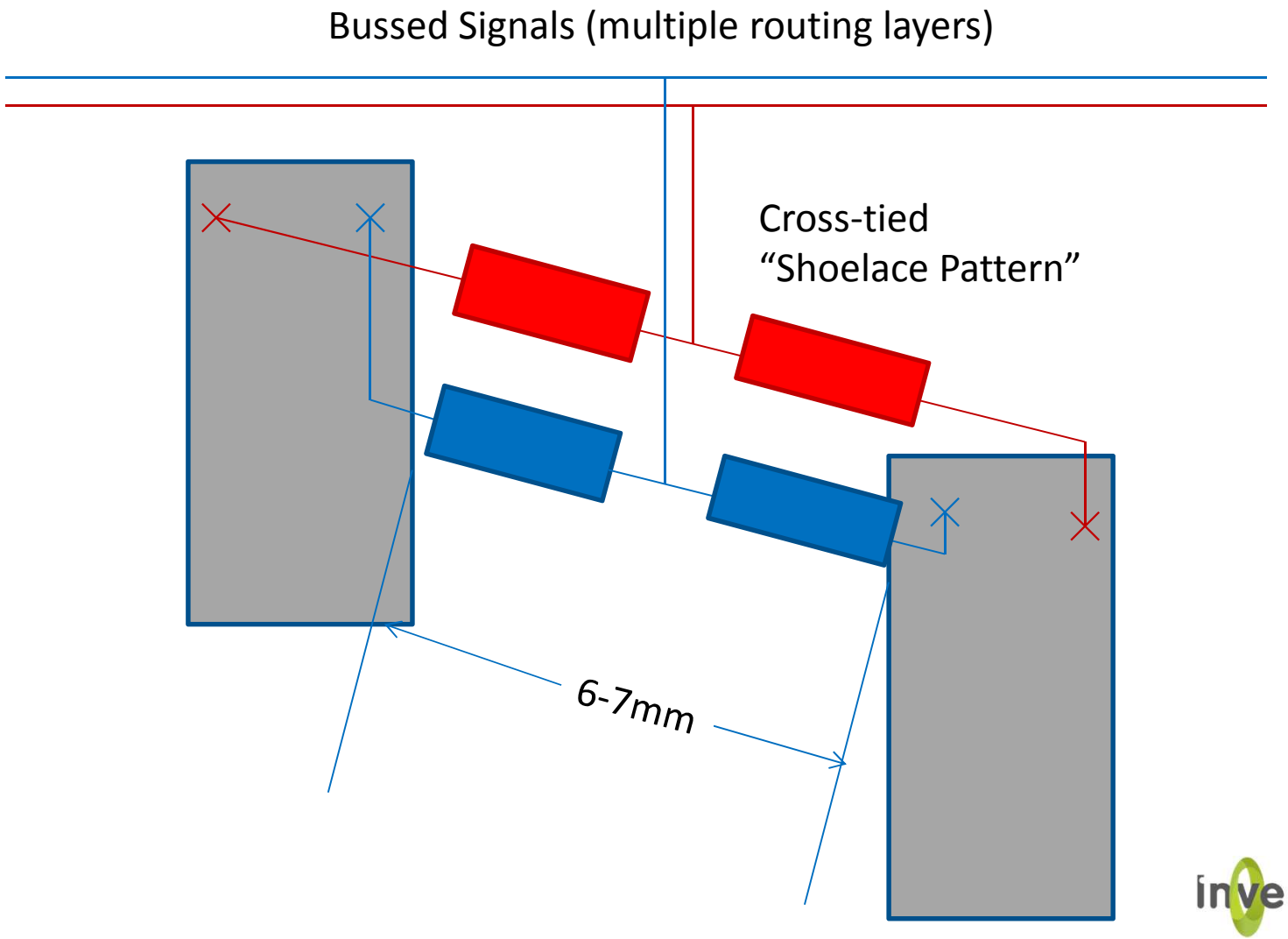
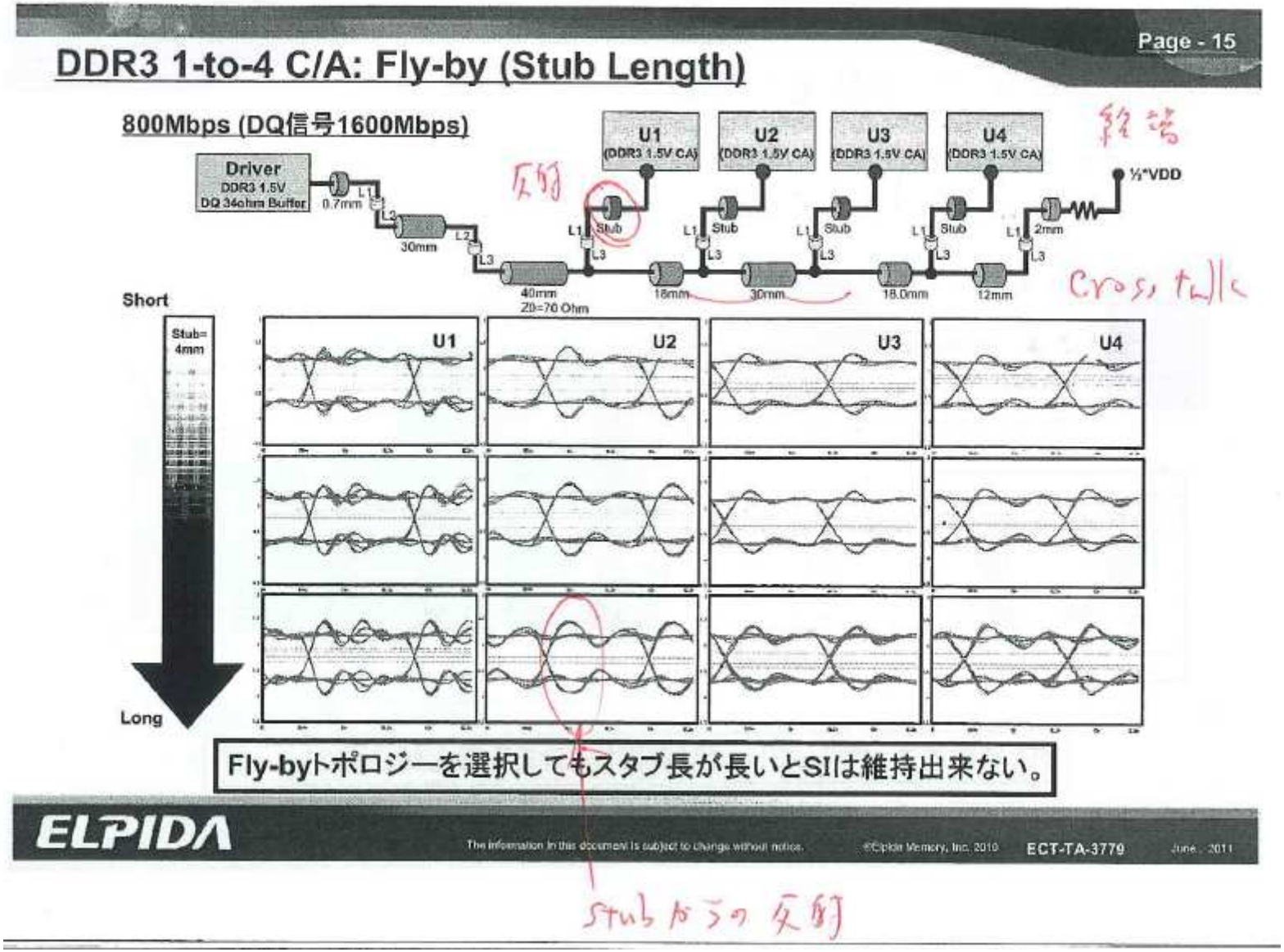
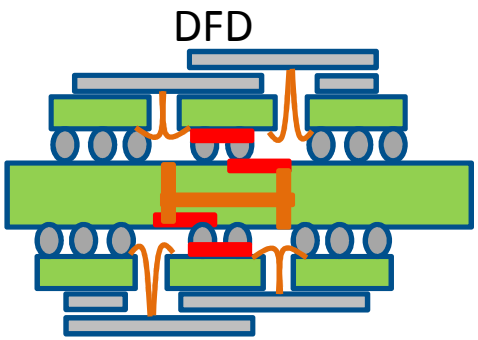
Electrical View: Standard BGA Package Breakout Stubs

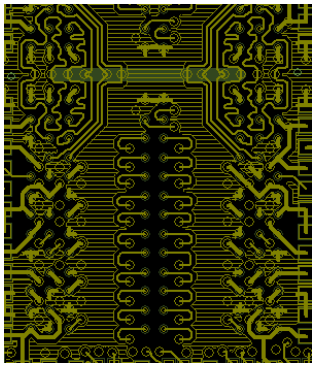


C/A Bus: Stub Issue

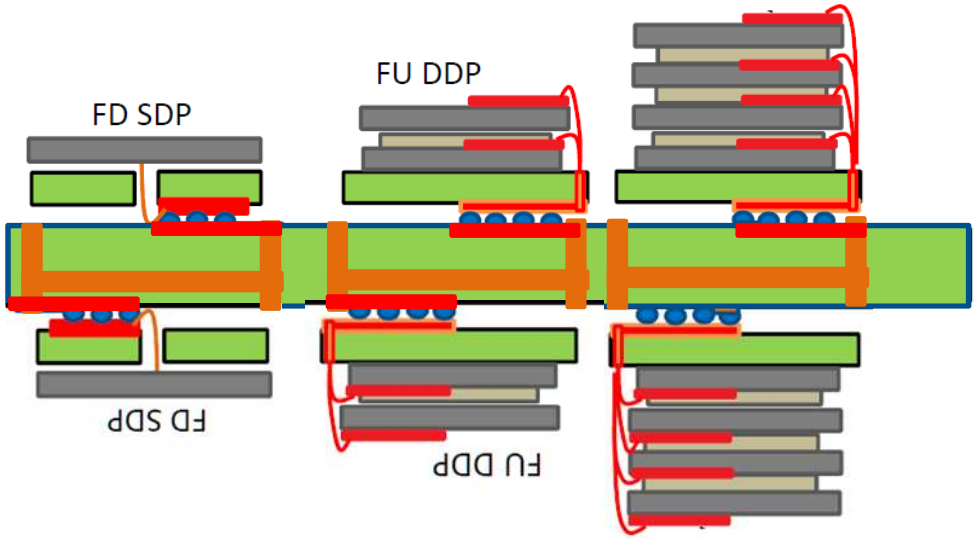


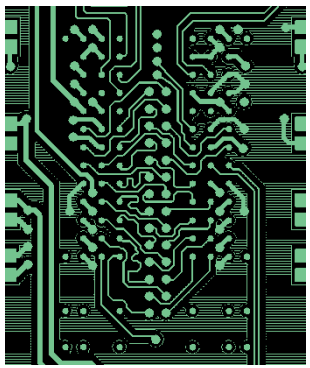
C/A Bus: Stubs





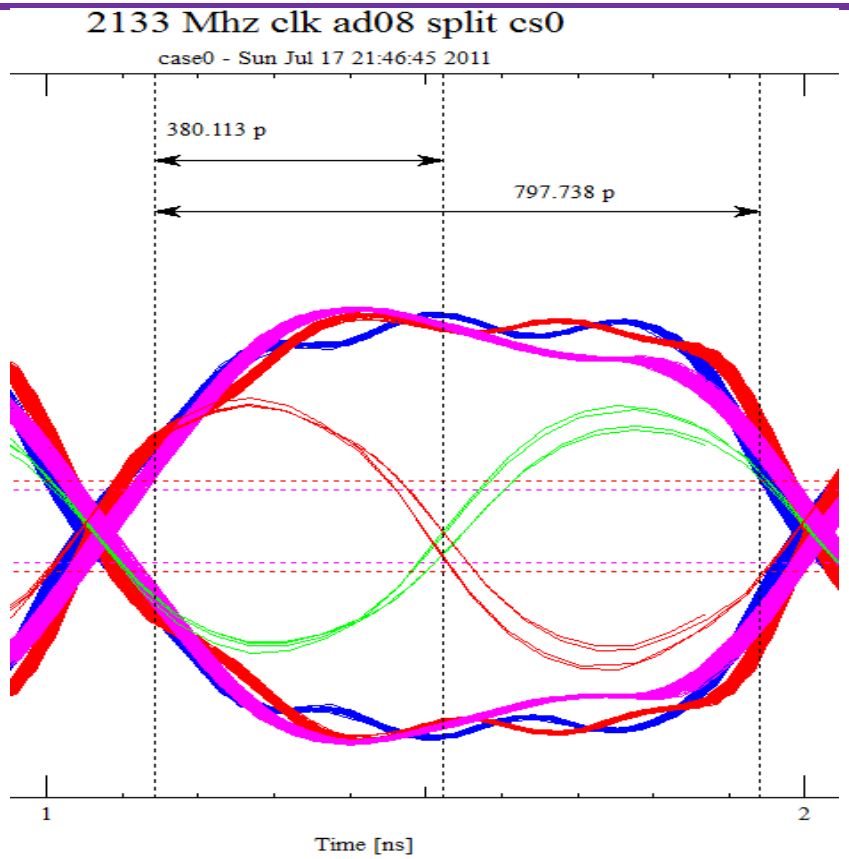
Invensas DFD

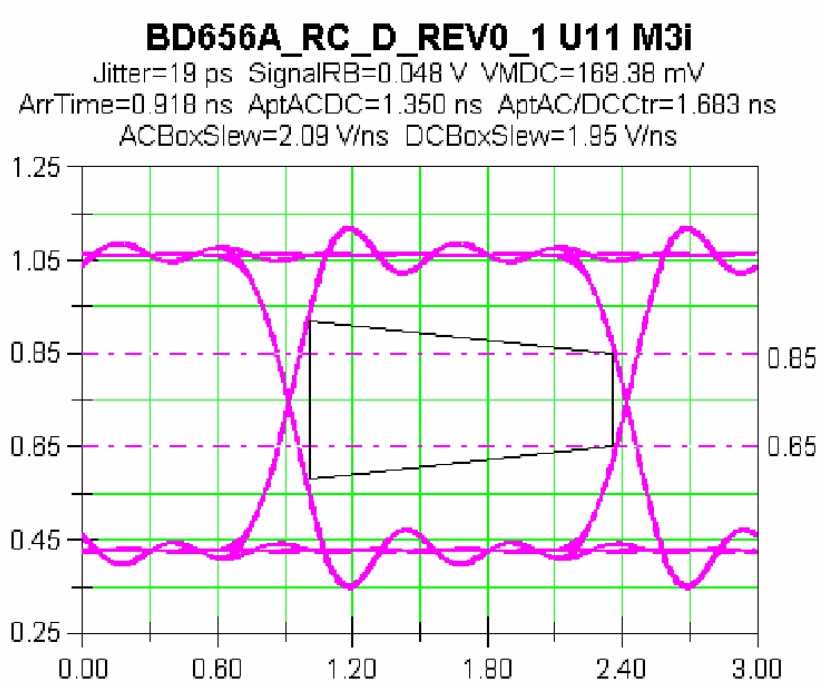




Standard BGA

A/Clk Simulation at DDR3-2133: 16% more margin at 75% faster operation





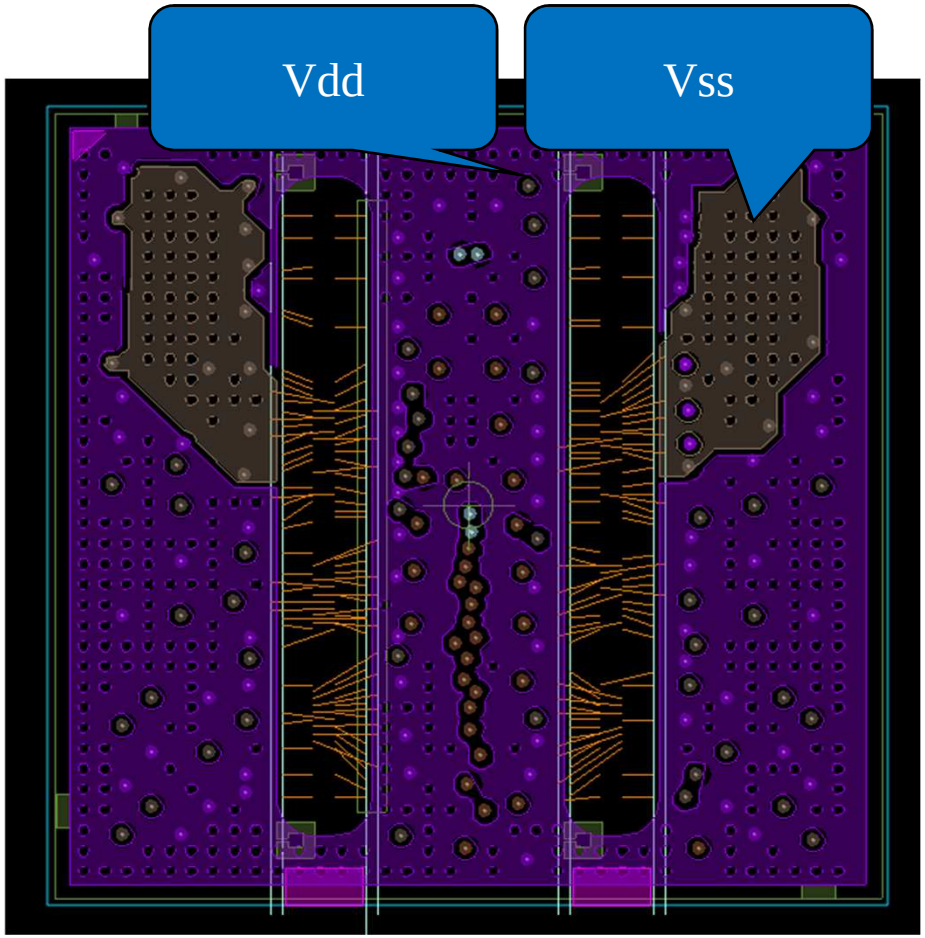
DFD @ 2133

- Window = 798 ps
- Ideal tCK = 938 ps
- 85% of a tCK

JEDEC r/c D @ 1333

- Window = 1093 ps
- Ideal tCK = 1500 ps
- 73% of a tCK

Electrical Considerations: Reference Planes for signals



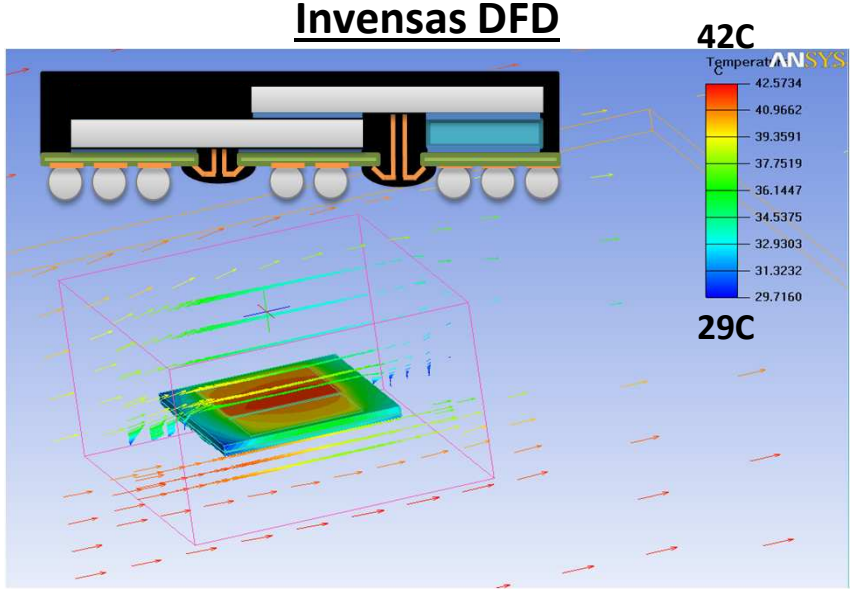
All C/A signals referenced to Vdd in JEDEC DIMM Specs

DFD references C/A signals to Vdd in package providing consistent image current path: controller to memory die

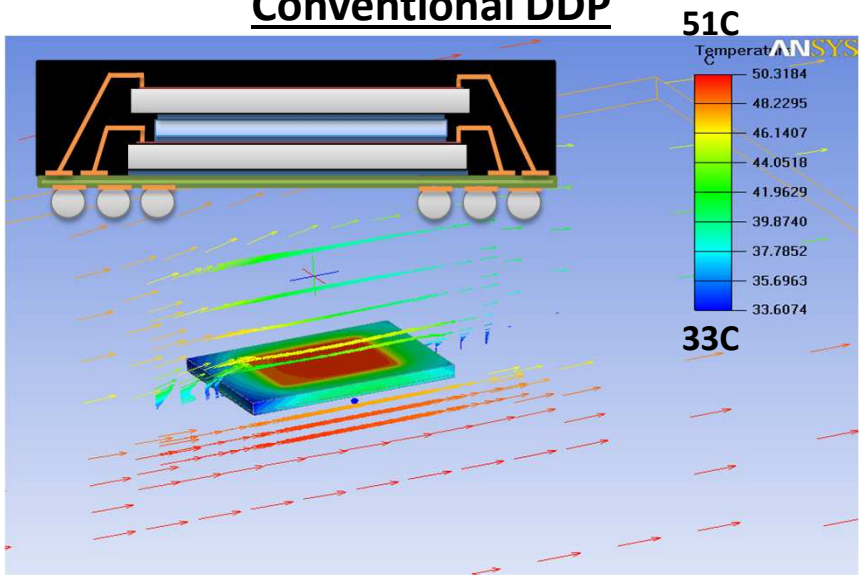
DFD also references all non C/A signals to Vss for consistent image current path: controller to memory die

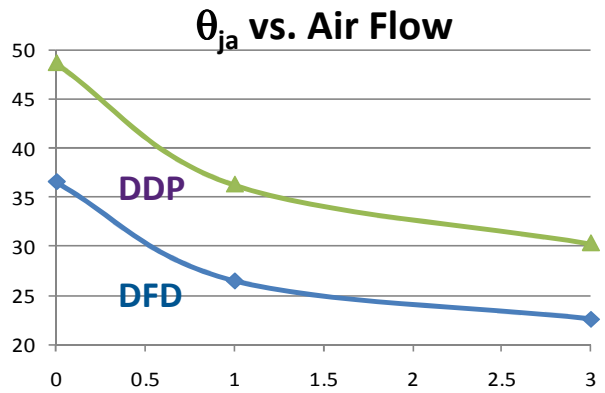
Forced Air Convection Heat Transfer Advantage

Invensas DFD



Conventional DDP





Configuration	DFD (°C/W)	DDP (°C/W)	Delta from DDP
θ_{ja} still air	36.6	48.7	-25%
θ_{ja} @ 1m/s	26.5	36.3	-27%
θ_{ja} @ 3m/s	22.6	30.3	-25%

~25% lower θ_{ja} for DFD vs. conventional DDP package

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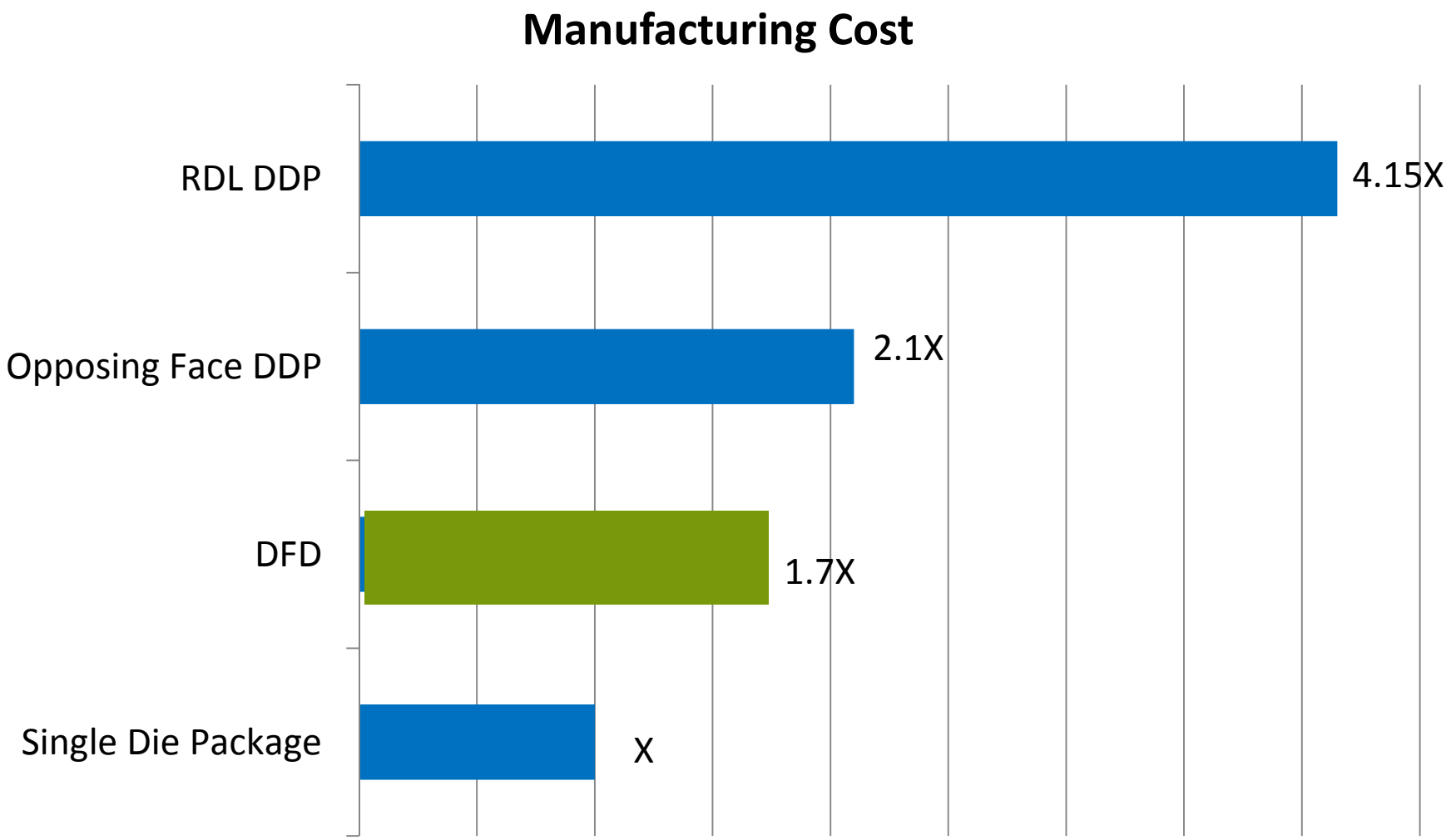
Cost Comparison



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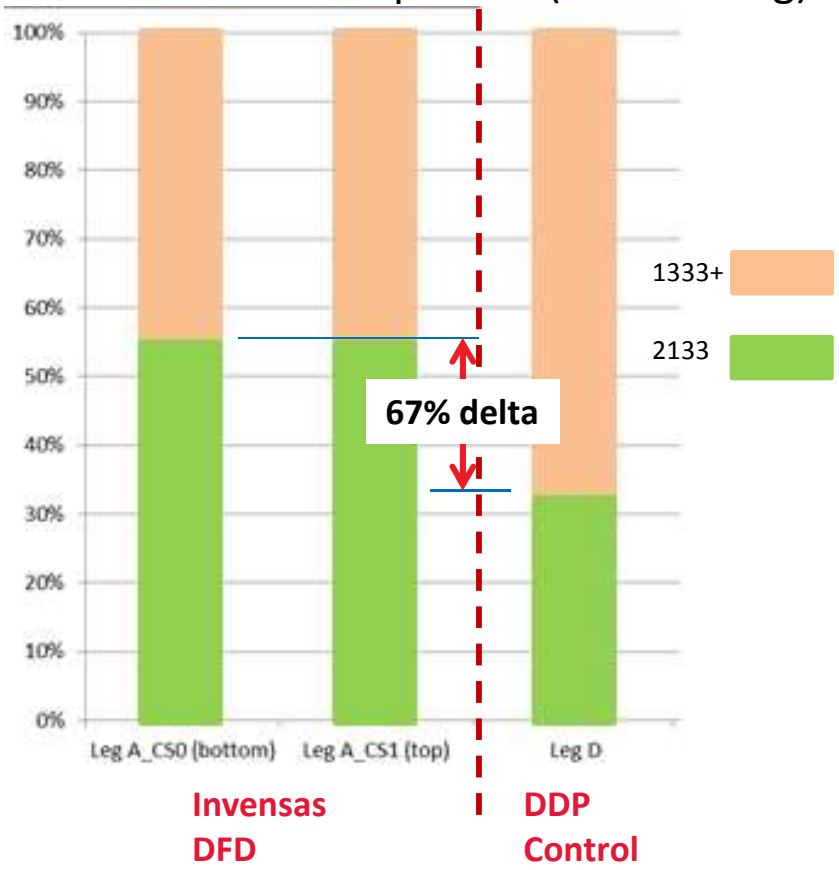
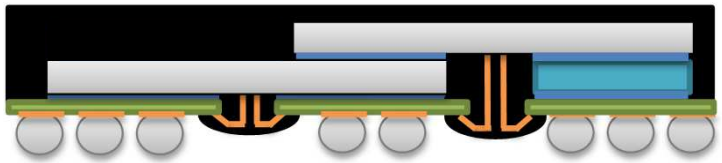
Sort Yield Advantage: Invensas DFD vs Conventional DDP

Bin splits of yielded goods improved significantly

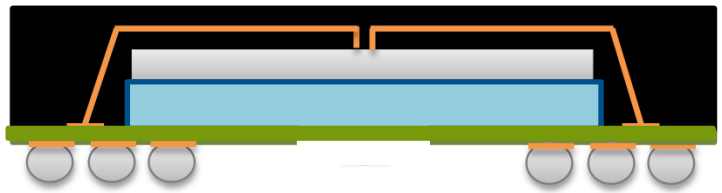
Speed Bin Yield vs. Control

1000 unit sample size (95°C testing)





Leg A bottom, Leg B top



Leg D (top die only w/o substrate routing for lower die: performance is therefore optimistic)

- 67% Improvement in 2133MT/s Yield vs Control using same wafer lot

Measured RDIMM Results

Overview of RDIMM Evaluation Vehicle

- Invensas developed an 8GByte Quadrank x72 ECC RDIMM using the DFD package technology (dual 1 Gbit die/package)
- Each module contains 72 die of 1Gbit capacity (x4 die organization)
- Standard RDIMM edge connector/module form factor
- Initial testing: full speed in-system with Memtest 86
- Additional at-speed probing of signals in-system with 12GHz DSA

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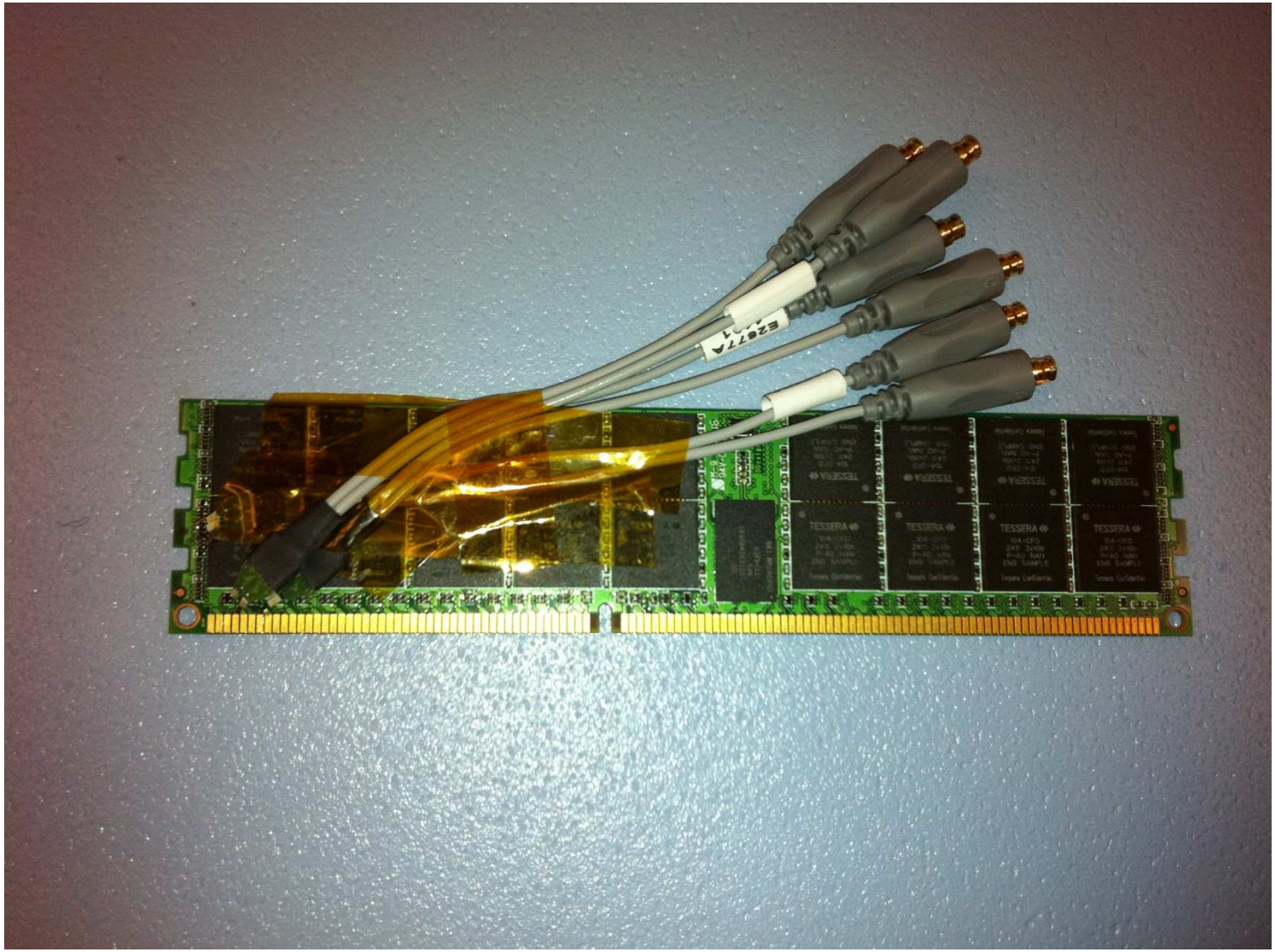
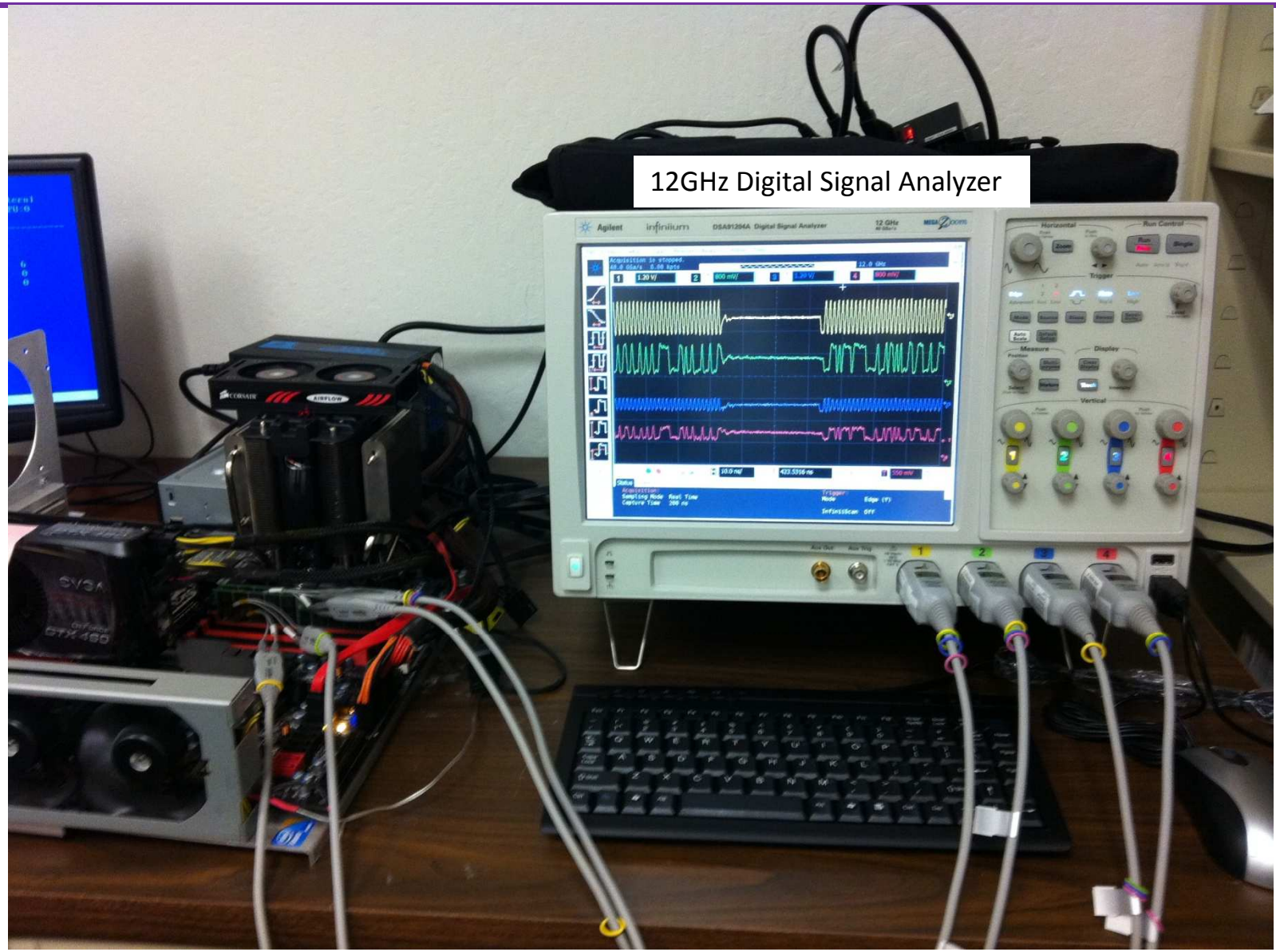
Instrumented DIMM With Probes Solder-Attached

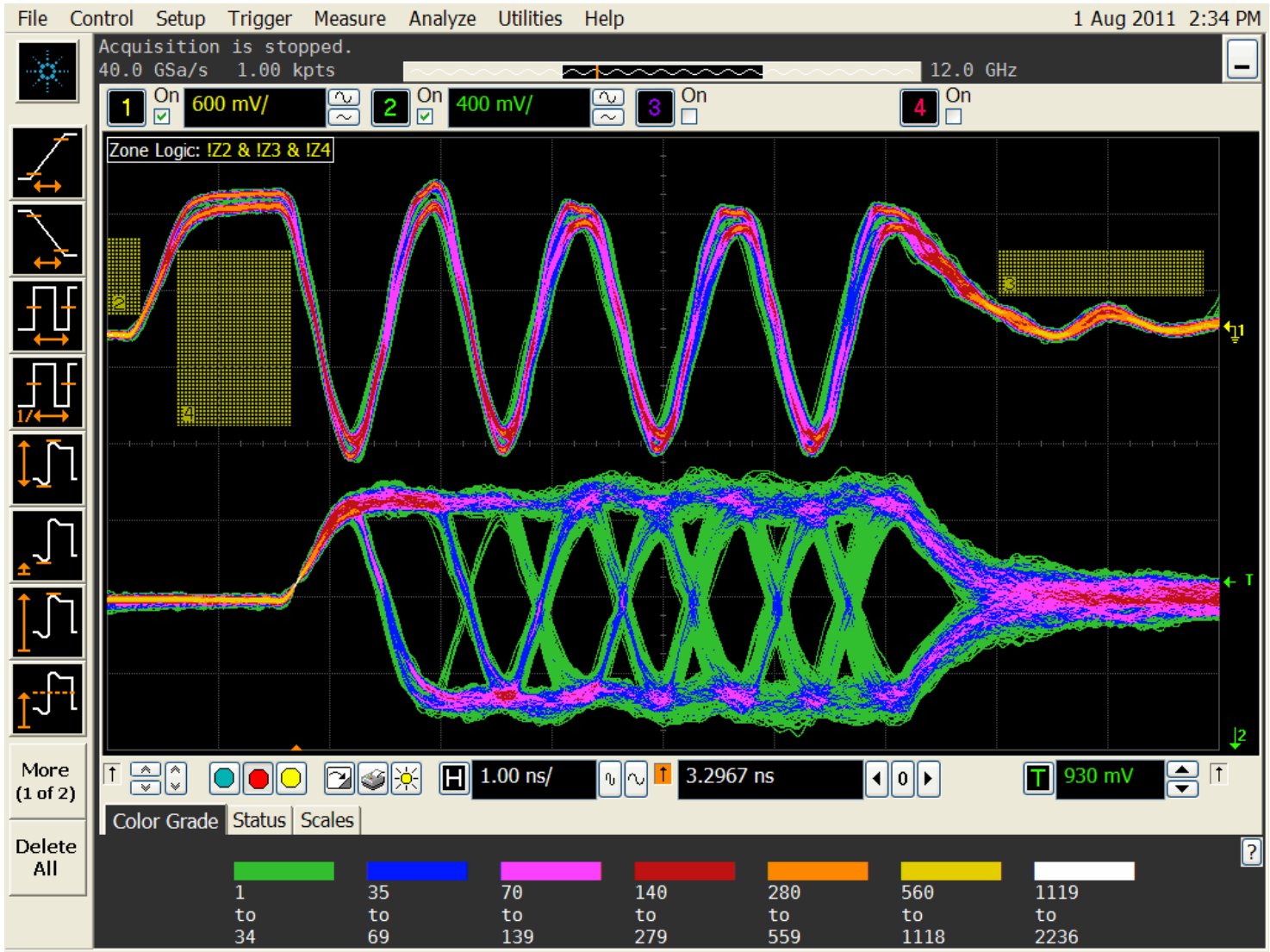


For full-speed in-system probing of DQ, DQS

In-System Test Setup

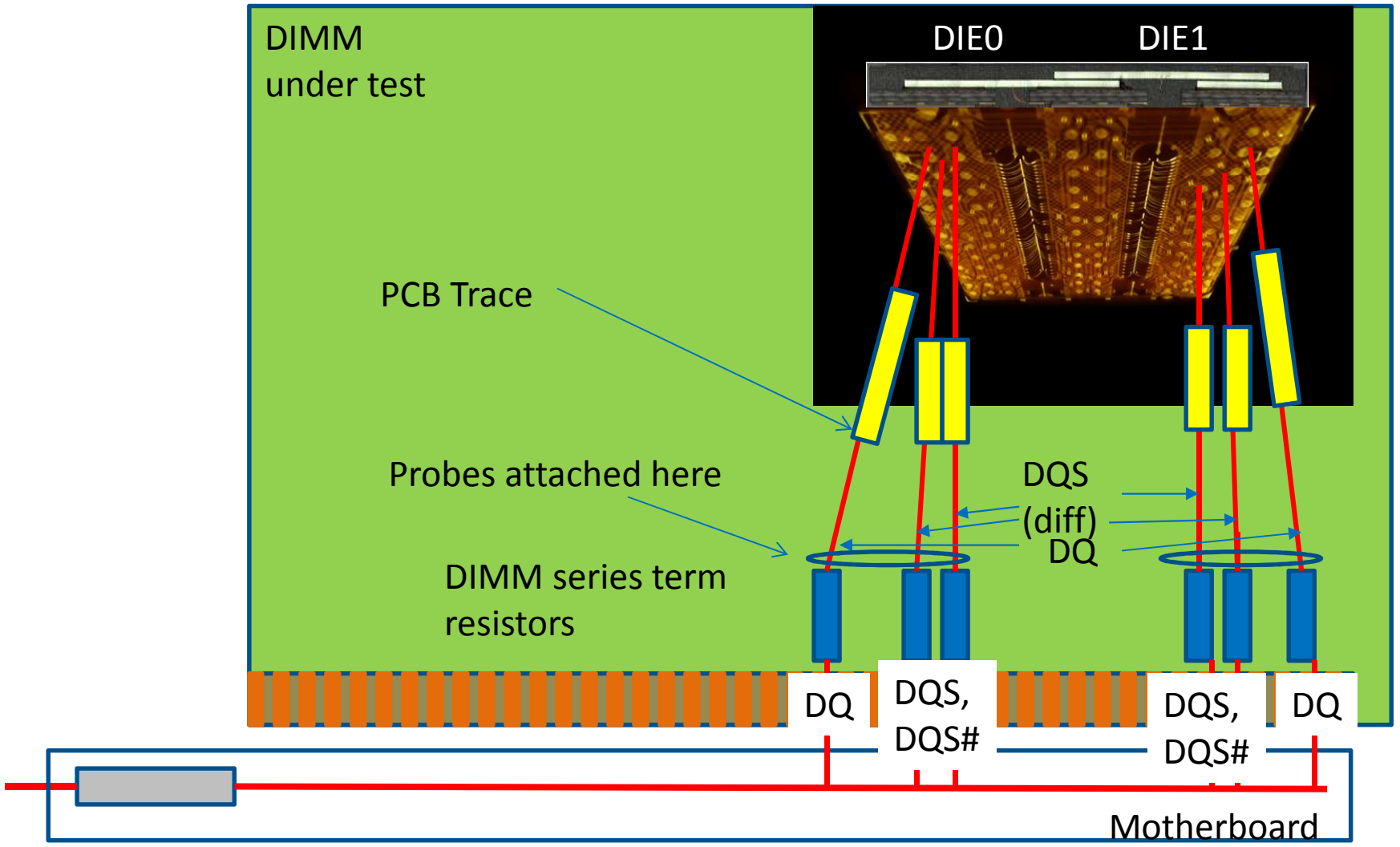


Read Eye Diagram (Quadrank RDIMMs, 2DPC @1600MT/s)



Symmetric Performance

(DQx, DQS from die in same package)



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DFD Reads Same Package, Both Die

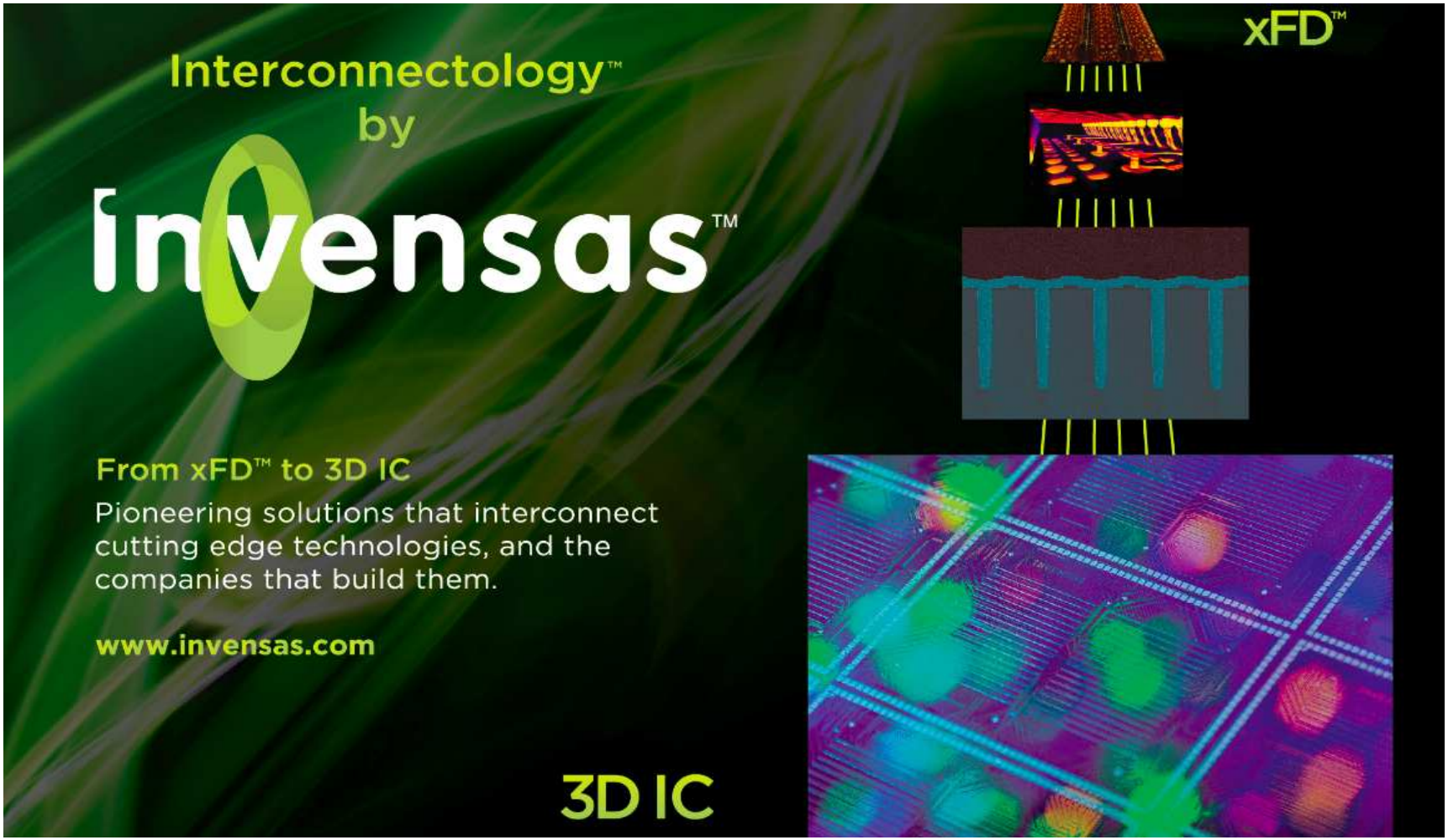
DQS (DIE0)

DQS (DIE1)

DQ (DIE1)

DQ (DIE0)

Thank You



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